

## Features

- Low power 3.3V 32 macrocell CPLD
- 4.5 ns pin-to-pin logic delays
- System frequencies up to 213 MHz
- 32 macrocells with 750 usable gates
- Available in small footprint packages
  - 48-ball CS BGA (36 user I/O pins)
  - 44-pin VQFP (36 user I/O)
  - 44-pin PLCC (36 user I/O)
- Optimized for 3.3V systems
  - Ultra-low power operation
  - Typical Standby Current of 17  $\mu$ A at 25° C
  - 5V tolerant I/O pins with 3.3V core supply
  - Advanced 0.35 micron five layer metal EEPROM process
  - Fast Zero Power™ (FZP) CMOS technology
  - 3.3V PCI electrical specification compatible outputs (no internal clamp diode on any input or I/O, no minimum clock input capacitance)
- Advanced system features
  - In-system programming
  - Input registers
  - Predictable timing model
  - Up to 23 available clocks per function block
  - Excellent pin retention during design changes
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
  - Four global clocks
  - Eight product term control terms per function block
- Fast ISP programming times
- Port Enable pin for dual function of JTAG ISP pins
- 2.7V to 3.6V supply voltage at industrial temperature range
- Programmable slew rate control per macrocell
- Security bit prevents unauthorized access
- Refer to the CoolRunner XPLA3 family data sheet ([DS012](#)) for architecture description

## Description

The CoolRunner™ XPLA3 XCR3032XL device is a 3.3V, 32-macrocell CPLD targeted at power sensitive designs that require leading edge programmable logic solutions. A total of two function blocks provide 750 usable gates. Pin-to-pin propagation delays are as fast as 4.5 ns with a maximum system frequency of 213 MHz.

## TotalCMOS Design Technique for Fast Zero Power

CoolRunner XPLA3 CPLDs offer a TotalCMOS™ solution, both in process technology and design technique. Xilinx CPLDs employ a cascade of CMOS gates to implement its sum of products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs that are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to [Figure 1](#) and [Table 1](#) showing the  $I_{CC}$  vs. Frequency of our XCR3032XL TotalCMOS CPLD (data taken with two resettable up/down, 16-bit counters at 3.3V, 25°C).

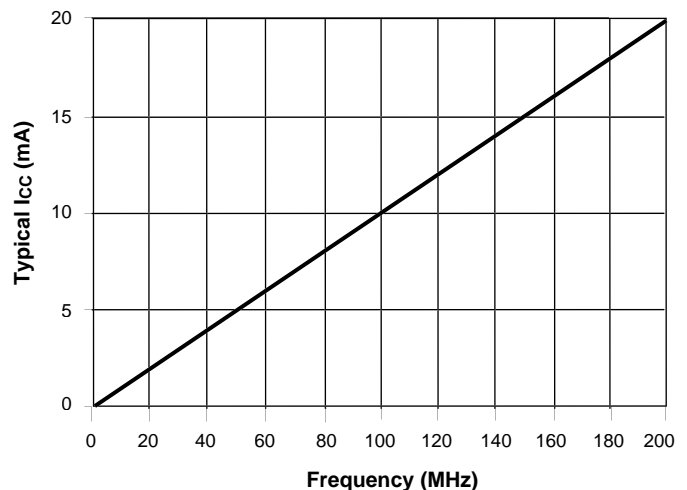


Figure 1:  $I_{CC}$  vs. Frequency at  $V_{CC} = 3.3V, 25^{\circ}C$

Table 1:  $I_{CC}$  vs. Frequency ( $V_{CC} = 3.3V, 25^{\circ}C$ )

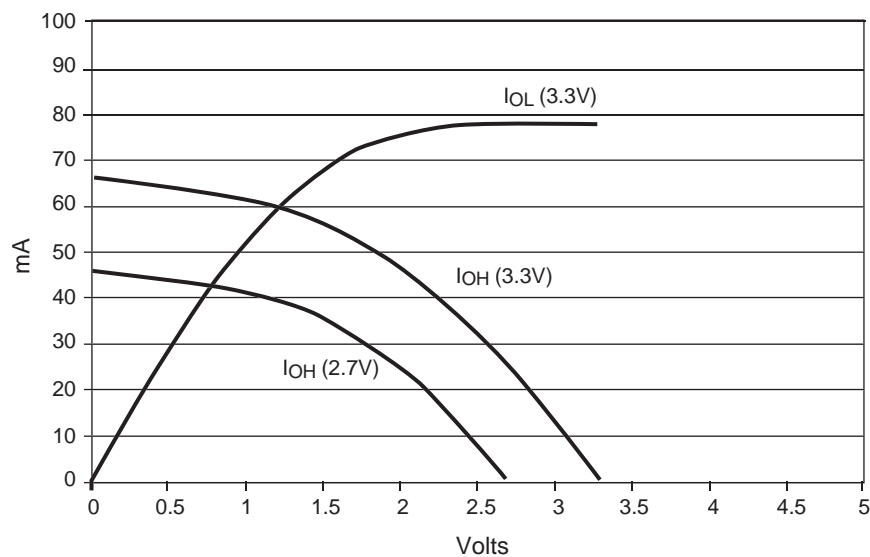
Frequency (MHz)	0	1	5	10	20	50	100	200
Typical $I_{CC}$ (mA)	0.017	0.13	0.54	1.06	2.09	5.2	10.26	20.3

## DC Electrical Characteristics Over Recommended Operating Conditions<sup>(1)</sup>

Symbol	Parameter	Test Conditions	Typical	Min.	Max.	Unit
$V_{OH}^{(2)}$	Output High voltage	$V_{CC} = 3.0V$ to $3.6V$ , $I_{OH} = -8$ mA	-	2.4	-	V
		$V_{CC} = 2.7V$ to $3.0V$ , $I_{OH} = -8$ mA	-	2.0	-	V
		$I_{OH} = -500$ $\mu A$	-	90% $V_{CC}^{(3)}$	-	V
$V_{OL}$	Output Low voltage	$I_{OL} = 8$ mA	-	-	0.4	V
$I_{IL}^{(4)}$	Input leakage current	$V_{IN} = GND$ or $V_{CC}$ to $5.5V$	-	-10	10	$\mu A$
$I_{IH}^{(4)}$	I/O High-Z leakage current	$V_{IN} = GND$ or $V_{CC}$ to $5.5V$	-	-10	10	$\mu A$
$I_{CCSB}^{(8)}$	Standby current	$V_{CC} = 3.6V$	24.5	-	100	$\mu A$
$I_{CC}$	Dynamic current <sup>(5,6)</sup>	$f = 1$ MHz	-	-	0.25	mA
		$f = 50$ MHz	-	-	7.5	mA
$C_{IN}$	Input pin capacitance <sup>(7)</sup>	$f = 1$ MHz	-	-	8	pF
$C_{CLK}$	Clock input capacitance <sup>(7)</sup>	$f = 1$ MHz	-	-	12	pF
$C_{I/O}$	I/O pin capacitance <sup>(7)</sup>	$f = 1$ MHz	-	-	10	pF

### Notes:

1. See the CoolRunner XPLA3 family data sheet ([DS012](#)) for recommended operating conditions
2. See [Figure 2](#) for output drive characteristics of the XPLA3 family.
3. This parameter guaranteed by design and characterization, not by testing.
4. Typical leakage current is less than  $1$   $\mu A$ .
5. See [Table 1](#), [Figure 1](#) for typical values.
6. This parameter measured with a 16-bit, resettable up/down counter loaded into every function block, with all outputs disabled and unloaded. Inputs are tied to  $V_{CC}$  or ground. This parameter guaranteed by design and characterization, not testing.
7. Typical values, not tested.
8. Typical value at  $70^{\circ} C$ .



DS012\_10\_031802

Figure 2: Typical IV Curve for the CoolRunner XPLA3 Family, 25°C

## AC Electrical Characteristics Over Recommended Operating Conditions<sup>(1,2)</sup>

Symbol	Parameter	-5		-7		-10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
T <sub>PD1</sub>	Propagation delay time (single p-term)		4.5	-	7.0	-	9.1	ns
T <sub>PD2</sub>	Propagation delay time (OR array) <sup>(3)</sup>		5.0	-	7.5	-	10.0	ns
T <sub>CO</sub>	Clock to output (global synchronous pin clock)		3.5		5.0	-	6.5	ns
T <sub>SUF</sub>	Setup time (fast input register)	2.5	-	3.0	-	3.0	-	ns
T <sub>SU1</sub> <sup>(4)</sup>	Setup time (single p-term)	3.0	-	4.3	-	5.4	-	ns
T <sub>SU2</sub>	Setup time (OR array)	3.5	-	4.8	-	6.3	-	ns
T <sub>H</sub> <sup>(4)</sup>	Hold time	0	-	0	-	0	-	ns
T <sub>WLH</sub> <sup>(4)</sup>	Global Clock pulse width (High or Low)	2.5	-	3.0	-	4.0	-	ns
T <sub>PLH</sub> <sup>(4)</sup>	P-term clock pulse width	4.0	-	5.0	-	6.0	-	ns
T <sub>APRPW</sub>	Asynchronous preset/reset pulse width (High or Low)	4.0	-	5.0	-	6.0	-	ns
T <sub>R</sub> <sup>(4)</sup>	Input rise time	-	20	-	20	-	20	ns
T <sub>L</sub> <sup>(4)</sup>	Input fall time	-	20	-	20	-	20	ns
f <sub>SYSTEM</sub> <sup>(4)</sup>	Maximum system frequency	-	213	-	119	-	95	MHz
T <sub>CONFIG</sub> <sup>(4)</sup>	Configuration time <sup>(5)</sup>	-	30	-	30	-	30	μs
T <sub>INIT</sub> <sup>(4)</sup>	ISP initialization time	-	30	-	30	-	30	μs
T <sub>POE</sub> <sup>(4)</sup>	P-term OE to output enabled	-	7.2	-	9.3	-	11.2	ns
T <sub>POD</sub> <sup>(4)</sup>	P-term OE to output disabled <sup>(6)</sup>	-	7.2	-	9.3	-	11.2	ns
T <sub>PCO</sub> <sup>(4)</sup>	P-term clock to output	-	6.0	-	8.3	-	10.7	ns
T <sub>PAO</sub> <sup>(4)</sup>	P-term set/reset to output valid	-	6.5	-	9.3	-	11.2	ns

### Notes:

1. Specifications measured with one output switching.
2. See CoolRunner XPLA3 family data sheet ([DS012](#)) for recommended operating conditions.
3. See [Figure 4](#) for derating.
4. These parameters guaranteed by design and/or characterization, not testing.
5. Typical current draw during configuration is 3 mA at 3.6V.
6. Output C<sub>L</sub> = 5 pF.

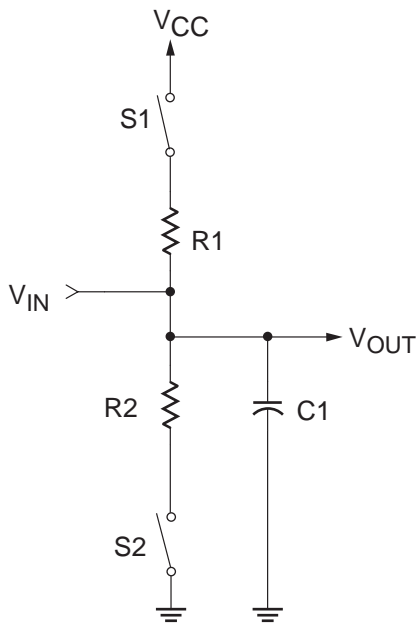
## Internal Timing Parameters<sup>(1,2)</sup>

Symbol	Parameter	-5		-7		-10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Buffer Delays</b>								
T <sub>IN</sub>	Input buffer delay	-	0.7	-	1.6	-	2.2	ns
T <sub>FIN</sub>	Fast Input buffer delay	-	2.2	-	3.0	-	3.1	ns
T <sub>GCK</sub>	Global Clock buffer delay	-	0.7	-	1.0	-	1.3	ns
T <sub>OUT</sub>	Output buffer delay	-	1.8	-	2.7	-	3.6	ns
T <sub>EN</sub>	Output buffer enable/disable delay	-	4.5	-	5.0	-	5.7	ns
<b>Internal Register, Product Term, and Combinatorial Delays</b>								
T <sub>LDI</sub>	Latch transparent delay	-	1.3	-	1.6	-	2.0	ns
T <sub>SUI</sub>	Register setup time	1.0	-	1.0	-	1.2	-	ns
T <sub>HI</sub>	Register hold time	0.3	-	0.5	-	0.7	-	ns
T <sub>ECSU</sub>	Register clock enable setup time	2.0	-	2.5	-	3.0	-	ns
T <sub>ECHO</sub>	Register clock enable hold time	3.0	-	4.5	-	5.5	-	ns
T <sub>COI</sub>	Register clock to output delay	-	1.0	-	1.3	-	1.6	ns
T <sub>AOI</sub>	Register async. S/R to output delay	-	2.0	-	2.3	-	2.1	ns
T <sub>RAI</sub>	Register async. recovery	-	3.5	-	5.0	-	6.0	ns
T <sub>PTCK</sub>	Product term clock delay	-	2.5	-	2.7	-	3.3	ns
T <sub>LOGI1</sub>	Internal logic delay (single p-term)	-	2.0	-	2.7	-	3.3	ns
T <sub>LOGI2</sub>	Internal logic delay (PLA OR term)	-	2.5	-	3.2	-	4.2	ns
<b>Feedback Delays</b>								
T <sub>F</sub>	ZIA delay	-	0.2	-	2.9	-	3.5	ns
<b>Time Adders</b>								
T <sub>LOGI3</sub>	Fold-back NAND delay	-	2.0	-	2.5	-	3.0	ns
T <sub>UDA</sub>	Universal delay	-	1.2	-	2.0	-	2.5	ns
T <sub>SLEW</sub>	Slew rate limited delay	-	4.0	-	5.0	-	6.0	ns

### Notes:

1. These parameters guaranteed by design and characterization, not testing.
2. See the CoolRunner XPLA3 family data sheet ([DS012](#)) for timing model.

## Switching Characteristics



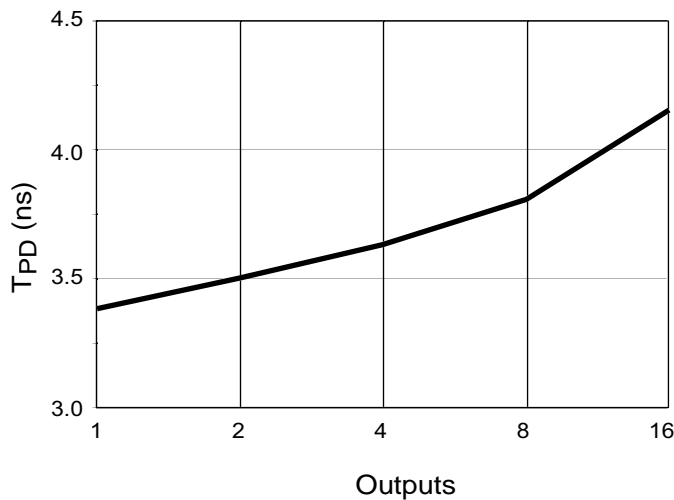
Component	Values
R1	390Ω
R2	390Ω
C1	35 pF

Measurement	S1	S2
T <sub>POE</sub> (High)	Open	Closed
T <sub>POE</sub> (Low)	Closed	Open
T <sub>P</sub>	Closed	Closed

**Note:** For T<sub>POD</sub>, C1 = 5 pF. Delay measured at output level of V<sub>OL</sub> + 300 mV, V<sub>OH</sub> - 300 mV.

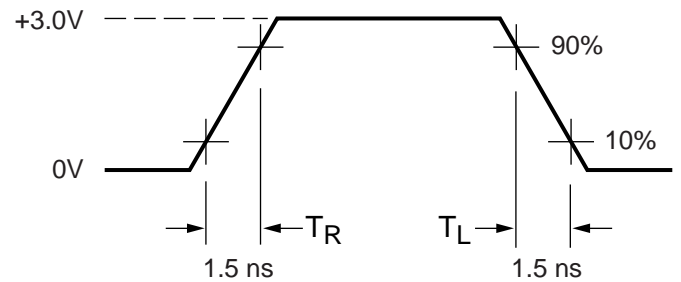
DS023\_03\_102401

Figure 3: AC Load Circuit



DS023\_05\_061101

Figure 4: Derating Curve for T<sub>PD2</sub>



**Measurements:**

All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

DS023\_06\_042800

Figure 5: Voltage Waveform

## Pin Descriptions

Table 2: XCR3032XL User I/O Pins

	PC44	VQ44	CS48
Total User I/O Pins	36	36	36

Table 3: XCR3032XL I/O Pins

Function Block	Macrocell	PC44	VQ44	CS48
1	1	4	42	A2
1	2	5	43	A1
1	3	6	44	C4
1	4	7 <sup>(1)</sup>	1 <sup>(1)</sup>	B1 <sup>(1)</sup>
1	5	8	2	C2
1	6	9	3	C1
1	7	11	5	D3
1	8	12	6	D1
1	9	13 <sup>(1)</sup>	7 <sup>(1)</sup>	D2 <sup>(1)</sup>
1	10	14	8	E1
1	11	16	10	F1
1	12	17	11	G1
1	13	18	12	E4
1	14	19	13	F2
1	15	20	14	G2
1	16	21	15	F3
2	1	41	35	C5
2	2	40	34	A6
2	3	39	33	B6
2	4	38 <sup>(1)</sup>	32 <sup>(1)</sup>	B7 <sup>(1)</sup>
2	5	37	31	D4
2	6	36	30	C6
2	7	34	28	D6
2	8	33	27	D7
2	9	32 <sup>(1)</sup>	26 <sup>(1)</sup>	E5 <sup>(1)</sup>
2	10	31	25	E7
2	11	29	23	F7
2	12	28	22	G7
2	13	27	21	G6
2	14	26	20	F5

Table 3: XCR3032XL I/O Pins

Function Block	Macrocell	PC44	VQ44	CS48
2	15	25	19	G5
2	16	24	18	F4

**Notes:**

- JTAG pins

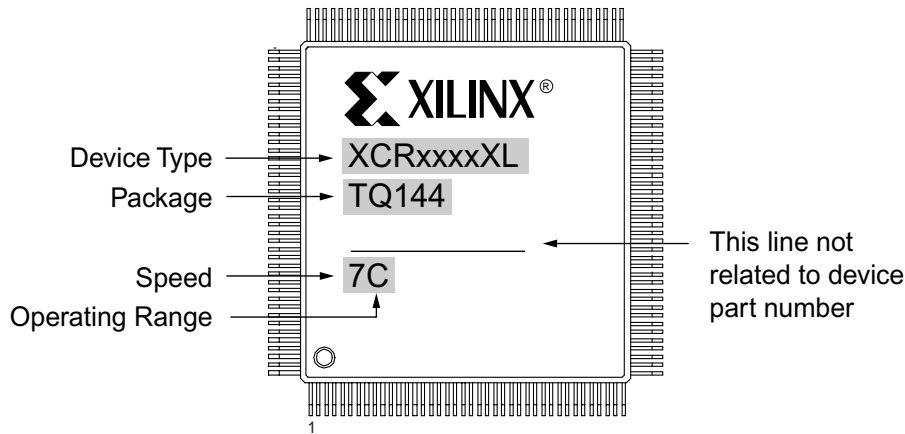
Table 4: XCR3032XL Global, JTAG, Port Enable, Power, and No Connect Pins

Pin Type	PC44	VQ44	CS48
IN0 / CLK0	2	40	A3
IN1 / CLK1	1	39	B4
IN2 / CLK2	44	38	A4
IN3 / CLK3	43	37	B5
TCK	32	26	E5
TDI	7	1	B1
TDO	38	32	B7
TMS	13	7	D2
PORT_EN	10 <sup>(1)</sup>	4 <sup>(1)</sup>	C3 <sup>(1)</sup>
V <sub>CC</sub>	3, 15, 23, 35	9, 17, 29, 41	B3, C7, E2, G4
GND	22, 30, 42	16, 24, 36	A5, E3, E6
No Connects	-	-	A7, B2, F6, G3

**Notes:**

- Port Enable is brought High to enable JTAG pins when JTAG pins are used as I/O. See family data sheet ([DS012](#)) for full explanation.

## Device Part Marking



Sample package with part marking.

**Notes:**

- Due to the small size of chip scale packages, part marking on these packages does not follow the above sample and the complete part number cannot be included in the marking. Part marking on chip scale packages by line:
  - Line 1 = X (Xilinx logo), then truncated part number (no XC), i.e., 3064XL.
  - Line 2 = Not related to device part number.
  - Line 3 = Not related to device part number.
  - Line 4 = Package code, speed, operating temperature, three digits not related to device part number. Package codes; C1 = CS48, C2 = CSG48.

## Ordering Combination Information

Device Ordering and Part Marking Number <sup>(2)</sup>	Speed (pin-to-pin delay)	Pkg. Symbol	No. of Pins	Package Type	Operating Range <sup>(1)</sup>
XCR3032XL-5PC44C	5 ns	PC44	44	Plastic Leaded Chip Carrier (PLCC)	C
XCR3032XL-5VQ44C	5 ns	VQ44	44	Very Thin Quad Flat Pack (VQFP)	C
XCR3032XL-5CS48C	5 ns	CS48	48	Chip Scale Package (CSP)	C
XCR3032XL-7PC44C	7.5 ns	PC44	44	Plastic Leaded Chip Carrier (PLCC)	C
XCR3032XL-7VQ44C	7.5 ns	VQ44	44	Very Thin Quad Flat Pack (VQFP)	C
XCR3032XL-7CS48C	7.5 ns	CS48	48	Chip Scale Package (CSP)	C
XCR3032XL-7PC44I	7.5 ns	PC44	44	Plastic Leaded Chip Carrier (PLCC)	I
XCR3032XL-7VQ44I	7.5 ns	VQ44	44	Very Thin Quad Flat Pack (VQFP)	I
XCR3032XL-7CS48I	7.5 ns	CS48	48	Chip Scale Package (CSP)	I
XCR3032XL-10PC44C	10 ns	PC44	44	Plastic Leaded Chip Carrier (PLCC)	C
XCR3032XL-10VQ44C	10 ns	VQ44	44	Very Thin Quad Flat Pack (VQFP)	C
XCR3032XL-10CS48C	10 ns	CS48	48	Chip Scale Package (CSP)	C
XCR3032XL-10PC44I	10 ns	PC44	44	Plastic Leaded Chip Carrier (PLCC)	I
XCR3032XL-10VQ44I	10 ns	VQ44	44	Very Thin Quad Flat Pack (VQFP)	I
XCR3032XL-10CS48I	10 ns	CS48	48	Chip Scale Package (CSP)	I

**Notes:**

- C = Commercial:  $T_A = 0^\circ$  to  $+70^\circ\text{C}$ ; I = Industrial:  $T_A = -40^\circ$  to  $+85^\circ\text{C}$
- Some packages available in Pb-free option. See [Xilinx Packaging](#) for more information.

## Additional Information

[CoolRunner XPLA3 Data Sheets and Application Notes](#)    [Device Package User Guide](#)

[Device Packages](#)

## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/18/00	1.0	Initial Xilinx release.
02/05/01	1.1	Removed Timing Model.
04/11/01	1.2	Update TSUF spec to meet UMC characterization data. Added I <sub>CC</sub> vs. Freq. numbers, <a href="#">Table 1</a> and updated <a href="#">Figure 1</a> . Added Typical I/V curve, <a href="#">Figure 2</a> ; added <a href="#">Table 2</a> : Total User I/O; changed V <sub>OH</sub> spec.
04/19/01	1.3	Updated Typical I/V curve, <a href="#">Figure 2</a> : added voltage levels.
08/27/01	1.4	Changed from Advance to Preliminary; updated DC Electrical Characteristics; AC Electrical Characteristics; Internal Timing Parameters; added Derating Curve; added -10 industrial packages. Added 200 MHz to <a href="#">Figure 1</a> and <a href="#">Table 1</a> . changed -5 F <sub>SYSTEM</sub> to 200 MHz, -5 T <sub>F</sub> to 0.5 ns.
01/08/02	1.5	Updated T <sub>HI</sub> spec to correct a typo. Added single p-term setup time (T <sub>SU1</sub> ) to AC Table, renamed T <sub>SU</sub> to T <sub>SU2</sub> for setup time through the OR array. Updated AC Load Circuit diagram to more closely resemble true test conditions, added note for T <sub>POD</sub> delay measurement. Updated note 5 in AC Characteristics table lowering typical current draw during configuration.
01/06/03	1.6	Added voltage and temperature to <a href="#">Figure 2</a> . Increased -5 T <sub>PCO</sub> to 6.0 (from 5.5 ns) by adding T <sub>PTCK</sub> parameter to internal timing model. Increased -5 F <sub>MAX</sub> . Updated Ordering Information format.
07/15/03	1.7	Updated Device Part Marking. Updated test conditions for I <sub>IL</sub> and I <sub>IH</sub> .
08/21/03	1.8	Updated Package Device Marking Pin 1 orientation.
02/13/04	1.9	Add solder temperature specification. Add links to data sheets, application notes and packages.
04/08/05	2.0	Added I <sub>CCSB</sub> Typical and T <sub>APRPW</sub> specifications. Removed T <sub>SOL</sub> specification. Added note about Pb-free packages.