

## 500-kHz Half-Bridge DC/DC Controller With Integrated Secondary Synchronous Rectification Drivers

### FEATURES

- 28-V to 75-V Input Voltage Range
- Compatible with ETSI 300 132-2
- Integrated  $\pm 1$ -A Half Bridge Primary Drivers
- Secondary Synchronous Rectifier Control Signals With Programmable Deadtime Delay
- Voltage Mode Control
- Voltage Feedforward Compensation
- High Voltage Pre-Regulator Operates During Start-Up
- Current Sensing On Low-Side Primary Device



- Frequency Foldback Eliminates Constant Current Tail
- Advanced Maximum Current Control During Start-Up and Shorted Load
- Low Input Voltage Detection
- Programmable Soft-Start Function
- Over Temperature Protection

### APPLICATIONS

- Network Cards
- Power Supply Modules

### DESCRIPTION

Si9122A is a half-bridge controller IC ideally suited to fixed telecom applications where high efficiency is required at low output voltages (e.g. <math><3.3\text{ V}</math>). Designed to operate within the fixed telecom voltage range of 33–75 V and withstand 100 V, 100 ms transients, the IC is capable of controlling and driving both the low and high-side switching devices of a half bridge circuit and also controlling the switching devices on the secondary side of the bridge. Due to the very low on-resistance of the secondary MOSFETs, a significant increase in conversion efficiency can be achieved as compared with conventional Schottky diodes. Control of the secondary devices is by means of a pulse transformer and a pair of inverters. Such a system has efficiencies well in excess of 90%

even for low output voltages. On-chip control of the dead time delays between the primary and secondary synchronous signals keep efficiencies high and prevent accidental destruction of the power transformer. An external resistor sets the switching frequency from 200 kHz to 625 kHz.

Si9122A has advanced current monitoring and control circuitry which allow the user to set the maximum current in the primary circuit. Such a feature acts as protection against output shorting and also provides constant current into large capacitive loads during start-up or when paralleling power supplies. Current sensing is by means of a sense resistor on the low-side primary device.

### FUNCTIONAL BLOCK DIAGRAM

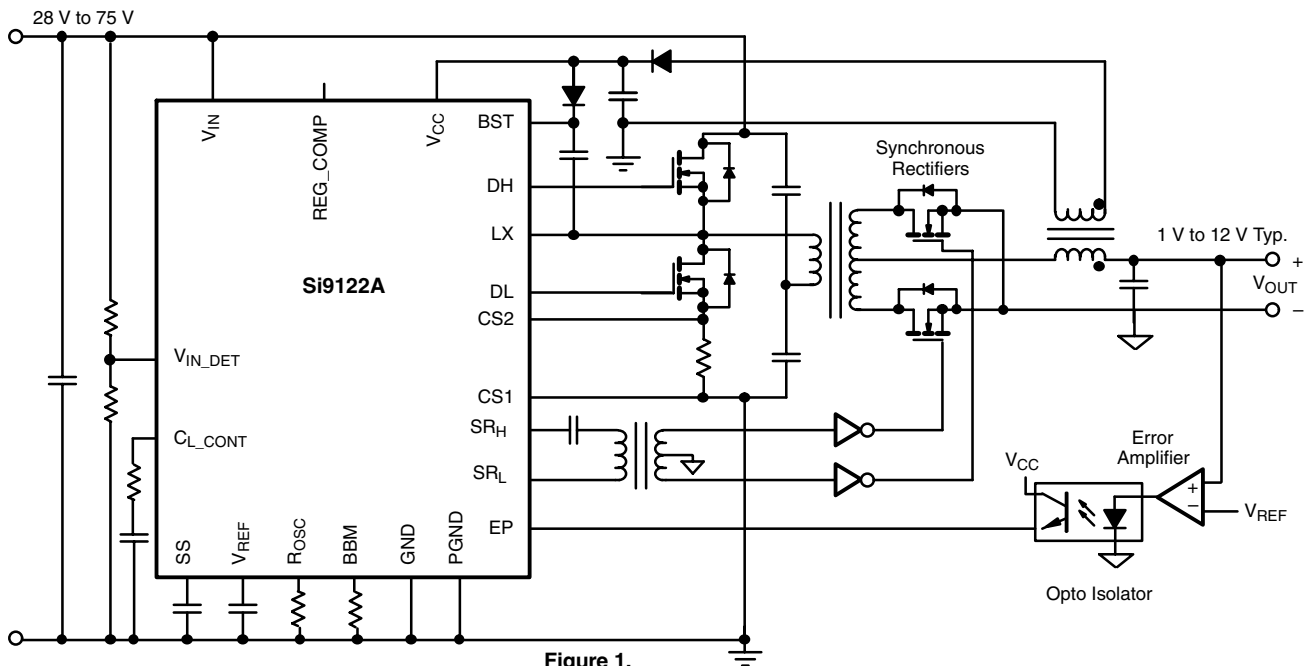


Figure 1.

**TECHNICAL DESCRIPTION**

Si9122A is a voltage mode controller for the half-bridge topology. With 100-V depletion mode MOSFET capability, the Si9122A is capable of powering directly from the high voltage bus to  $V_{CC}$  through an external PNP pass transistor, or may be powered through an external regulator directly through the  $V_{CC}$  pin. With PWM control, Si9122A provides peak efficiency throughout the entire line and load range. In order to simplify the design of efficient secondary synchronous rectification circuitry, Si9122A provides intelligent gate drive signals to control the secondary MOSFETs. With independent gate drive signals from the controller, transformer design is no longer limited by the gate to source rating of the secondary-side MOSFETs. Si9122A provides constant  $V_{GS}$  voltage, independent of line voltage to minimize the gate charge loss as well as conduction loss. A break-before-make function is

included to prevent shoot through current or transformer shorting. Adjustable Break-Before-Make time is incorporated into the IC and is programmable by an external resistor value.

Si9122A is packaged in lead (Pb)-free [TSSOP-20](#) and [MLP65-20](#) packages. To satisfy stringent ambient temperature requirements, Si9122A is rated to handle the industrial temperature range of  $-40$  to  $85^{\circ}\text{C}$ . When a situation arises which results in a rapid increase in primary (or secondary current) such as output shorted or start-up with a large output capacitor, control of the PWM generator is handed over to the current loop. Monitoring of the load current is by means of an external current sense resistor in the source of the primary low-side switch.

**SI9122 BLOCK DIAGRAM**

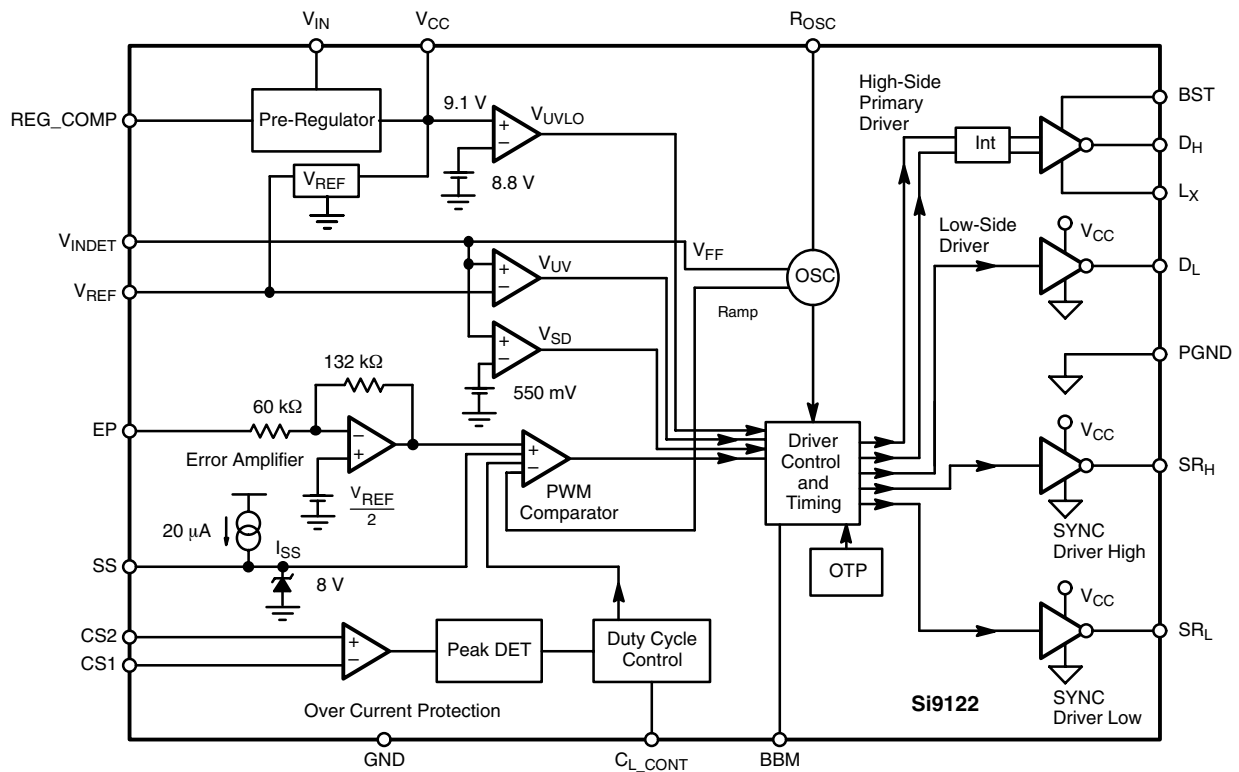


Figure 2.



**ABSOLUTE MAXIMUM RATINGS (ALL VOLTAGES REFERENCED TO GND = 0 V)**

$V_{IN}$ (Continuous) .....	80 V	Storage Temperature .....	-65 to 150°C
$V_{IN}$ (100 ms) .....	100 V	Operating Junction Temperature .....	125°C
$V_{CC}$ .....	14.5 V	Power Dissipation <sup>a</sup>	
$V_{BST}$ (Continuous) .....	95 V	TSSOP-20 <sup>b</sup> .....	850 mW
(100 ms) .....	113.2 V	MLP65-20 <sup>c</sup> .....	2500 mW
$V_{LX}$ .....	100 V	Thermal Impedance ( $\theta_{JA}$ )	
$V_{BST} - V_{LX}$ .....	15 V	TSSOP-20 .....	75°C/W
$V_{REF}, R_{OSC}$ .....	-0.3 V to $V_{CC} + 0.3$ V	MLP65-20 .....	38°C/W
Logic Inputs .....	-0.3 V to $V_{CC} + 0.3$ V	Notes	
Analog Inputs .....	-0.3 V to $V_{CC} + 0.3$ V	a. Device mounted on JEDEC compliant 1S2P test board..	
HV Pre-Regulator Input Current (continuous) .....	5 mA	b. Derate -14 mW/°C above 25°C.	
		c. Derate -26 mW/°C above 25°C.	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING RANGE (ALL VOLTAGES REFERENCED TO GND = 0 V)**

$V_{IN}$ .....	28 to 75 V	$R_{BBM}$ .....	22 to 50 k $\Omega$
$V_{CC}$ Operating .....	10.5 to 13.2 V	$C_{REF}$ .....	0.1 $\mu$ F
$C_{VCC}$ .....	$\geq 4.7$ $\mu$ F	$C_{BOOST}$ .....	0.1 $\mu$ F
$f_{OSC}$ .....	200 to 625 kHz	Analog Inputs .....	0 to $V_{CC} - 2$ V
$R_{OSC}$ .....	22.6 to 72 k $\Omega$	Digital Inputs .....	0 to $V_{CC}$
		Reference Voltage Output Current .....	0 to 2.5 mA

**SPECIFICATIONS<sup>a</sup>**

Parameter	Symbol	Test Conditions Unless Otherwise Specified $f_{NOM} = 500$ kHz, $V_{IN} = 75$ V $V_{INDET} = 7.5$ V; $10.5$ V $\leq V_{CC} \leq 13.2$ V	Limits -40 to 85°C			Unit
			Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
<b>Reference (3.3 V)</b>						
Output Voltage	$V_{REF}$	$V_{CC} = 12$ V, 25°C Load = 0 mA	3.2	3.3	3.4	V
Short Circuit Current	$I_{SREF}$	$V_{REF} = 0$ V			-50	mA
Load Regulation	$dVr/dlr$	$I_{REF} = 0$ to -2.5 mA		-30	-75	mV
Power Supply Rejection	PSRR	@ 100Hz		60		dB
<b>Oscillator</b>						
Accuracy (1% $R_{OSC}$ )		$R_{OSC} = 30$ k $\Omega$ , $f_{NOM} = 500$ kHz	-20		20	%
Max Frequency <sup>h</sup>	$F_{MAX}$	$R_{OSC} = 22.6$ k $\Omega$	500	625	750	kHz
Foldback Frequency <sup>d</sup>	$F_{FOBK}$	$f_{NOM} = 500$ kHz, $V_{CS2} - V_{CS1} > 150$ mV		100		
<b>Error Amplifier</b>						
Input Bias Current	$I_{BIAS}$	$V_{EP} = 0$ V	-40		-15	$\mu$ A
Gain	$A_V$			-2.2		V/V
Bandwidth	BW			5		MHz
Power Supply Rejection	PSRR	@ 100Hz		60		dB
Slew Rate	SR			0.5		V/ $\mu$ s
<b>Current Sense Amplifier</b>						
Input Voltage CM Range	$V_{CM}$	$V_{CS1} - GND, V_{CS2} - GND$		$\pm 150$		mV
Input Amplifier Gain	$A_{VOL}$			17.5		dB
Input Amplifier Bandwidth	BW			5		MHz
Input amplifier Offset Voltage	$V_{OS}$			$\pm 5$		mV

SPECIFICATIONS <sup>a</sup>						
Parameter	Symbol	Test Conditions Unless Otherwise Specified $f_{NOM} = 500 \text{ kHz}$ , $V_{IN} = 75 \text{ V}$ $V_{INDET} = 7.5 \text{ V}$ ; $10.5 \text{ V} \leq V_{CC} \leq 13.2 \text{ V}$	Limits –40 to 85°C			Unit
			Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
<b>Current Sense Amplifier</b>						
CL_CONT Current	I <sub>CL_CONT</sub>	dV <sub>CS</sub> = 0		120		μA
		dV <sub>CS</sub> = 100 mV		0		
		dV <sub>CS</sub> = 170 mV		>2		mA
Lower Current Limit Threshold	V <sub>TLCL</sub>	I <sub>PD</sub> = I <sub>PU</sub> – I <sub>CL_CONT</sub> = 0 <a href="#">See Figure 6</a>		100		mV
Upper Current Limit Threshold	V <sub>THCL</sub>	I <sub>PD</sub> > 2 mA		150		
Hysteresis		I <sub>PU</sub> < 500 μA		–50		
CL_CONT Clamp Level	CL_CONT(min)	I <sub>PU</sub> = 500 μA	0.6		1.5	V
<b>PWM Operation</b>						
Duty Cycle <sup>e</sup>	D <sub>MAX</sub>	f <sub>OSC</sub> = 500 kHz V <sub>EP</sub> = 0 V V <sub>EP</sub> = 1.75 V	90	92	95	%
	D <sub>MIN</sub>		V <sub>CS2</sub> – V <sub>CS1</sub> > 150 mV		<15	
<b>Pre-Regulator</b>						
Input Voltage	+V <sub>IN</sub>	I <sub>IN</sub> = 10 μA	28		75	V
Input Leakage Current	I <sub>LKG</sub>	V <sub>IN</sub> = 75 V, V <sub>CC</sub> > V <sub>REG</sub>			10	μA
Regulator Bias Current	I <sub>REG1</sub>	V <sub>IN</sub> = 75 V, V <sub>INDET</sub> < V <sub>SD</sub>		86	200	
	I <sub>REG2</sub>	V <sub>IN</sub> = 75 V, V <sub>INDET</sub> > V <sub>REF</sub>		8	14	mA
Regulator_Comp	I <sub>SOURCE</sub>	V <sub>CC</sub> = 12 V	–29	–19	–9	μA
	I <sub>SINK</sub>		50	82	110	
Pre-Regulator Drive Capacity	I <sub>START</sub>	V <sub>CC</sub> < V <sub>REG</sub>	20			mA
V <sub>CC</sub> Pre-Regulator Turn Off Threshold Voltage	V <sub>REG1</sub>	V <sub>INDET</sub> > V <sub>REF</sub>	7.4	9.1	10.4	V
		T <sub>A</sub> = 25°C	8.5	9.1	9.7	
	V <sub>REG2</sub>	V <sub>INDET</sub> = 0 V		9.2		
Undervoltage Lockout	V <sub>UVLO</sub>	V <sub>CC</sub> Rising	7.15	8.8	9.8	
		T <sub>A</sub> = 25°C	8.1	8.8	9.3	
V <sub>UVLO</sub> Hysteresis <sup>g</sup>	V <sub>UVLOHYS</sub>			0.5		
<b>Soft-Start</b>						
Soft-Start Current Output	I <sub>SS</sub>	Start-Up Condition	12	20	28	μA
Soft-Start Completion Voltage	V <sub>SS_COMP</sub>	Normal Operation	7.35	8.05	8.85	V
<b>Shutdown</b>						
V <sub>INDET</sub> Shutdown	V <sub>SD</sub>	V <sub>INDET</sub> Rising	350	550	720	mV
V <sub>SD</sub> Hysteresis		V <sub>INDET</sub>		200		
<b>V<sub>INDET</sub> Input Threshold Voltages</b>						
V <sub>INDET</sub> – V <sub>IN</sub> Under Voltage	V <sub>UV</sub>	V <sub>INDET</sub> Rising	3.13	3.3	3.46	V
V <sub>UV</sub> Hysteresis		V <sub>INDET</sub>		0.3		
<b>Over Temperature Protection</b>						
Activating Temperature		T <sub>J</sub> Increasing		160		°C
De-Activating Temperature		T <sub>J</sub> Decreasing		130		
<b>Converter Supply Current (V<sub>CC</sub>)</b>						
Shutdown	I <sub>CC1</sub>	Shutdown, V <sub>INDET</sub> = 0 V	50		350	μA
Switching Disabled	I <sub>CC2</sub>	V <sub>INDET</sub> < V <sub>REF</sub>	4	8	12	mA
Switching w/o Load	I <sub>CC3</sub>	V <sub>INDET</sub> > V <sub>REF</sub> , f <sub>NOM</sub> = 500 kHz	5	10	15	
Switching with C <sub>LOAD</sub>	I <sub>CC4</sub>	V <sub>CC</sub> = 12 V, C <sub>DH</sub> = C <sub>DL</sub> = 3 nF C <sub>SRH</sub> = C <sub>SRL</sub> = 0.3 nF		21		



<b>SPECIFICATIONS<sup>a</sup></b>						
Parameter	Symbol	Test Conditions Unless Otherwise Specified $f_{NOM} = 500 \text{ kHz}$ , $V_{IN} = 75 \text{ V}$ $V_{INDET} = 7.5 \text{ V}$ ; $10.5 \text{ V} \leq V_{CC} \leq 13.2 \text{ V}$	Limits -40 to 85°C			Unit
			Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
<b>Output MOSFET DH Driver (High-Side)</b>						
Output High Voltage	$V_{OH}$	Sourcing 10 mA	$V_{BST} - 0.3$			V
Output Low Voltage	$V_{OL}$	Sinking 10 mA			$V_{LX} + 0.3$	
Boost Current	$I_{BST}$	$V_{LX} = 75 \text{ V}$ , $V_{BST} = V_{LX} + V_{CC}$	1.3	1.9	2.7	mA
$L_X$ Current	$I_{LX}$	$V_{LX} = 75 \text{ V}$ , $V_{BST} = V_{LX} + V_{CC}$	-1.1	-0.7	-0.4	
Peak Output Source	$I_{SOURCE}$	$V_{CC} = 10.5 \text{ V}$		-1.0	-0.75	A
Peak Output Sink	$I_{SINK}$		0.75	1.0		
Rise Time	$t_r$	$C_{DH} = 3 \text{ nF}$		35		ns
Fall Time	$t_f$			35		
<b>Output MOSFET DLDriver (Low-Side)</b>						
Output High Voltage	$V_{OH}$	Sourcing 10 mA	$V_{CC} - 0.3$			V
Output Low Voltage	$V_{OL}$	Sinking 10 mA			0.3	
Peak Output Source	$I_{SOURCE}$	$V_{CC} = 10.5 \text{ V}$		-1.0	-0.75	A
Peak Output Sink	$I_{SINK}$		0.75	1.0		
Rise Time	$t_r$	$C_{DL} = 3 \text{ nF}$		35		ns
Fall Time	$t_f$			35		
<b>Synchronous Rectifier (SRH, SRL) Drivers</b>						
Output High Voltage	$V_{OH}$	Sourcing 10 mA	$V_{CC} - 0.4$			V
Output Low Voltage	$V_{OL}$	Sinking 10 mA			0.4	
Break-Before-Make Time <sup>f</sup>	$t_{BBM1}$	$T_A = 25^\circ\text{C}$ , $R_{BBM} = 33 \text{ k}\Omega$ , <a href="#">See Figure 3</a>		55		ns
	$t_{BBM2}$			40		
	$t_{BBM3}$	$T_A = 25^\circ\text{C}$ , $R_{BBM} = 33 \text{ k}\Omega$ , $L_X = 75 \text{ V}$		35		
	$t_{BBM4}$			55		
Peak Output Source	$I_{SOURCE}$	$V_{CC} = 10.5 \text{ V}$		-100		mA
Peak Output Sink	$I_{SINK}$			100		
Rise Time	$t_r$	$C_{SRH} = C_{SRL} = 0.3 \text{ nF}$		35		ns
Fall Time	$t_f$			35		
<b>Voltage Mode</b>						
Error Amplifier	$t_{d1DH}$ $t_{d2DL}$	Input to high-side switch off		< 200		ns
		Input to low-side switch off		< 200		
<b>Current Mode</b>						
Current Amplifier	$t_{d3DH}$ $t_{d4DL}$	Input to high-side switch off		< 200		ns
		Input to low-side switch off		< 200		

**Notes**

- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum (-40° to 85°C).
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- $F_{MIN}$  when  $V_{CL\_CONT}$  at clamp level. Typical foldback frequency change +20%, -30% over temperature.
- Measured on SRL or SRH outputs.
- See Figure 3 for Break-Before-Make time definition.
- $V_{UVLO}$  tracks  $V_{REG1}$  by a diode drop
- Guaranteed by design and characterization, not tested in production.

**TIMING DIAGRAM FOR MOS DRIVERS**

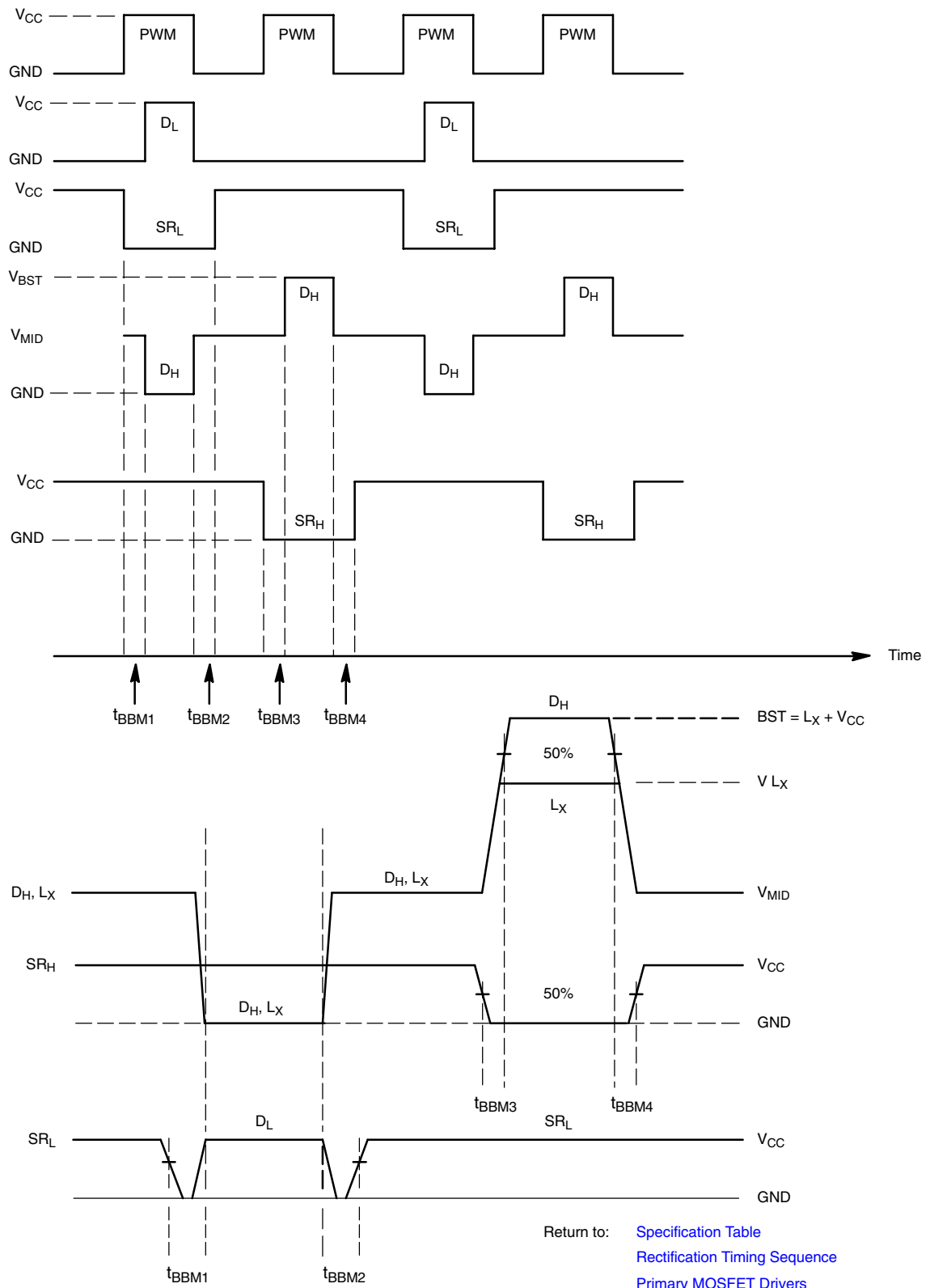
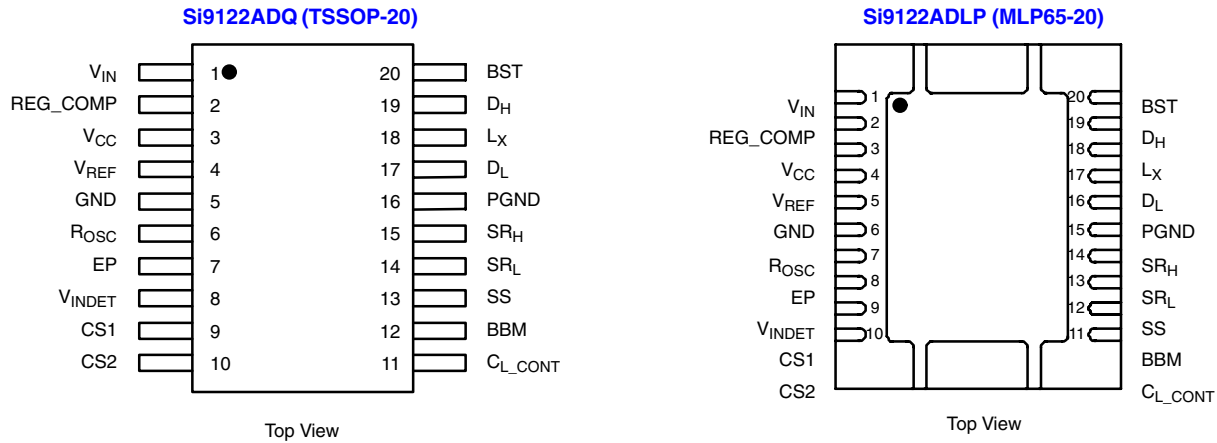


Figure 3.

## PIN CONFIGURATION



## ORDERING INFORMATION

Part Number	Temperature Range	Package
Si9122ADQ-T1-E3	-40 to 85°C	TSSOP-20
Si9122ADLP-T1-E3		MLP65-20

Eval Board	Temperature Range	Board Type
Contact Factory	-10 to 70°C	Surface Mount and Thru-Hole

## PIN DESCRIPTION

Pin Number	Name	Function
1	$V_{IN}$	Input supply voltage for the start-up circuit.
2	REG_COMP	Control signal for an external pass transistor.
3	$V_{CC}$	Supply voltage for internal circuitry
4	$V_{REF}$	3.3-V reference
5	GND	Ground
6	R <sub>OSC</sub>	External resistor connection to oscillator
7	EP	Voltage control input
8	$V_{INDET}$	$V_{IN}$ under voltage detect and shutdown function input. Shuts down or disables switching when $V_{INDET}$ falls below preset threshold voltages and provides the feed forward voltage.
9	CS1	Current limit amplifier negative input
10	CS2	Current limit amplifier positive input
11	C <sub>L_CONT</sub>	Current limit compensation
12	BBM	Programmable Break-Before-Make time connection to an external resistor to set time delay
13	SS	Soft-Start control – external capacitor connection
14	SR <sub>L</sub>	Signal transformer drive, sequenced with the primary side.
15	SR <sub>H</sub>	Signal transformer drive, sequenced with the primary side.
16	PGND	Power ground.
17	D <sub>L</sub>	Low-side gate drive signal – primary
18	L <sub>X</sub>	High-side source and transformer connection node
19	D <sub>H</sub>	High-side gate drive signal – primary
20	BST	Bootstrap voltage to drive the high-side n-channel MOSFET switch

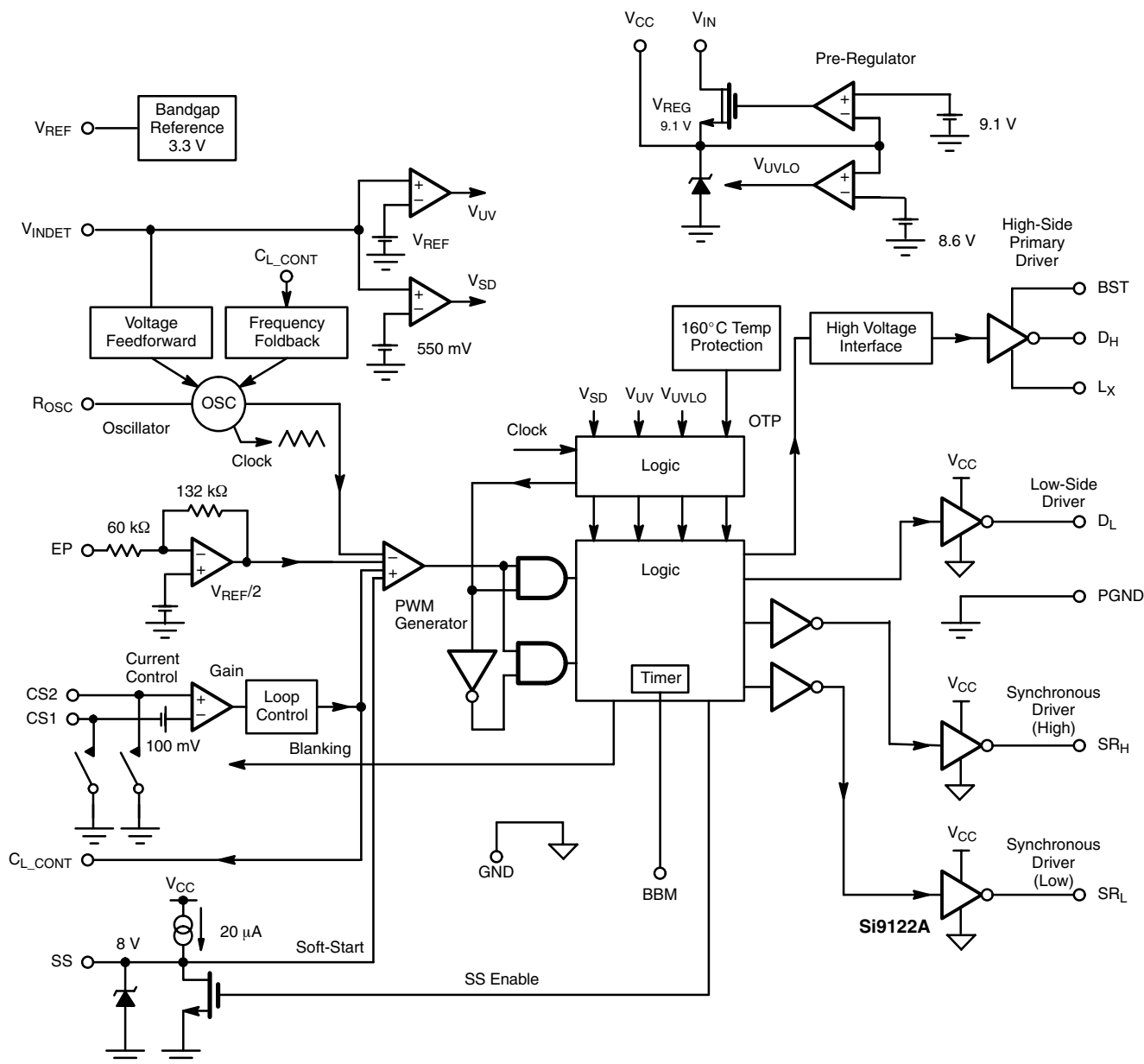


Figure 4. Detailed Si9122A Block Diagram

## DETAILED OPERATION

### Start-Up

When  $V_{INEXT}$  rises above 0 V, the internal pre-regulator begins to charge up the  $V_{CC}$  capacitor. Current into the external  $V_{CC}$  capacitor is limited to typically 40 mA by the internal DMOS device. When  $V_{CC}$  exceeds the UVLO voltage of 8.8 V a soft-start cycle of the switch mode supply is initiated. The  $V_{CC}$  supply continues to be charged by the pre-regulator until  $V_{CC}$  equals  $V_{REG}$ . During this period, between  $V_{UVLO}$  and  $V_{REG}$ , excessive load current will result in  $V_{CC}$  falling below  $V_{UVLO}$  and stopping switch mode operation. This situation is avoided by the hysteresis between  $V_{REG}$  and  $V_{UVLO}$  and correct sizing

of the  $V_{CC}$  capacitor, bootstrap capacitor and the soft-start capacitor. The value of the  $V_{CC}$  capacitor should therefore be chosen to be capable of maintaining switch mode operation until the required  $V_{CC}$  current can be supplied from the external circuit (e.g via a power transformer winding and zener regulator). Feedback from the output of the switch mode supply charges  $V_{CC}$  above  $V_{REG}$  and fully disconnects the pre-regulator, isolating  $V_{CC}$  from  $V_{IN}$ .  $V_{CC}$  is then maintained above  $V_{REG}$  for the duration of switch mode operation. In the event of an over voltage condition on  $V_{CC}$ , an internal voltage clamp turns on at 14.5 V to shunt excessive current to GND.



Care needs to be taken if there is a delay prior to the external circuit feeding back to the  $V_{CC}$  supply. To prevent excessive power dissipation within the IC it is advisable to use an external PNP device. A pin has been incorporated on the IC, (REG\_COMP) to provide compensation when employing the external device. In this case the  $V_{IN}$  pin is connected to the base of the PNP device and controls the current, while the REG\_COMP pin determines the frequency compensation of the circuit. To understand the operation please refer to [Figure 5](#).

The soft-start circuit is designed for the dc-dc converter to start-up in an orderly manner and reduce component stress on the IC. This feature is programmable by selecting an external  $C_{SS}$ . An internal 20- $\mu$ A current source charges  $C_{SS}$  from 0 V to the final clamped voltage of 8 V. In the event of UVLO or shutdown,  $V_{SS}$  will be held low (<1 V) disabling driver switching. To prevent oscillations, a longer soft-start time may be needed for highly capacitive loads and/or high peak output current applications.

#### Reference

The reference voltage of Si9122A is set at 3.3 V. The reference voltage should be de-coupled externally with 0.1- $\mu$ F capacitor. The  $V_{REF}$  voltage is 0 V in shutdown mode and has 50-mA source capability.

#### Voltage Mode PWM Operation

Under normal load conditions, the IC operates in voltage mode and generates a fixed frequency pulse width modulated signal to the drivers. Duty cycle is controlled over a wide range to maintain output voltage under line and load variation. Voltage feed forward is also included to take account of variations in supply voltage  $V_{IN}$ .

In the half-bridge topology requiring isolation between output and input, the reference voltage and error amplifier must be supplied externally, usually on the secondary side. The error information is thus passed to the power controller through an opto-coupling device. This information is inverted, hence 0 V represents the maximum duty cycle, whilst 2 V represents minimum duty cycle. The error information enters the IC via pin EP, and is passed to the PWM generator via an inverting amplifier. The relationship between Duty cycle and  $V_{EP}$  is shown in the Typical Characteristic Graph, [Duty Cycle vs.  \$V\_{EP}\$  25°C](#), page 11. Voltage feedforward is implemented by taking the attenuated  $V_{IN}$  signal at  $V_{INDET}$  and directly modulating the duty cycle.

At start-up, i.e., once  $V_{CC}$  is greater than  $V_{UVLO}$ , switching is initiated under soft-start control which increases primary switch on-times linearly from  $D_{MIN}$  to  $D_{MAX}$  over the soft-start period. Start-up from a  $V_{INDET}$  power down is also initiated under soft-start control.

#### Half-Bridge and Synchronous Rectification Timing Sequence

The PWM signal generated within the Si9122A controls the low and high-side bridge drivers on alternative cycles. A period of inactivity always results after initiation of the soft-start cycle until the soft-start voltage reaches approximately 1.2 V and PWM controlled switching begins. The first bridge driver to switch is always the low-side ( $D_L$ ), as this allows charging of the high-side boost capacitor.

The timing and coordination of the drives to the primary and secondary stages is very important and shown in [Figure 3](#). It is essential to avoid the situation where both of the secondary MOSFETs are on when either the high or the low-side switch are active. In this situation the transformer would effectively be presented with a short across the output. To avoid this, a dedicated break-before-make circuit is included which will generate non overlapping waveforms for the primary and the secondary drive signals. This is achieved by a programmable timer which delays the switching on of the primary driver relative to the switching off of the related secondary and subsequently delays the switching on of the secondary relative to the switching off of the related primary.

Typical variations of BBM times with respect to  $R_{BBM}$  and other operating parameters are shown on page 13 and 14.

#### Primary High- and Low-Side MOSFET Drivers

The drive voltage for the low-side MOSFET switch is provided directly from  $V_{CC}$ . The high-side MOSFET however requires the gate voltage to be enhanced above  $V_{IN}$ . This is achieved by bootstrapping the  $V_{CC}$  voltage onto the  $L_X$  voltage (the high-side MOSFET source). In order to provide the bootstrapping an external diode and capacitor are required as shown on the application schematic. The capacitor will charge up after the low-side driver has turned on. The switch gate drive signals  $D_H$  and  $D_L$  are shown in [Figure 3](#).

#### Secondary MOSFET Drivers

The secondary side MOSFETs are driven from the Si9122A via a center tapped pulse transformer and inverter drivers. The waveforms from SRH and SRL are shown in [Figure 3](#). Of importance is the relative voltage between SRH and SRL, i.e. that which is presented across the primary of the pulse transformer. When both potentials of SRL and SRH are equal then by the action of the inverting drivers both secondary MOSFETs are turned on.

#### Oscillator

The oscillator is designed to operate at a nominal frequency of 500 kHz. The 500-kHz operating frequency allows the converter to minimize the inductor and capacitor size, improving the power density of the converter. The oscillator and therefore the switching frequency is programmable by attaching a resistor to the  $R_{OSC}$  pin. Under overload conditions the oscillator frequency is reduced by the current overload protection to enable a constant current to be maintained into a low impedance circuit.

**Current Limit**

Current mode control providing constant current operation is achieved by monitoring the differential voltage between the CS1 and CS2 pins which are connected across a primary low-side sense resistor. Once this differential voltage exceeds the 100-mV trigger point, the voltage on the CL\_CONT pin is pulled lower at a rate proportional to the excess voltage and the value of the external capacitor connected between the CL\_CONT pin and ground. If the voltage between CS1 and CS2 exceeds 150 mV the CL\_CONT capacitor is discharged rapidly resulting in minimum duty cycle and frequency immediately.

Lowering the CL\_CONT voltage results in PWM control of the output drive being taken over by the current limit control loop. Current control works to initially reduce the switching duty cycle down to D\_MIN (12.5%). Further reduction in the duty cycle is accompanied by a reduction in switching frequency at a rate proportional to the duty cycle. This prevents the on time of the primary drivers from falling below 100 ns, thereby avoiding “current tailing”. Frequency reduction will then occur until the operating frequency reaches 20% of the nominal frequency, yielding a duty cycle as low as 2.5% during output overloads.

With constant current mode control of on time and with reduced operating frequency, protection of the MOSFET switches is increased during fault conditions. Minimum duty cycle and reduced frequency switching continues for the duration of the fault condition. The converter reverts to voltage mode operation immediately whenever the primary current fails to reach the limit level. CL\_CONT clamps to 6.5 V when not in current limit.

The soft-start function does not apply under current limit as this would constitute hiccup mode operation.

**V\_IN Voltage Monitor –V\_INDET**

The chip provides a means of sensing the voltage of V\_IN, and withholding operation of the output drivers until a minimum

voltage of V\_REF (3.3 V, 300-mV hysteresis), is achieved. This is achieved by choosing an appropriate resistive tap between the ground and V\_IN, and comparing this voltage with the reference voltage. When the applied voltage is greater than V\_REF, the output drivers are activated as normal. V\_INDET also provides the input to the voltage feed forward function.

However, if the divided voltage applied to the V\_INDET pin is greater than V\_CC –0.3 V, the high-side driver, D\_H, will stop switching until the voltage drops below V\_CC –0.3 V. Thus, the resistive tap on the V\_IN divider must be set to accommodate the normal V\_CC operating voltage to avoid this condition. Alternatively, a zener clamp diode from V\_INDET to GND may also be used.

**Shutdown Mode**

If V\_INDET is forced below the lower V\_SD threshold, the device will enter SHUTDOWN mode. This powers down all unnecessary functions of the controller, ensures that the primary switches are off, and results in a low level current demand from the V\_IN or V\_CC supplies.

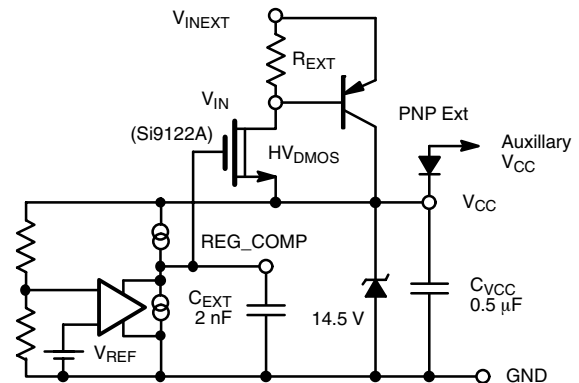


Figure 5. High-Voltage Pre-Regulator Circuit

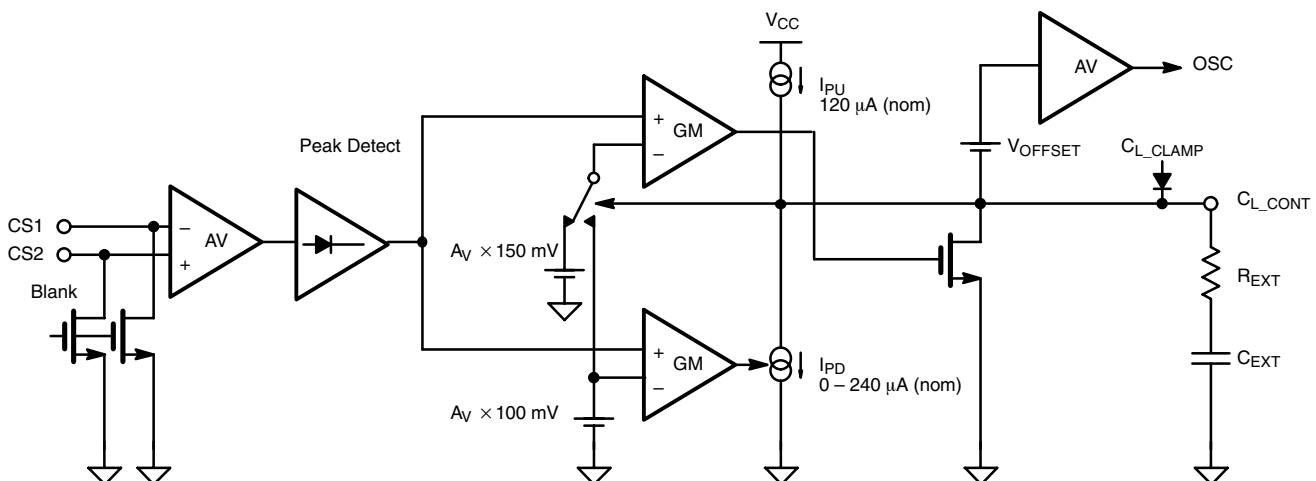
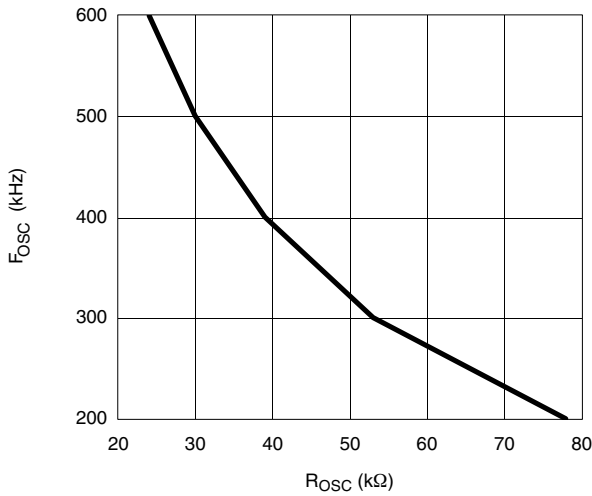


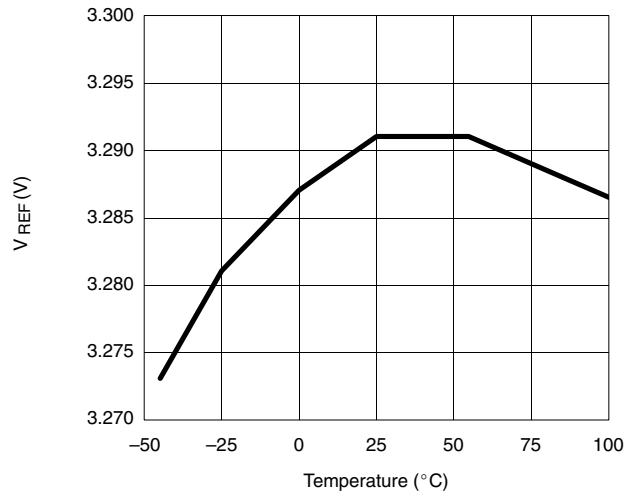
Figure 6. Current Limit Circuit

**TYPICAL CHARACTERISTICS**

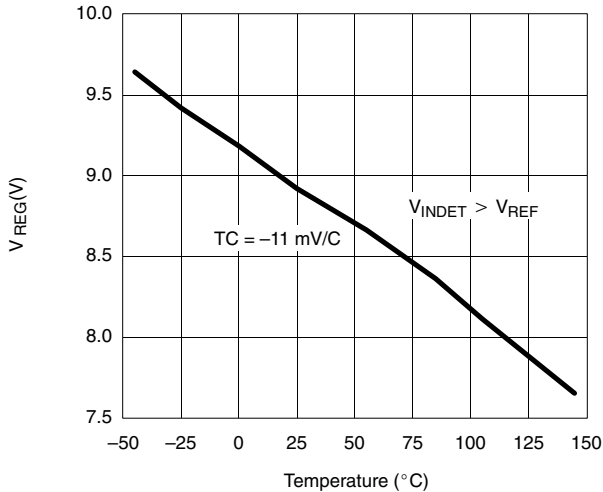
**F<sub>OSC</sub> vs. R<sub>OSC</sub> @ V<sub>CC</sub> = 12 V**



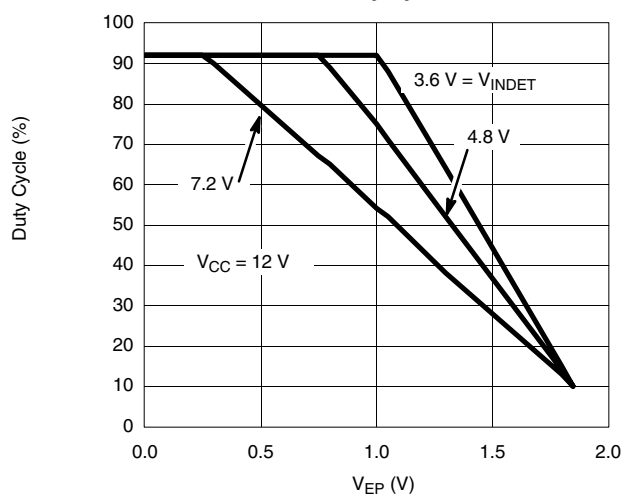
**V<sub>REF</sub> vs. Temperature, V<sub>CC</sub> = 12 V**



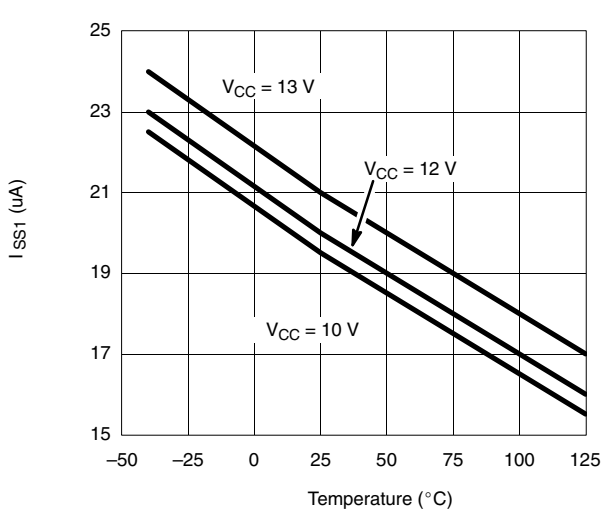
**V<sub>REG</sub> vs. Temperature, V<sub>IN</sub> = 48 V**



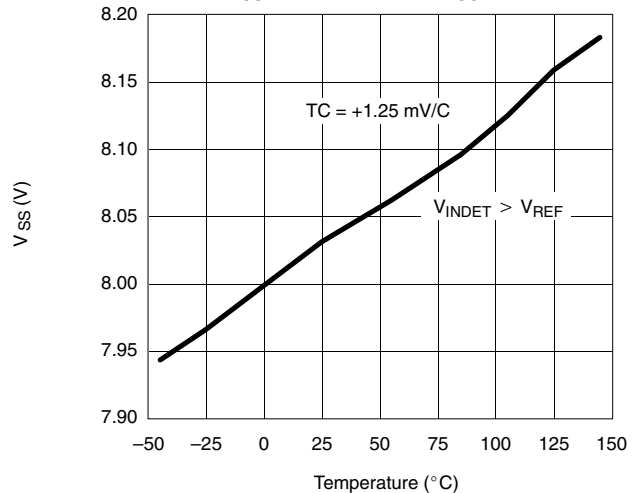
**SRL, SRH Duty Cycle vs. V<sub>EP</sub>**



**I<sub>SS1</sub> vs. Temperature**

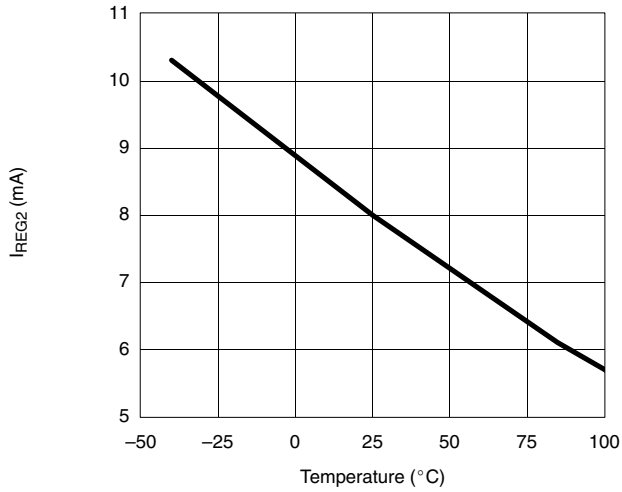


**V<sub>SS</sub> vs. Temperature, V<sub>CC</sub> = 12 V**

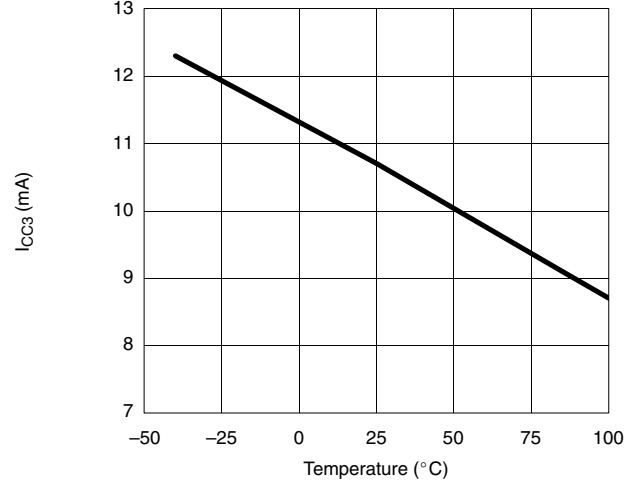


**TYPICAL CHARACTERISTICS**

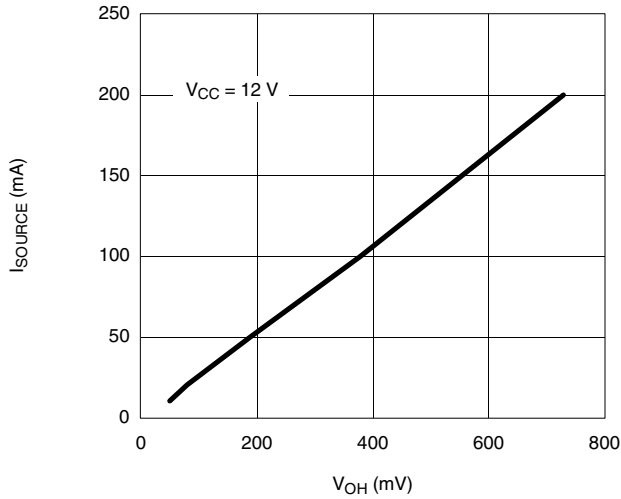
**I<sub>REG2</sub> vs. Temperature**



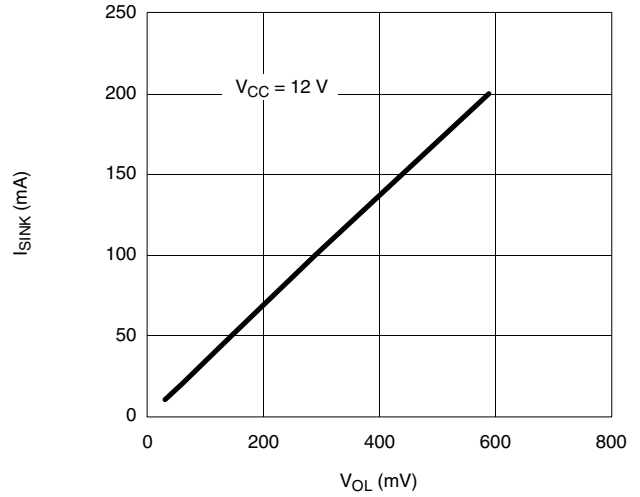
**I<sub>CC3</sub> vs. Temperature**



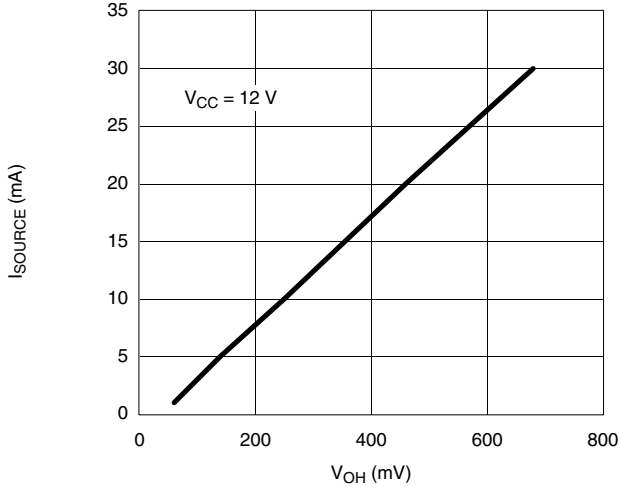
**D<sub>H</sub>, D<sub>L</sub> I<sub>SOURCE</sub> vs. V<sub>OH</sub>**



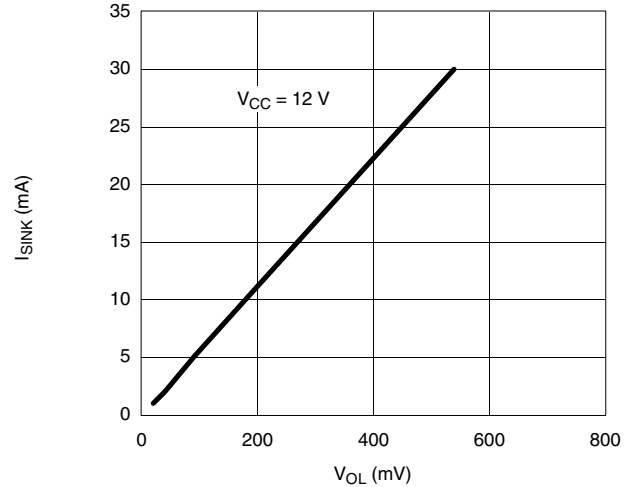
**D<sub>H</sub>, D<sub>L</sub> I<sub>SINK</sub> vs. V<sub>OL</sub>**



**SRL, SRH I<sub>SOURCE</sub> vs. V<sub>OH</sub>**



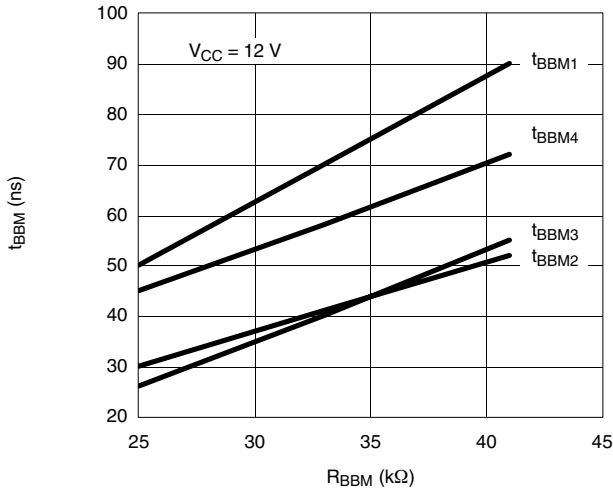
**SRL, SRH I<sub>SINK</sub> vs. V<sub>OL</sub>**



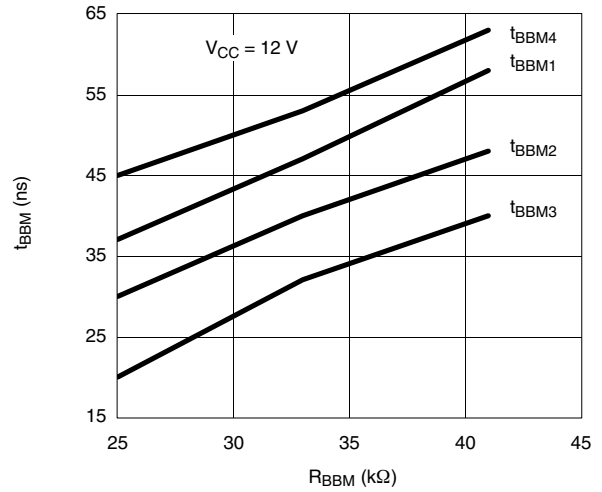


**TYPICAL CHARACTERISTICS**

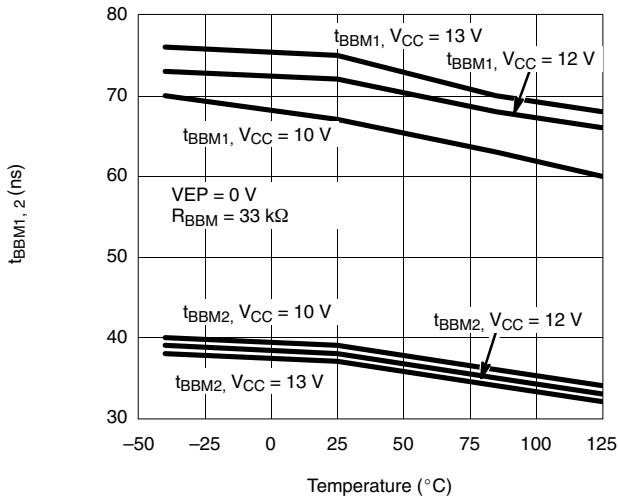
**$t_{BBM}$  vs.  $R_{BBM}$ ,  $V_{EP} = 0 V$**



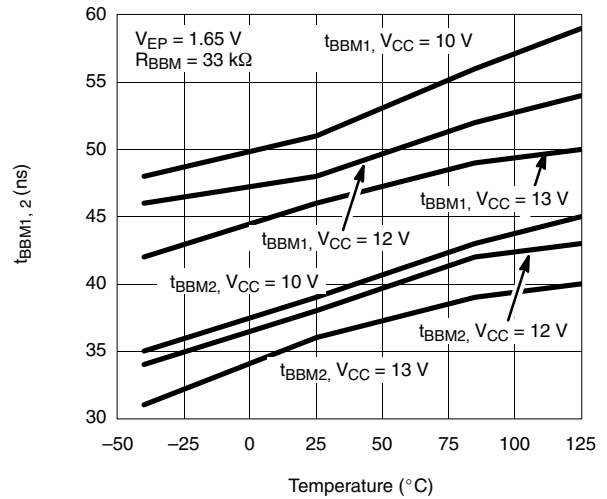
**$t_{BBM}$  vs.  $R_{BBM}$ ,  $V_{EP} = 1.65 V$**



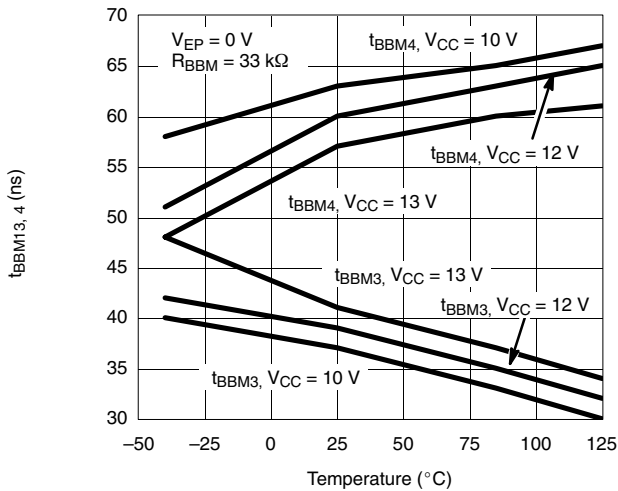
**$t_{BBM1, 2}$  vs. Temperature,  $V_{EP} = 0 V$**



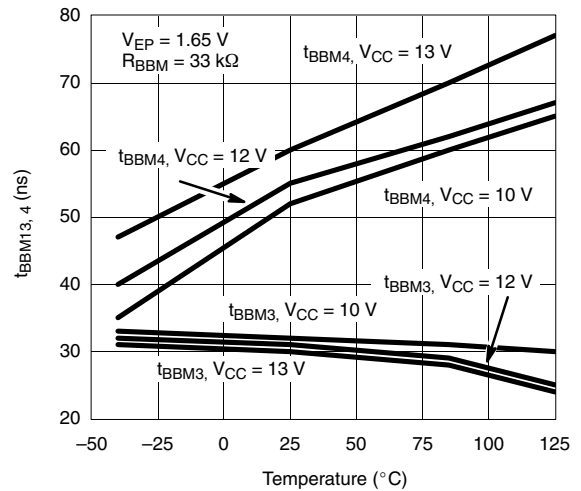
**$t_{BBM1, 2}$  vs. Temperature,  $V_{EP} = 1.65 V$**



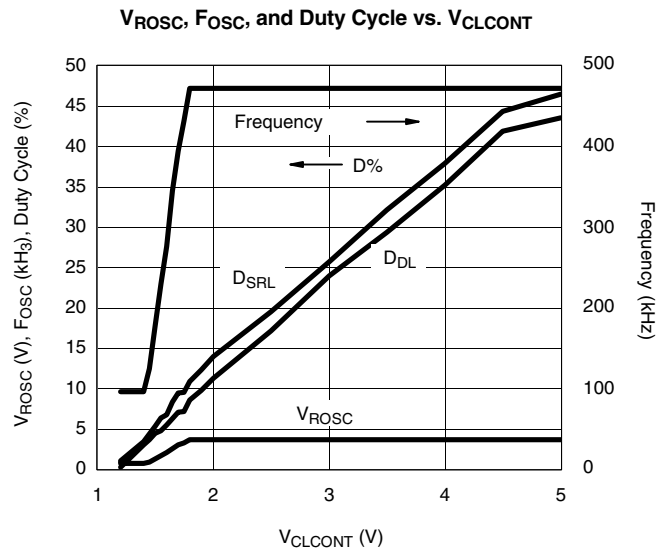
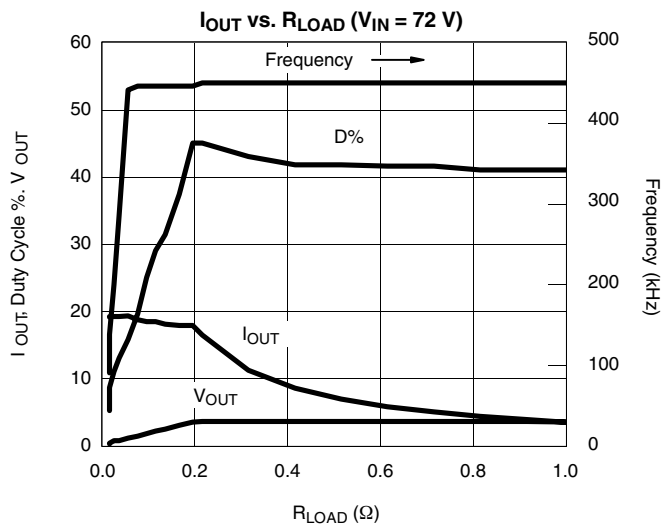
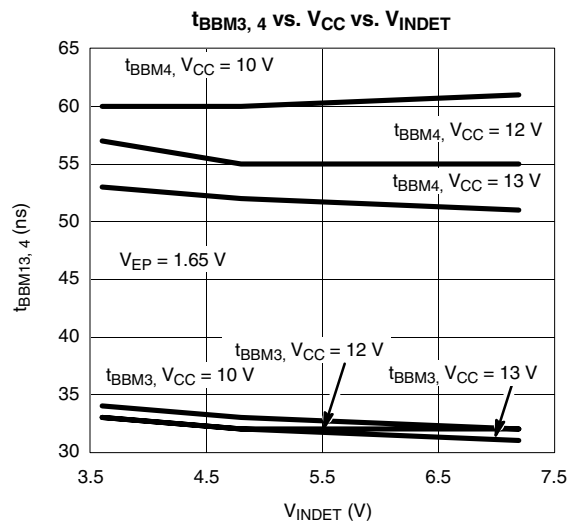
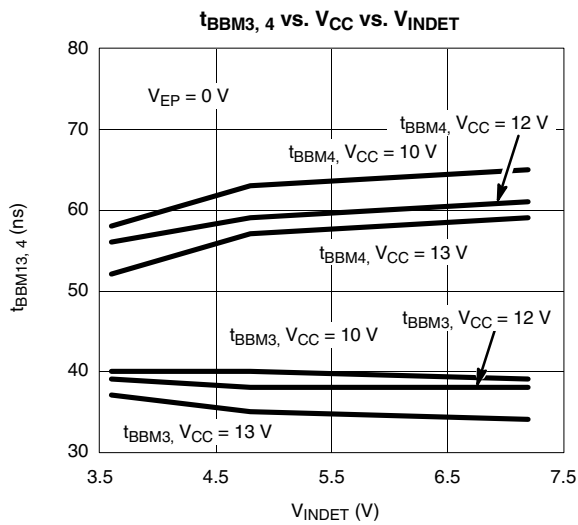
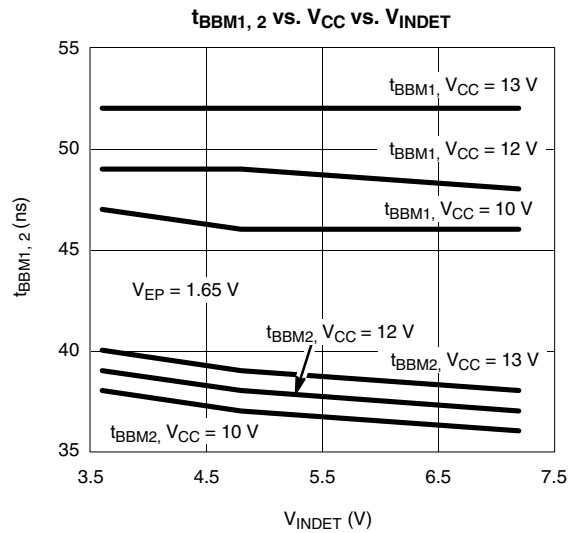
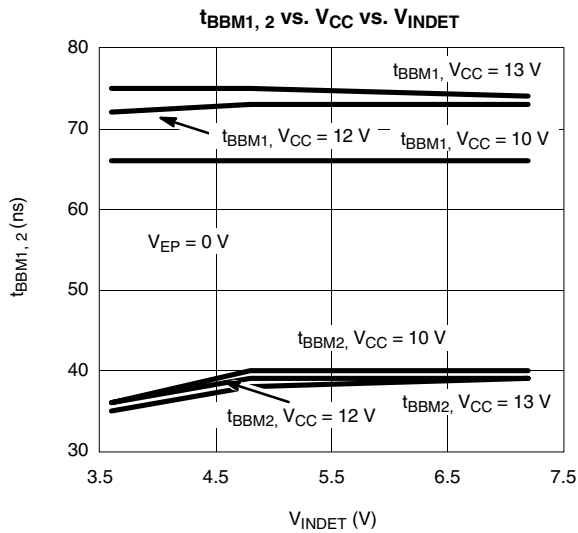
**$t_{BBM3, 4}$  vs. Temperature,  $V_{EP} = 0 V$**



**$t_{BBM3, 4}$  vs. Temperature,  $V_{EP} = 1.65 V$**

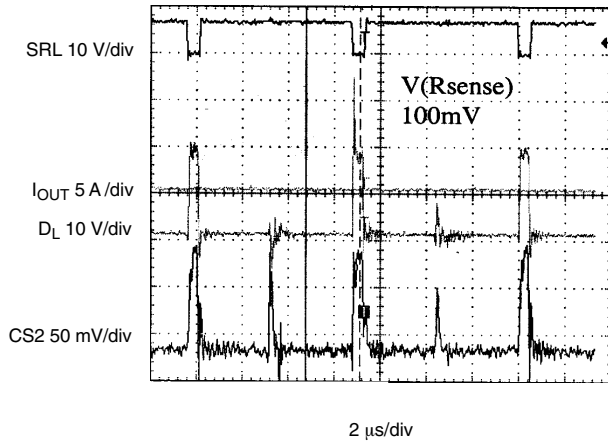


**TYPICAL CHARACTERISTICS**

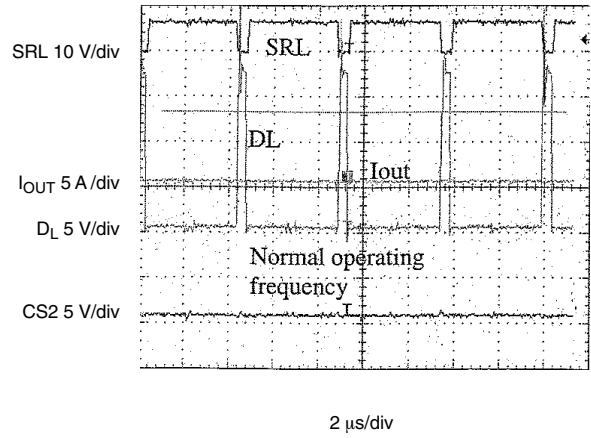


**TYPICAL WAVEFORMS**

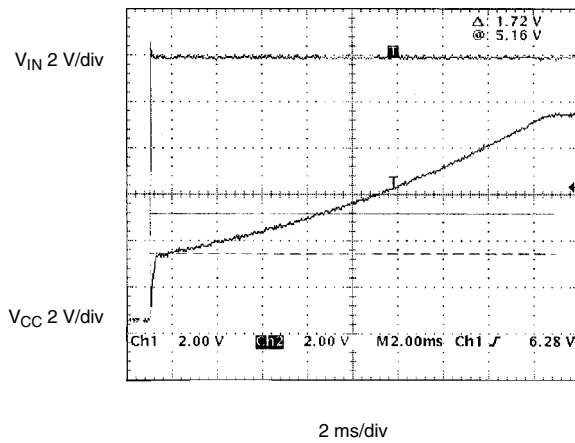
**Figure 7.** Foldback Mode,  $R_L = 0.02 \Omega$



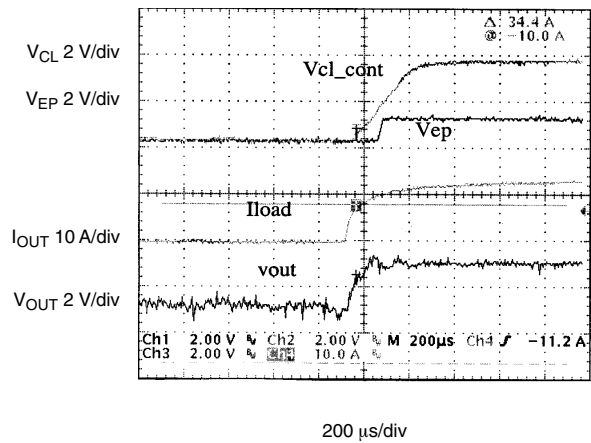
**Figure 8.** Normal Mode,  $R_L = 0.1 \Omega$



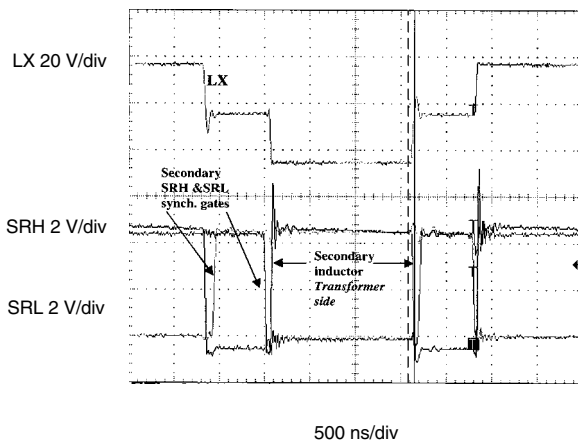
**Figure 9.** V<sub>CC</sub> Ramp-Up



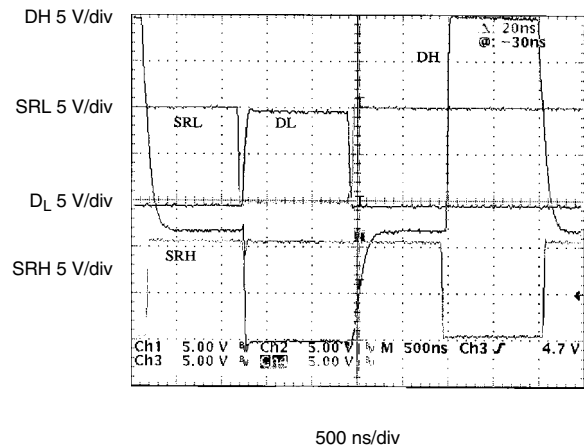
**Figure 10.** Overload Recovery



**Figure 11.** Effective BBM—Measured On Secondary



**Figure 12.** Drive Waveforms



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