Bi-Directional P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

V_{S1S2} (V)	$r_{S1S2(on)}$ (Ω)	I_{S1S2} (A)
−20	0.060 @ V_{GS} = −4.5 V	−4.4
	0.080 @ V_{GS} = −2.5 V	−3.9
	0.105 @ V_{GS} = −1.8 V	−3.4

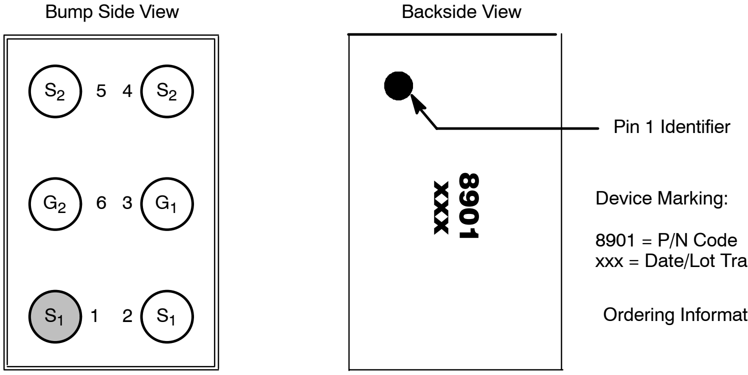
FEATURES

- TrenchFET® Power MOSFET
- Ultra-Low $r_{SS(on)}$
- New MICRO FOOT® Chipscale Packaging Reduces Footprint Area, Profile (0.65 mm) and On-Resistance Per Footprint Area

APPLICATIONS

- Smart Batteries for Portable Devices

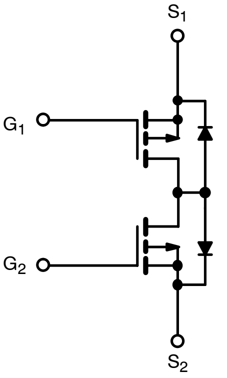
MICRO FOOT



Device Marking:

8901 = P/N Code
xxx = Date/Lot Traceability Code

Ordering Information: Si8901DB-T2—E3



P-Channel

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter		Symbol	5 secs	Steady State	Unit
Source1—Source2 Voltage		V_{S1S2}	−20		V
Gate-Source Voltage		V_{GS}	±8		
Continuous Source1—Source2 Current (T_J = 150°C)[a]	T_A = 25°C	I_{S1S2}	−4.4	−3.5	A
	T_A = 85°C		−3.2	−2.5	
Pulsed Source1—Source2 Current		I_{SM}	−30		
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.7	1	W
	T_A = 85°C		0.8	0.5	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C
Package Reflow Conditions[c]	VPR		215		
	IR/Convection		220		

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 5 sec	R_{thJA}	60	75	°C/W
	Steady State		95	120	
Maximum Junction-to-Foot[b]	Steady State	R_{thJF}	18	22	

Notes
a. Surface Mounted on 1” x 1” FR4 Board.
b. The Foot is defined as the top surface of the package.
c. Refer to IPC/JEDEC (J-STD-020A), no manual or hand soldering.

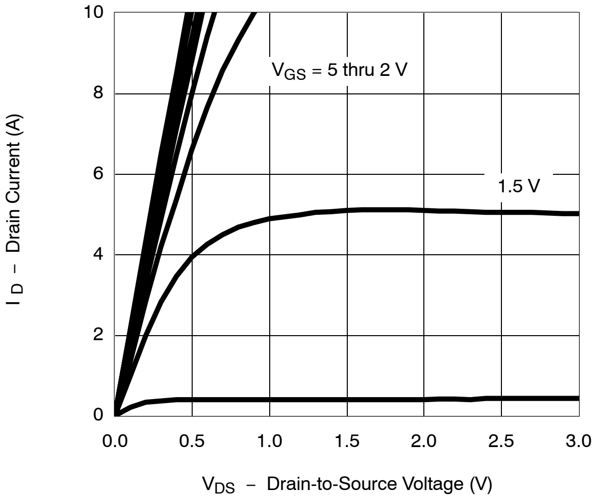
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{SS} = V_{GS}$, $I_D = -350\ \mu A$	−0.45		−1.0	V
Gate-Body Leakage	I_{GSS}	$V_{SS} = 0$ V, $V_{GS} = \pm 8$ V			±100	nA
Zero Gate Voltage Source Current	I_{S1S2}	$V_{SS} = -20$ V, $V_{GS} = 0$ V			−1	µA
		$V_{SS} = -20$ V, $V_{GS} = 0$ V, $T_J = 85°C$			−5	
On-State Source Current[a]	$I_{S(on)}$	$V_{SS} = -5$ V, $V_{GS} = -4.5$ V	−5			A
Source1—Source2 On-State Resistance[a]	$r_{S1S2(on)}$	$V_{GS} = -4.5$ V, $I_{SS} = -1$ A		0.048	0.060	Ω
		$V_{GS} = -2.5$ V, $I_{SS} = -1$ A		0.062	0.080	
		$V_{GS} = -1.8$ V, $I_{SS} = -1$ A		0.081	0.105	
Forward Transconductance[a]	g_{fs}	$V_{SS} = -10$ V, $I_{SS} = -1$ A		7		S
Dynamic[b]						
Gate Resistance	R_g			9.5		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{SS} = -10$ V, $R_L = 10\ \Omega$ $I_{SS} \cong -1$ A, $V_{GEN} = -4.5$ V, $R_g = 6\ \Omega$		13	20	ns
Rise Time	t_r			27	40	
Turn-Off Delay Time	$t_{d(off)}$			120	180	
Fall Time	t_f			65	100	

Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

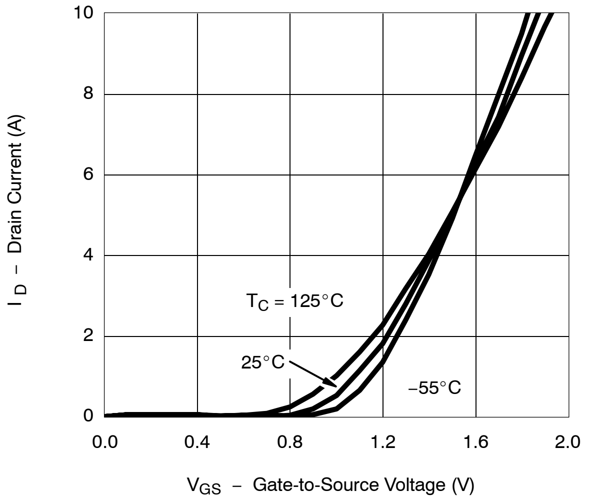
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

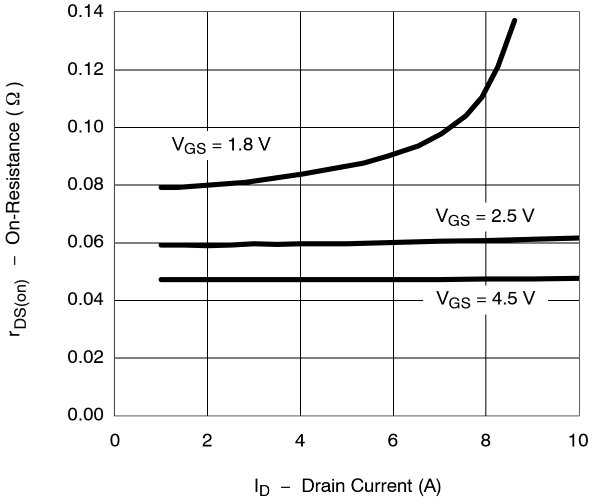
Output Characteristics



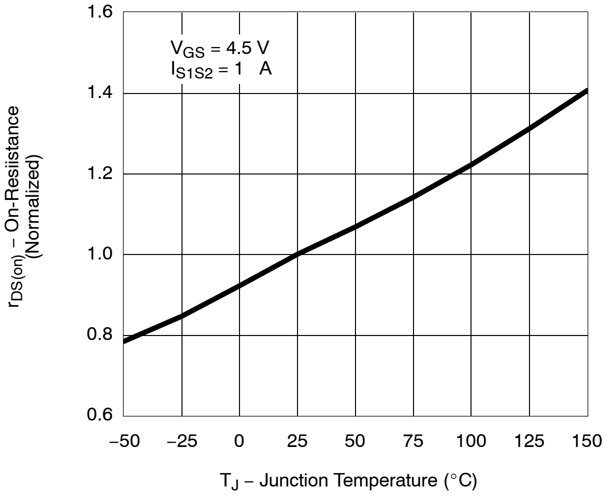
Transfer Characteristics



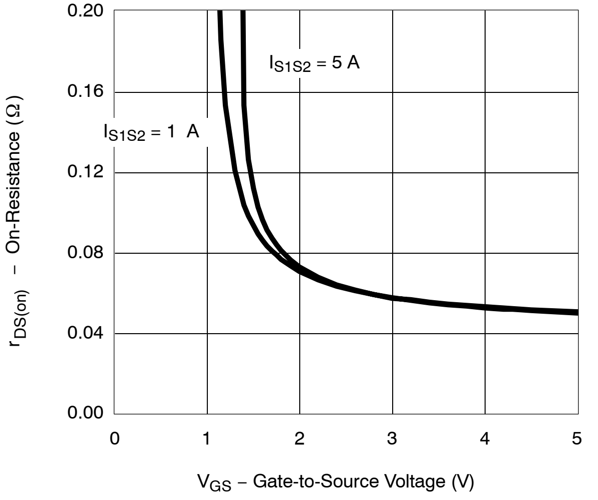
On-Resistance vs. Drain Current



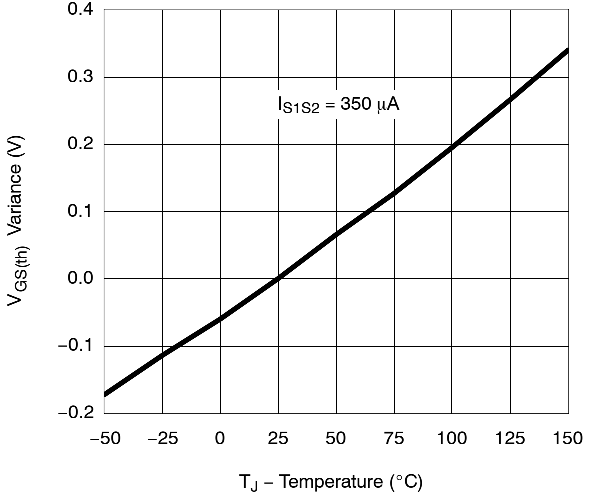
On-Resistance vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage

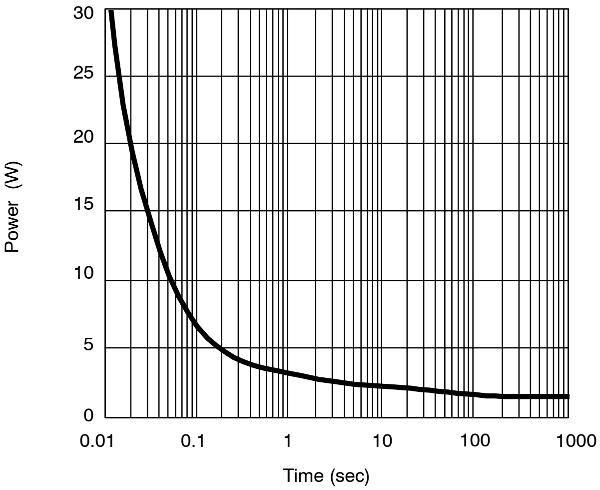


Threshold Voltage

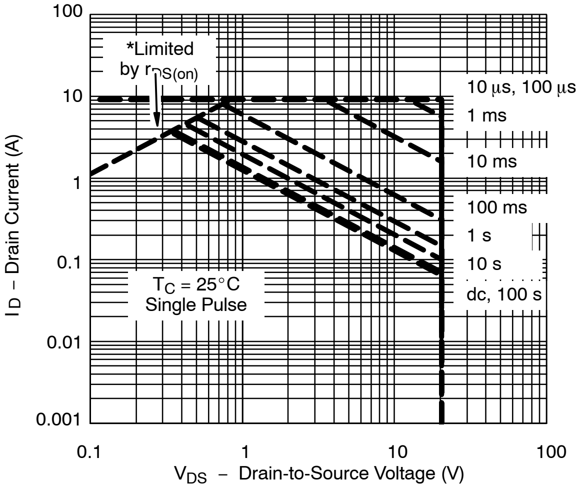


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Single Pulse Power, Junction-to-Ambient

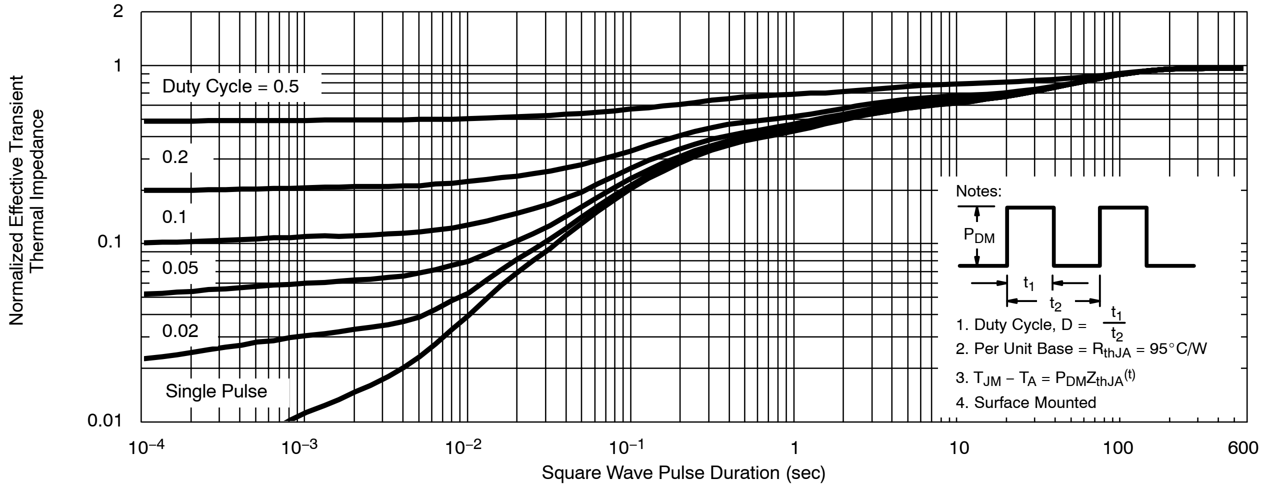


Safe Operating Area



*V_{GS} > minimum V_{GS} at which $r_{DS(on)}$ is specified

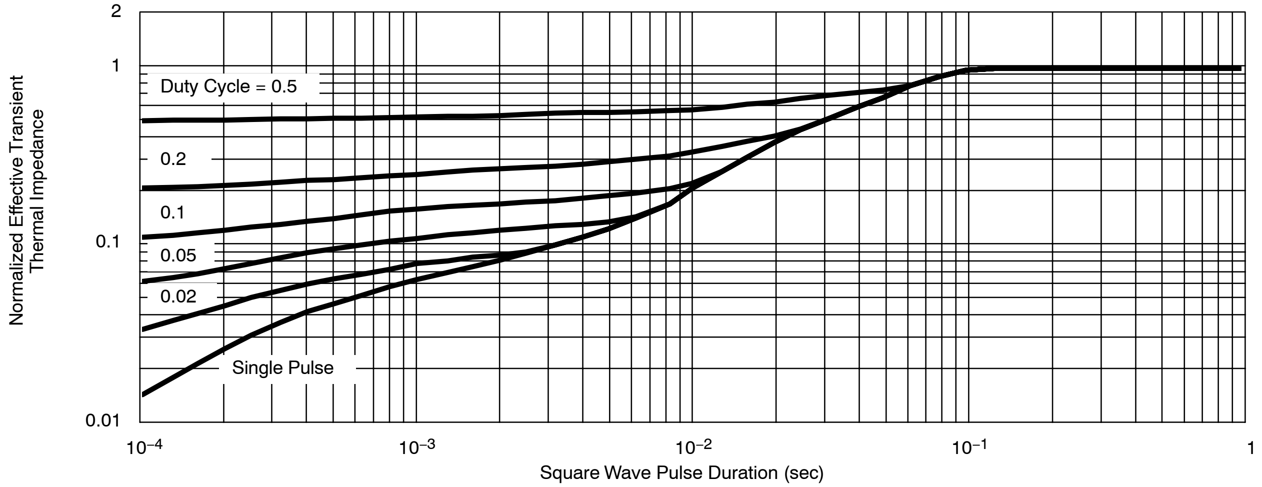
Normalized Thermal Transient Impedance, Junction-to-Ambient



Notes:

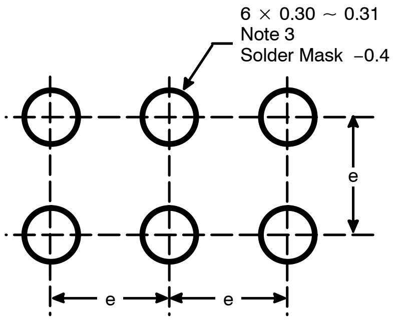
1. Duty Cycle, D = $\frac{t_1}{t_2}$
2. Per Unit Base = R_{thJA} = 95°C/W
3. $T_{JM} - T_A = P_{DM}Z_{thJA}^{(t)}$
4. Surface Mounted

Normalized Thermal Transient Impedance, Junction-to-Foot

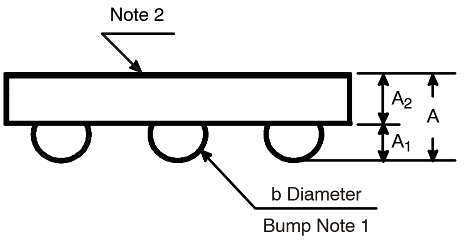


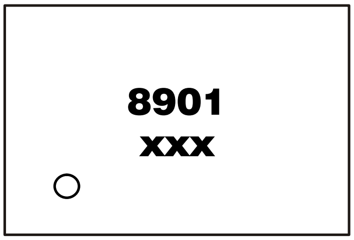
PACKAGE OUTLINE

MICRO FOOT: 6-BUMP (2 X 3, 0.8-mm PITCH)

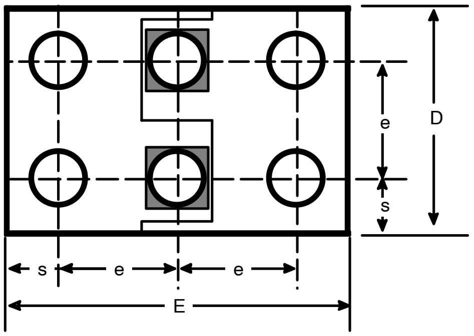


Recommended Land





Mark on Backside of Die



NOTES (Unless Otherwise Specified):

1. 6 solder bumps are Eutetic 63Sn/37Pb with diameter 0.37 – 0.41 mm
2. Backside surface is coated with a Ag/Ni/Ti layer
3. Non-solder mask defined copper landing pad.
4. Laser marks on the silicon die back

	MILLIMETERS*		INCHES	
Dim	Min	Max	Min	Max
A	0.600	0.650	0.0236	0.0256
A_1	0.260	0.290	0.102	0.114
A_2	0.340	0.360	0.0134	0.0142
b	0.370	0.410	0.0146	0.0161
D	1.52	1.6	0.0598	0.0630
E	2.32	2.4	0.0913	0.0945
e	0.750	0.850	0.0295	0.0335
s	0.380	0.400	0.0150	0.0157

* Use millimeters as the primary measurement.

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