

N-Channel 30-V (D-S) Fast Switching MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.0065 @ $V_{GS} = 10$ V	21
	0.008 @ $V_{GS} = 4.5$ V	19

FEATURES

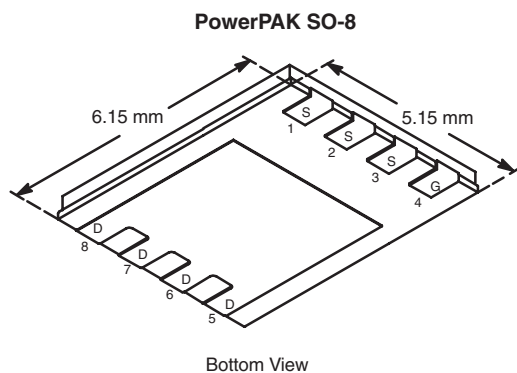
- TrenchFET[®] Power MOSFET
- New Low Thermal Resistance PowerPAK[®] Package with Low 1.07-mm Profile
- 100 % R_G Tested



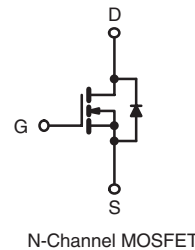
RoHS+
COMPLIANT

APPLICATIONS

- DC/DC Converters
- Optimized for “Low-Side” Synchronous Rectifier Operation



Ordering Information: Si7440DP-T1
Si7440DP-T1—E3 (Lead (Pb)-Free)



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	30		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	21	12	A
		$T_A = 70^\circ\text{C}$	17	9	
Pulsed Drain Current	I_{DM}	60			
Continuous Source Current (Diode Conduction) ^a	I_S	4.3	1.6		
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	5.4	1.9	W
		$T_A = 70^\circ\text{C}$	3.4	1.2	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature) ^{b,c}		260			

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	18	23	$^\circ\text{C/W}$
	Steady State		52	65	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.0	1.3	

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
b. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

* Pb containing terminations are not RoHS compliant, exemptions may apply.



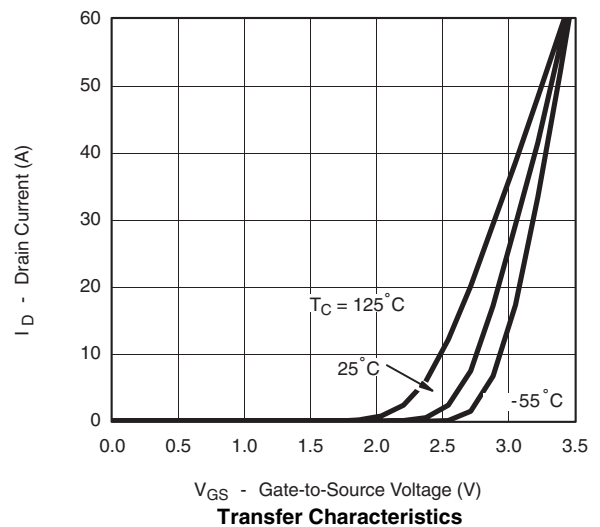
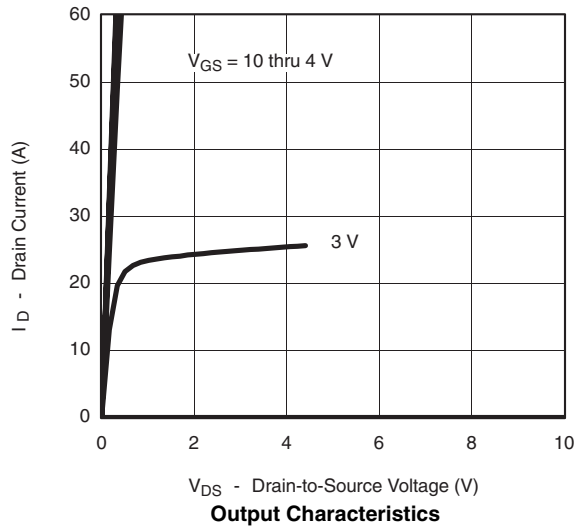
MOSFET SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0		3.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	40			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 21\text{ A}$		0.0053	0.0065	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 19\text{ A}$		0.0065	0.008	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 21\text{ A}$		65		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 4.3\text{ A}, V_{GS} = 0\text{ V}$		0.72	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 21\text{ A}$		29.0	35	nC
Gate-Source Charge	Q_{gs}		10.5			
Gate-Drain Charge	Q_{gd}		10.0			
Gate Resistance	R_g		0.5	1.4	2.2	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 15\text{ }\Omega$ $I_D \cong 1.0\text{ A}, V_{GEN} = 10\text{ V}, R_G = 6\text{ }\Omega$		18	28	ns
Rise Time	t_r		16	25		
Turn-Off Delay Time	$t_{d(off)}$		75	180		
Fall Time	t_f		41	65		
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 4.3\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		50	80	

Notes

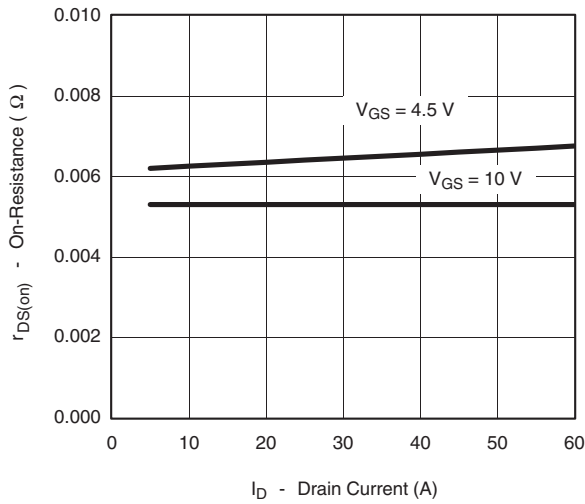
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

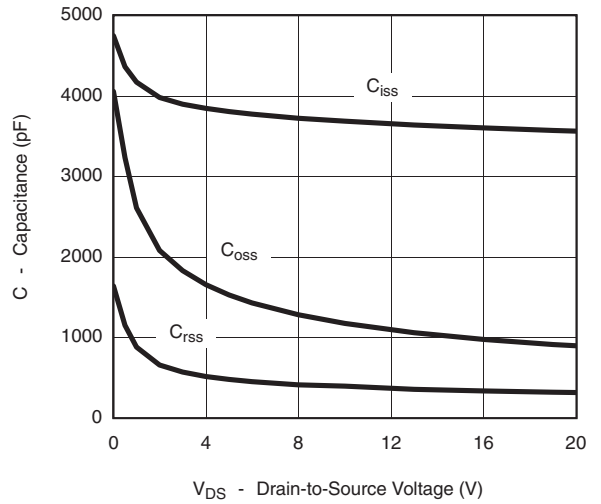
TYPICAL CHARACTERISTICS $25\text{ }^\circ\text{C}$, unless noted



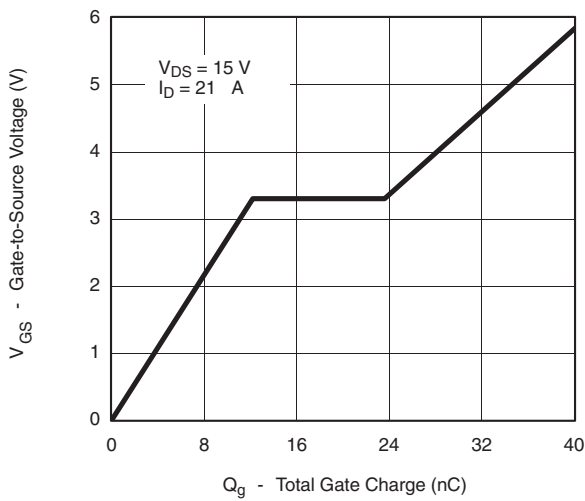
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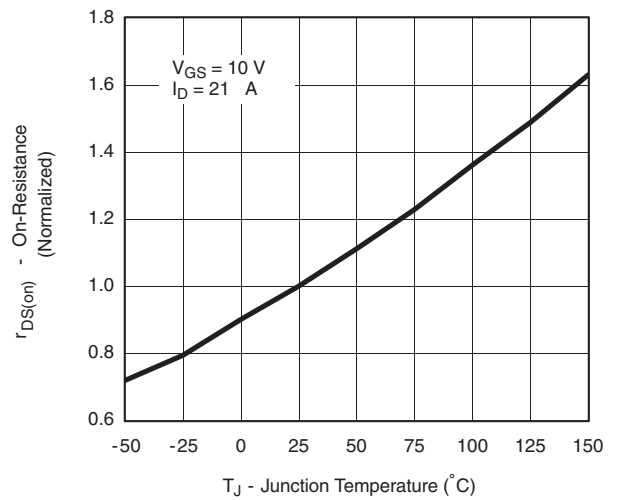
On-Resistance vs. Drain Current



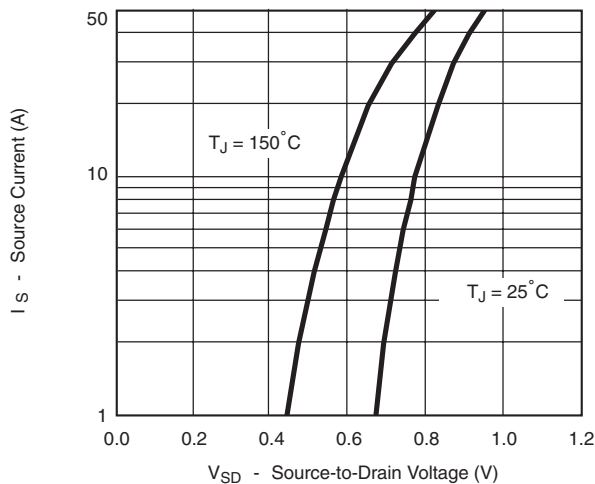
Capacitance



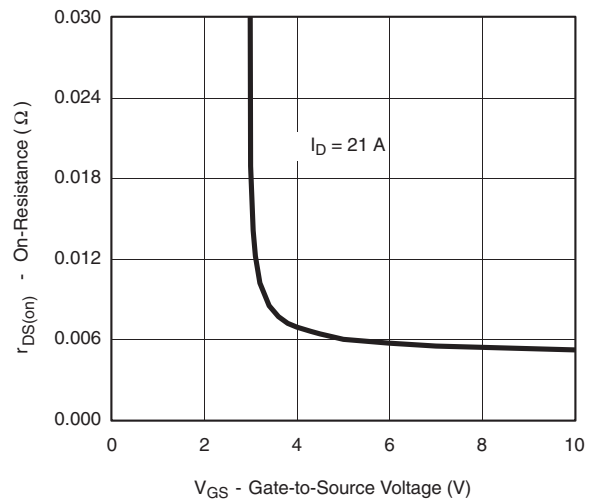
Gate Charge



On-Resistance vs. Junction Temperature

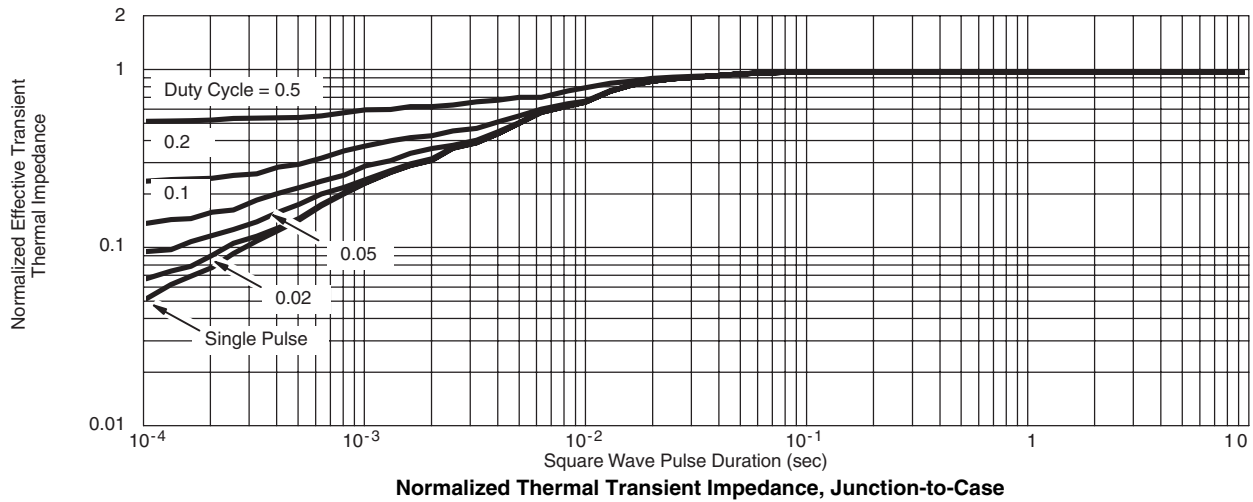
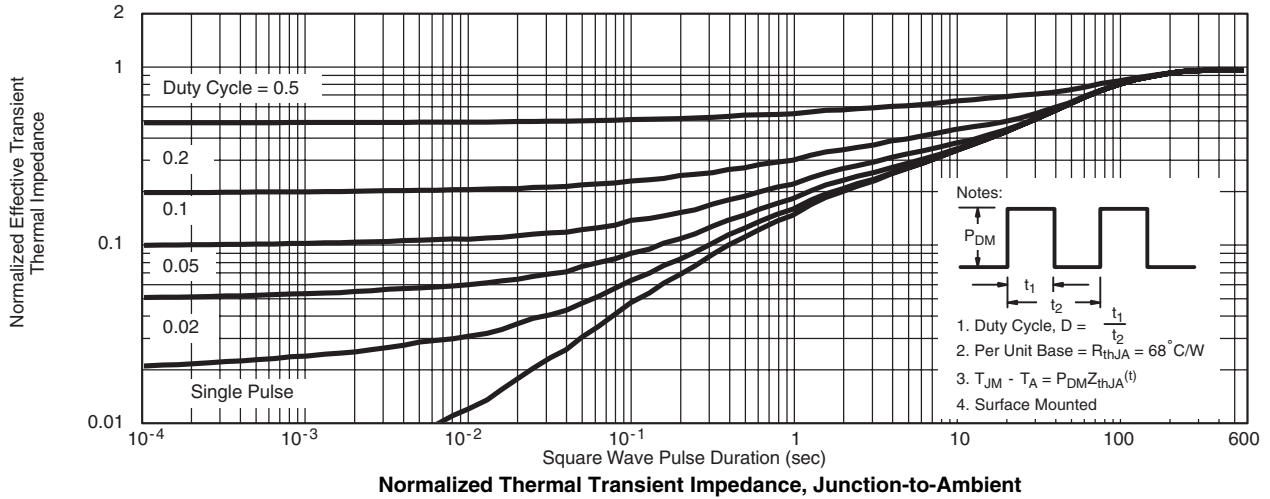
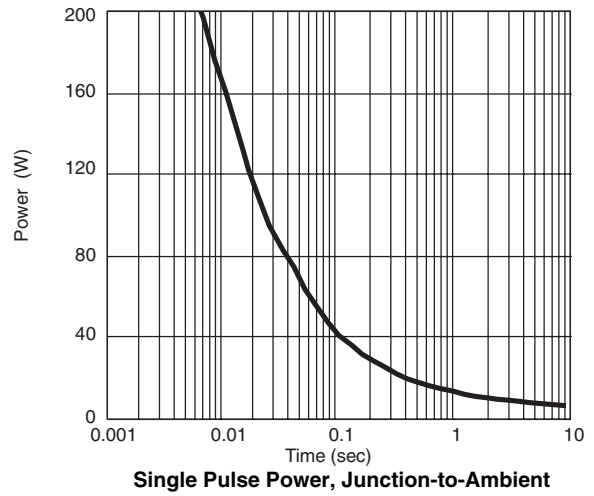
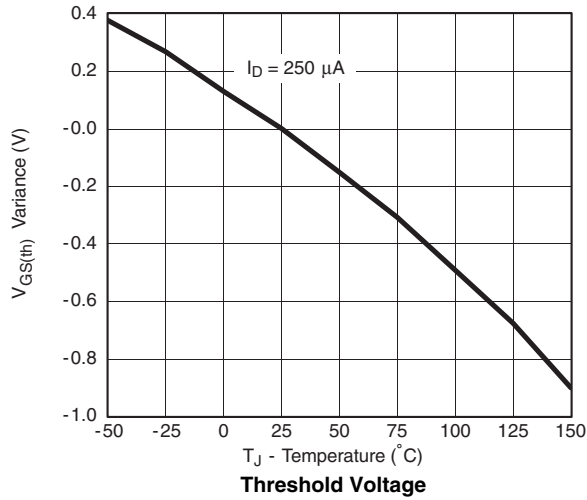


Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?71623>.