

N- and P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.0145 at $V_{GS} = 10$ V	9.6
		0.017 at $V_{GS} = 4.5$ V	8.6
P-Channel	- 20	0.033 at $V_{GS} = - 4.5$ V	- 6.2
		0.050 at $V_{GS} = - 2.5$ V	- 5

FEATURES

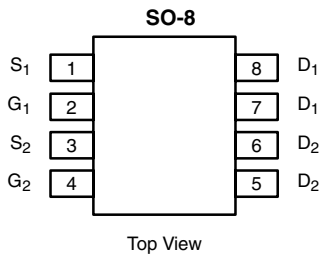
- TrenchFET® Power MOSFET

APPLICATIONS

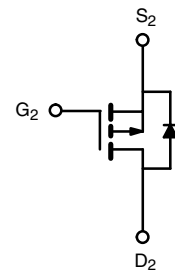
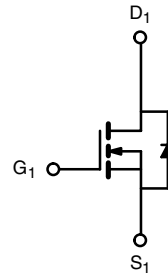
- Level Shift
- Load Switch



Available
RoHS*
COMPLIANT



Ordering Information: Si4511DY-T1
Si4511DY-T1-E3 (Lead (Pb)-Free)



ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter		Symbol	N-Channel		P-Channel		Unit
			10 secs	Steady	10 secs	Steady	
Drain-Source Voltage		V _{DS}	20		- 20		V
Gate-Source Voltage		V _{GS}	± 16		± 12		
Continuous Drain Current (T _J = 150 °C) ^{a, b}	T _A = 25 °C	I _D	9.6	7.2	- 6.2	- 4.6	A
	T _A = 70 °C		7.7	5.8	- 4.9	- 3.7	
Pulsed Drain Current		I _{DM}	40		- 40		
Continuous Source Current (Diode Conduction) ^a		I _S	1.7	0.9	- 1.7	0.9	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	2	1.1	2	1.1	W
	T _A = 70 °C		1.3	0.7	1.3	0.7	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150				°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	N-Channel		P-Channel		Unit
		Typ	Max	Typ	Max	
Maximum Junction-to-Ambient ^a	R_{thJA}	50	62.5	50	62.5	°C/W
		85	110	90	110	
Maximum Junction-to-Foot (Drain)	R_{thJF}	30	40	30	35	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. $t \leq 10$ sec

* Pb containing terminations are not RoHS compliant, exemptions may apply.

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	0.6		1.8	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-0.6		1.4	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$	N-Ch			± 100	nA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$	P-Ch			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1	
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^{\circ}\text{C}$	N-Ch			5	
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^{\circ}\text{C}$	P-Ch			-5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	N-Ch	40			A
		$V_{DS} = -5\text{ V}, V_{GS} = -4.5\text{ V}$	P-Ch	-40			
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 9.6\text{ A}$	N-Ch		0.0115	0.0145	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -6.2\text{ A}$	P-Ch		0.022	0.033	
		$V_{GS} = 4.5\text{ V}, I_D = 8.6\text{ A}$	N-Ch		0.0135	0.017	
		$V_{GS} = -2.5\text{ V}, I_D = -5\text{ A}$	P-Ch		0.035	0.050	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 9.6\text{ A}$	N-Ch		33		S
		$V_{DS} = -15\text{ V}, I_D = -6.2\text{ A}$	P-Ch		17		
Diode Forward Voltag ^b	V_{SD}	$I_S = 1.7\text{ A}, V_{GS} = 0\text{ V}$	N-Ch		0.8	1.2	V
		$I_S = -1.7\text{ A}, V_{GS} = 0\text{ V}$	P-Ch		-0.8	-1.2	
Dynamic ^a							
Total Gate Charge	Q_g	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 9.6\text{ A}$	N-Ch		11.5	18	nC
Gate-Source Charge	Q_{gs}		P-Ch		17	20	
Gate-Drain Charge	Q_{gd}	P-Channel $V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -6.2\text{ A}$	N-Ch		3.7		
			P-Ch		4.1		
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \equiv 1\text{ A}, V_{GEN} = 10\text{ V}, R_G = 6\text{ }\Omega$	N-Ch		12	20	ns
Rise Time	t_r		P-Ch		25	40	
			N-Ch		12	20	
Turn-Off Delay Time	$t_{d(off)}$		P-Ch		30	45	
		N-Ch		55	85		
Fall Time	t_f	P-Channel $V_{DD} = -10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \equiv -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_G = 6\text{ }\Omega$	P-Ch		70	105	
			N-Ch		15	25	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	N-Ch		50	100	
		$I_F = -1.7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	P-Ch		40	80	

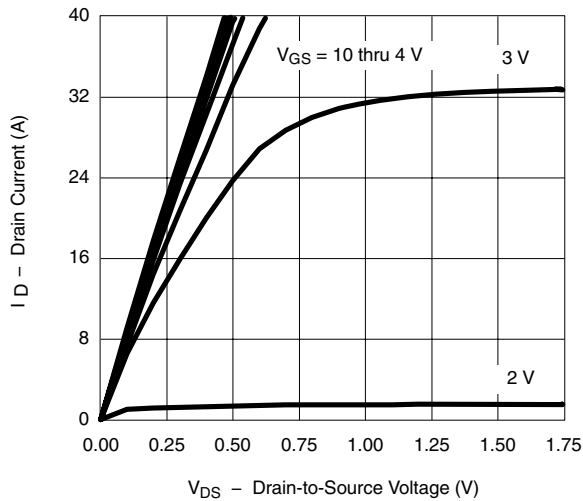
Notes

a. Guaranteed by design, not subject to production testing.

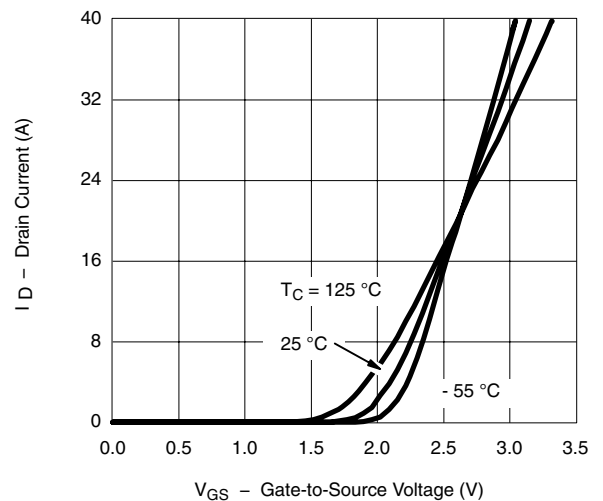
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

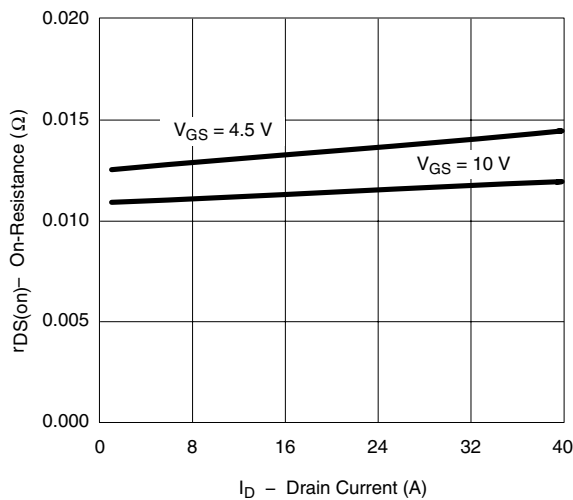
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless noted



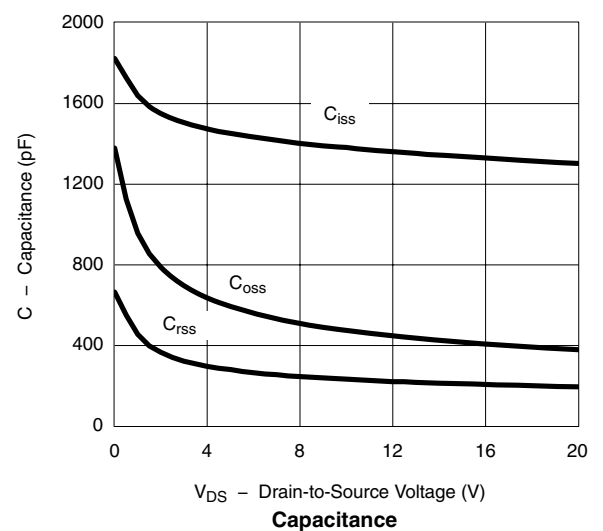
Output Characteristics



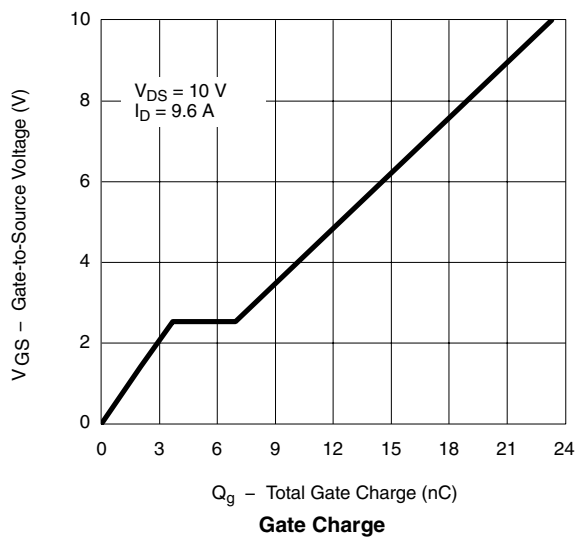
Transfer Characteristics



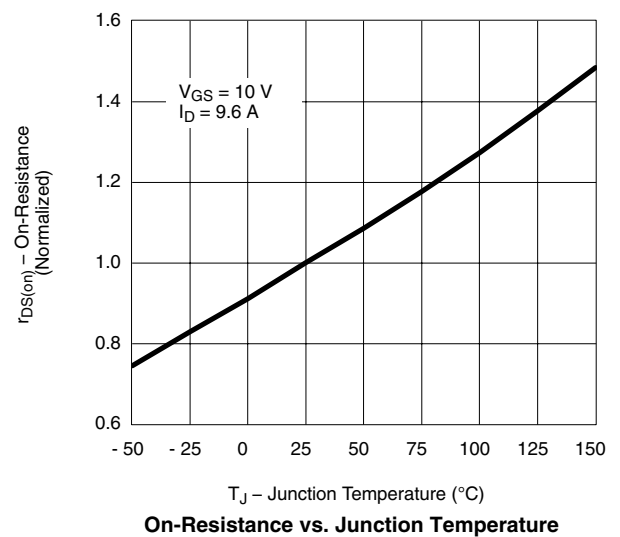
On-Resistance vs. Drain Current



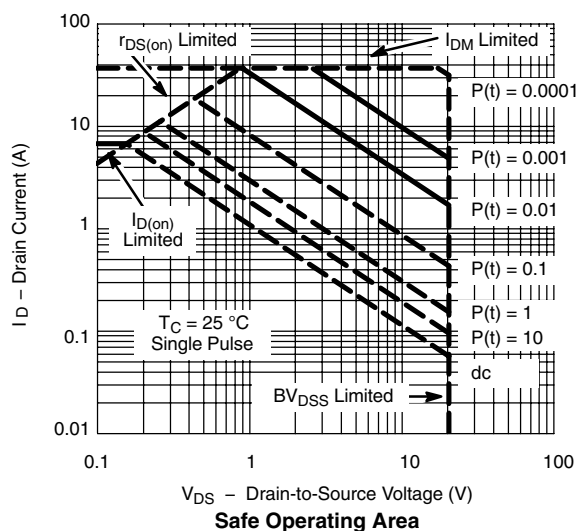
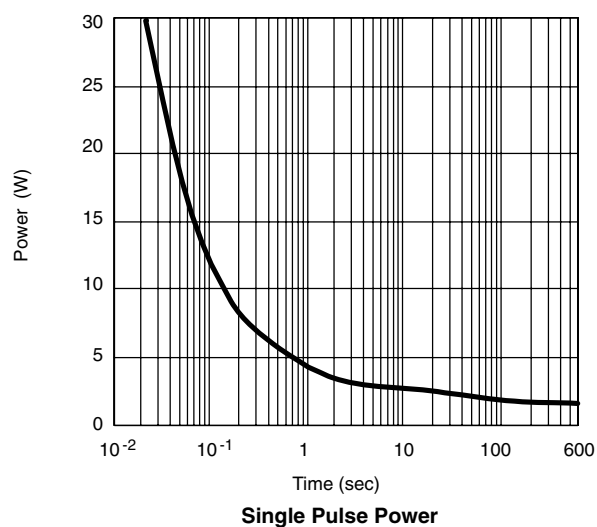
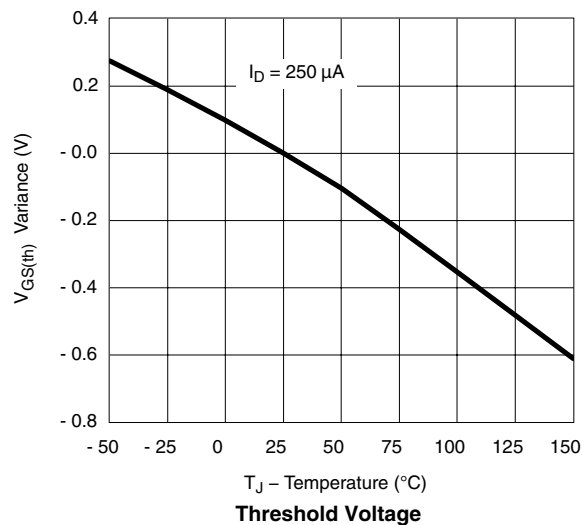
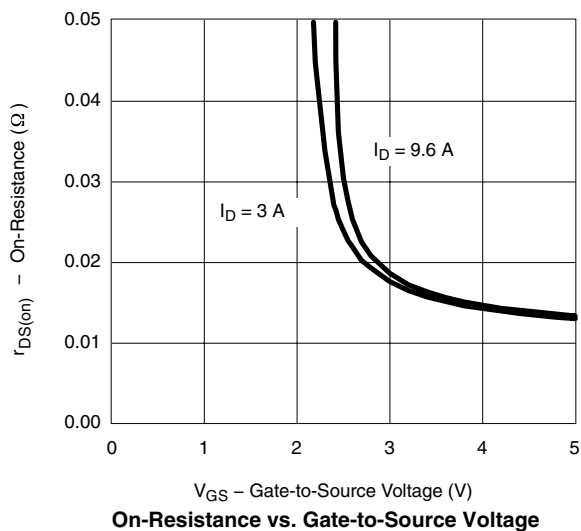
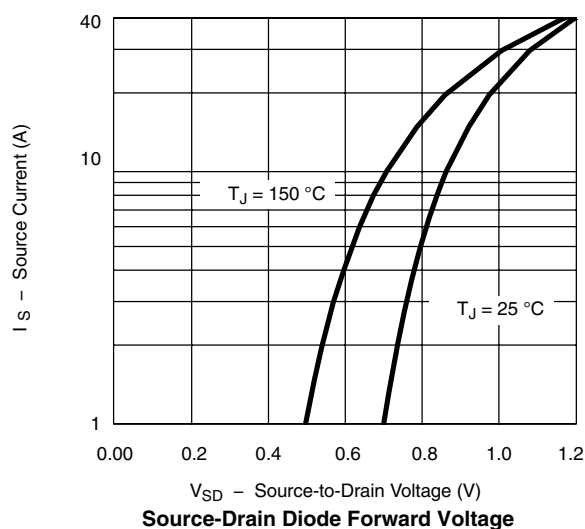
Capacitance



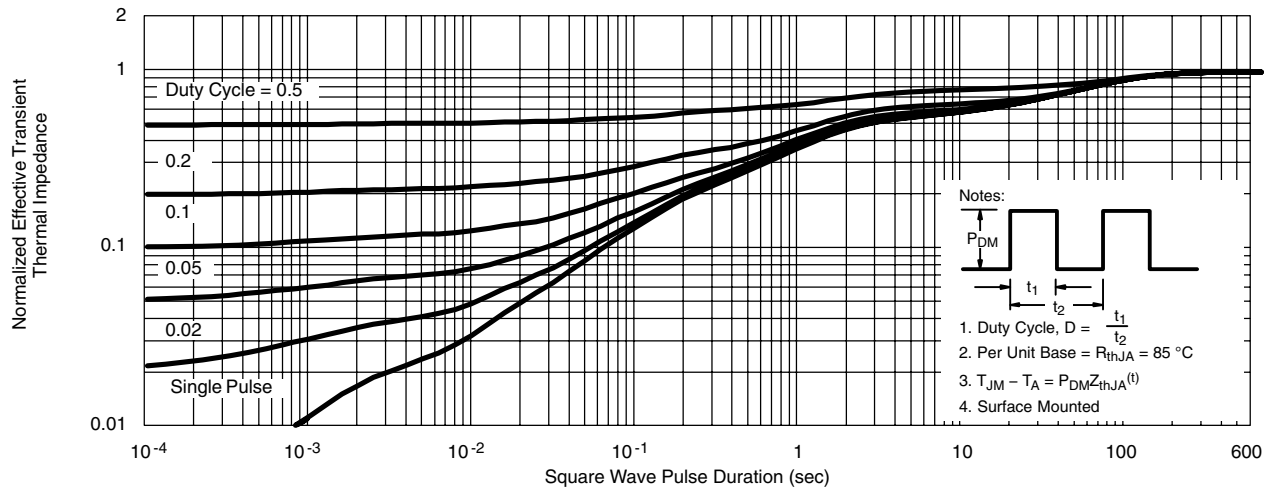
Gate Charge



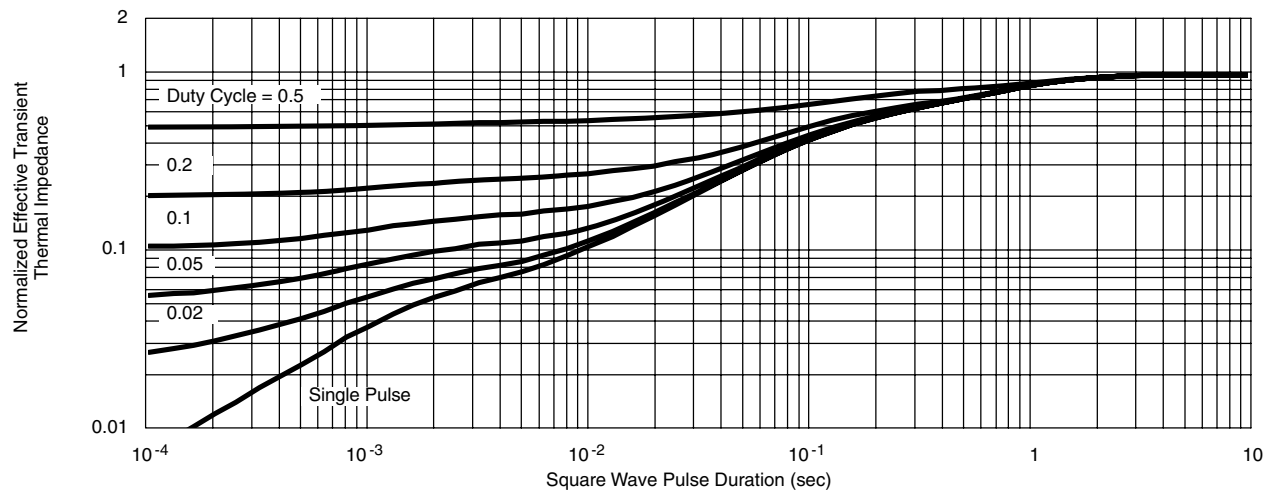
On-Resistance vs. Junction Temperature

N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless noted

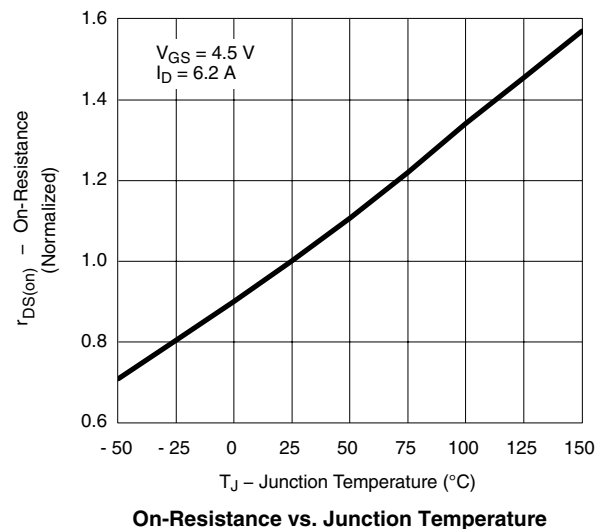
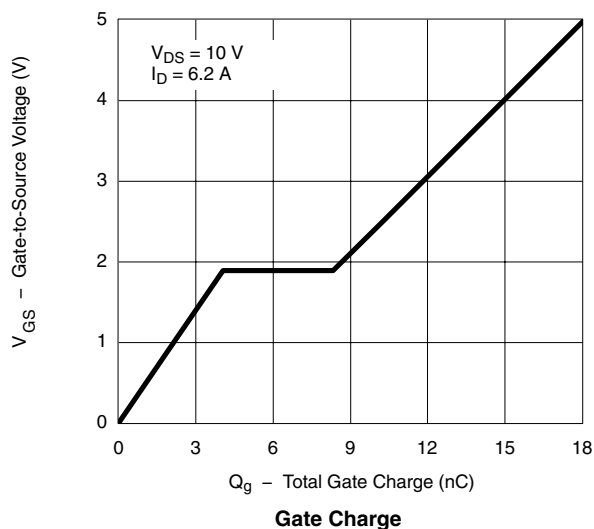
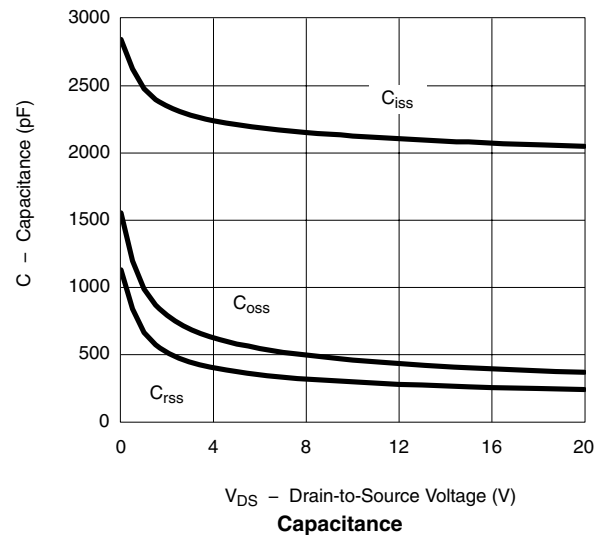
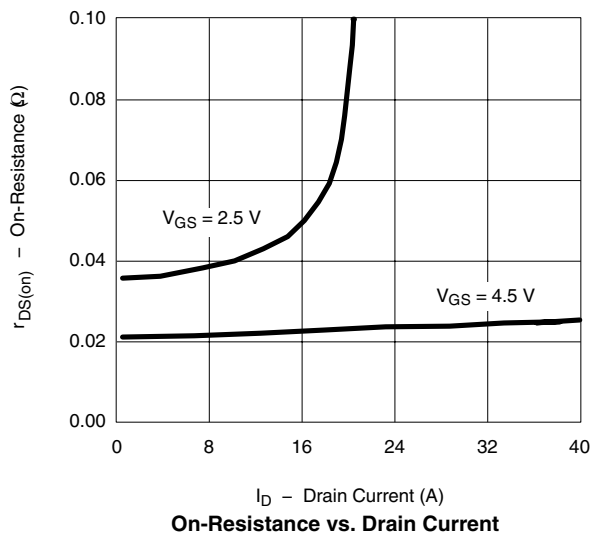
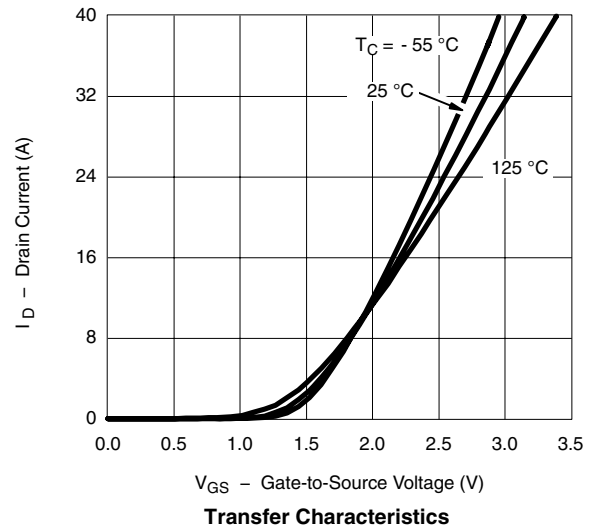
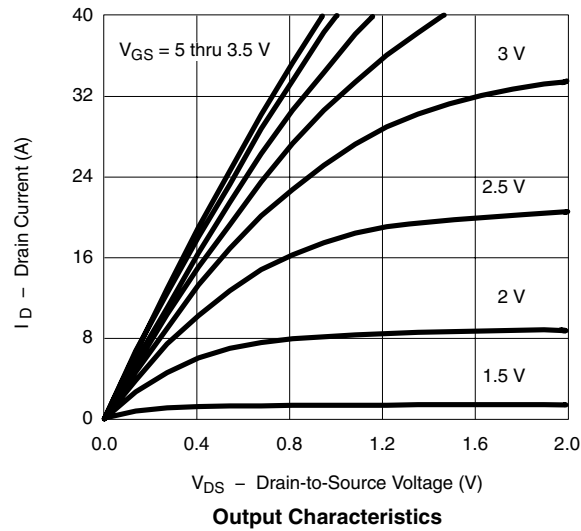
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless noted



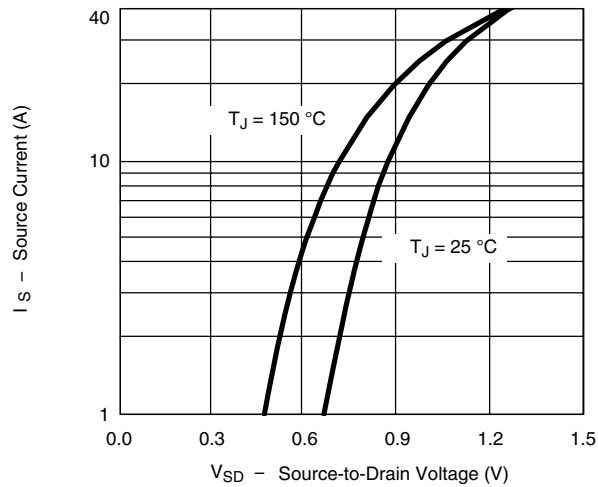
Normalized Thermal Transient Impedance, Junction-to-Ambient



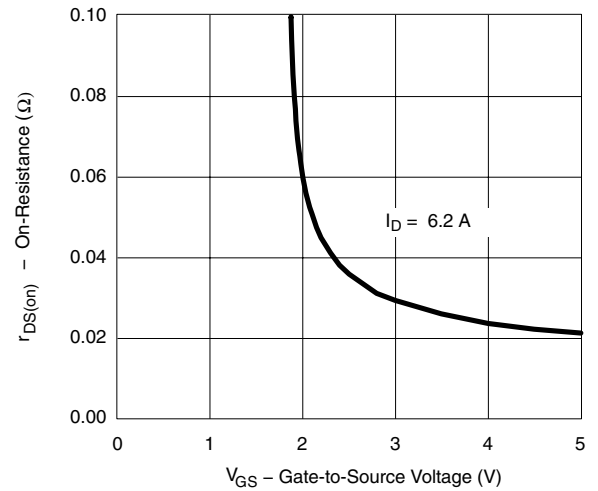
Normalized Thermal Transient Impedance, Junction-to-Foot

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless noted

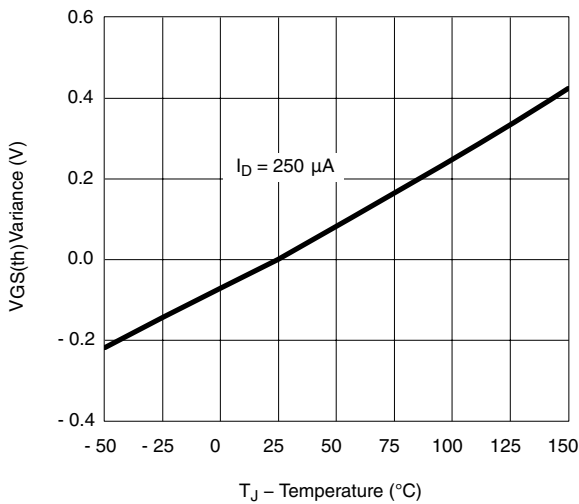
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless noted



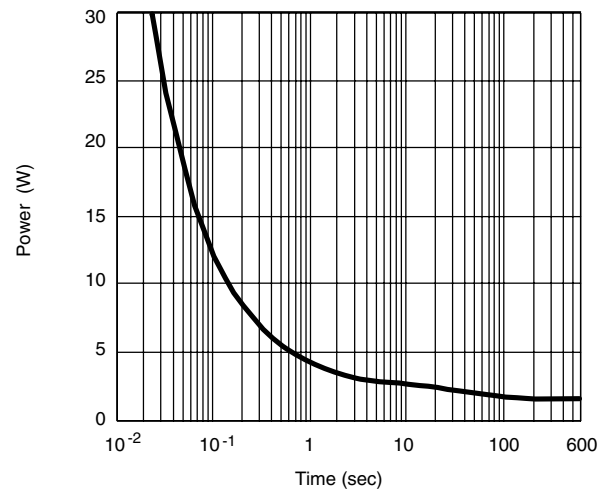
Source-Drain Diode Forward Voltage



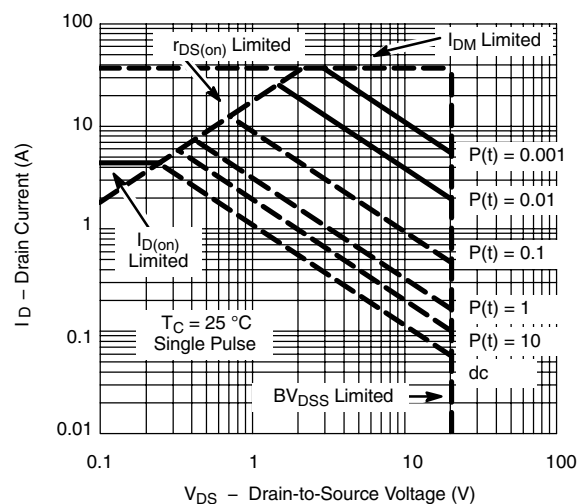
On-Resistance vs. Gate-to-Source Voltage



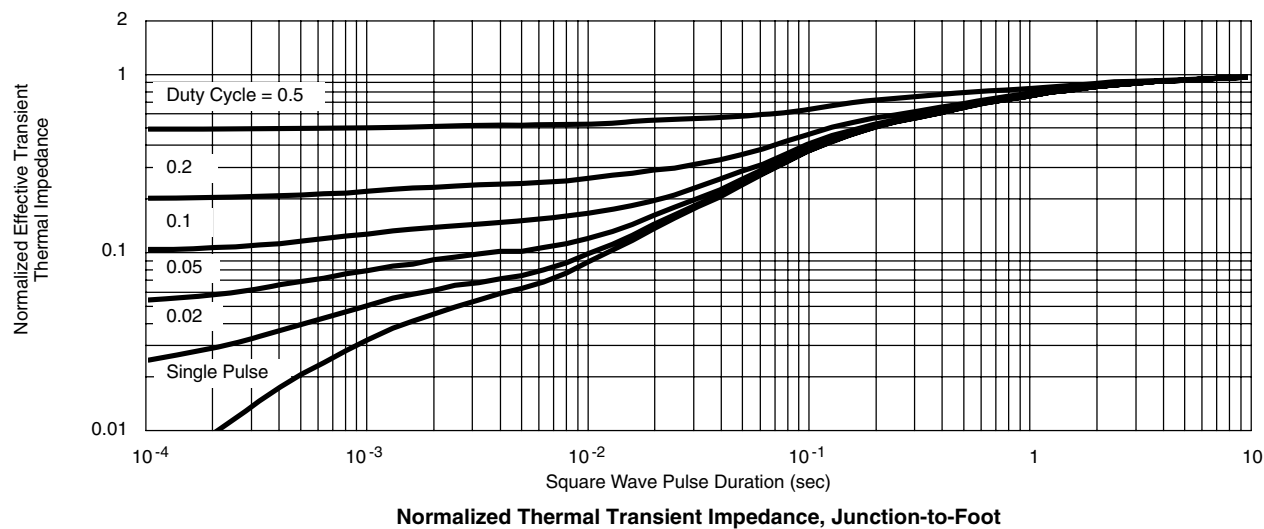
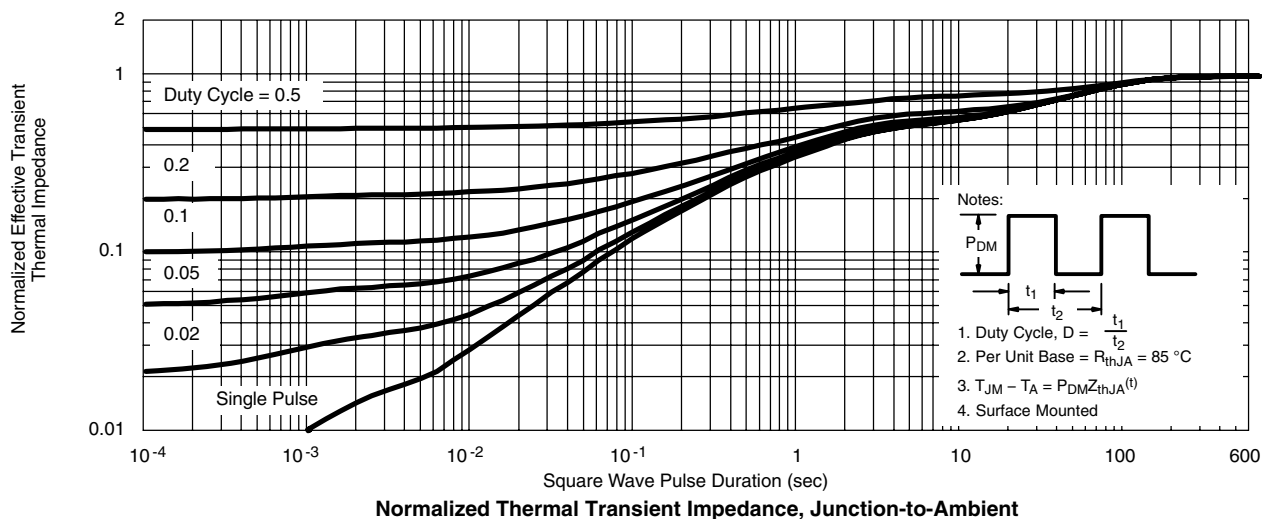
Threshold Voltage



Single Pulse Power



Safe Operating Area

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless noted

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