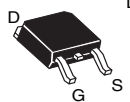
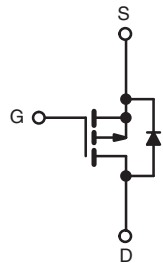
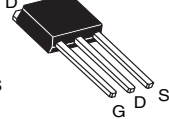




Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	- 50	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10$ V	0.33
Q_g (Max.) (nC)	14	
Q_{gs} (nC)	6.5	
Q_{gd} (nC)	6.5	
Configuration	Single	

DPAK
(TO-252)IPAK
(TO-251)

P-Channel MOSFET

FEATURES

- Surface Mountable (Order as IRFR9022, SiHFR9022)
- Straight Lead Option (Order as IRFU9022, SiHFU9022)
- Repetitive Avalanche Ratings
- Dynamic dV/dt Rating
- Simple Drive Requirements
- Ease of Paralleling

RoHS*
COMPLIANT

DESCRIPTION

The Power MOSFET technology is the key to Vishay's advanced line of Power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dV/dt .

The Power MOSFET transistors also feature all of the well established advantages of MOSFET'S such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

Surface mount packages enhance circuit performance by reducing stray inductances and capacitance. The TO-252 surface mount package brings the advantages of Power MOSFET's to high volume applications where PC Board surface mounting is desirable. The surface mount option IRFR9022, SiHFR9022 is provided on 16 mm tape. The straight lead option IRFU9022, SiHFU9022 of the device is called the IPAK (TO-251).

They are well suited for applications where limited heat dissipation is required such as, computers and peripherals, telecommunication equipment, DC/DC converters, and a wide range of consumer products.

ORDERING INFORMATION

Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free	IRFR9022PbF	IRFR9022TRPbF ^a	IRFR9022TRLPbF ^a	IRFU9022PbF
	SiHFR9022-E3	SiHFR9022T-E3 ^a	SiHFR9022TL-E3 ^a	SiHFU9022-E3
SnPb	IRFR9022	IRFR9022TR ^a	IRFR9022TRL ^a	IRFU9022
	SiHFR9022	SiHFR9022T ^a	SiHFR9022TL ^a	SiHFU9022

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	- 50	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	V_{GS} at - 10 V	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Pulsed Drain Current ^a	I_{DM}	- 36	
Linear Derating Factor		0.33	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^b	E_{AS}	440	mJ
Repetitive Avalanche Current ^a	I_{AR}	- 9.9	A
Repetitive Avalanche Energy ^a	E_{AR}	4.2	mJ
Maximum Power Dissipation	P_D	42	W
Peak Diode Recovery dV/dt ^c	dV/dt	5.8	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 14).

b. $V_{DD} = -25$ V, Starting $T_J = 25^\circ\text{C}$, $L = 5.1$ mH, $R_G = 25\ \Omega$, Peak $I_L = -9.9$ A

c. $I_{SD} \leq -9.9$ A, $dI/dt \leq -120$ A/ μs , $V_{DD} \leq 40$ V, $T_J \leq 150^\circ\text{C}$.

d. 0.063" (1.6 mm) from case.

e. When mounted on 1" square PCB (FR-4 or G-10 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	-	110	°C/W
Case-to-Sink	R_{thCS}	-	1.7	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	3.0	

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA		- 50	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA		- 2.0	-	- 4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 500	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = max. rating, V _{GS} = 0 V		-	-	250	μA
		V _{DS} = 0.8 x max. rating, V _{GS} = 0 V, T _J = 125 °C		-	-	1000	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = - 10 V	I _D = 5.7 A ^b	-	0.28	0.33	Ω
Forward Transconductance	g _{fs}	V _{DS} ≤ - 50 V, I _{DS} = - 5.7 A		2.3	3.5	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = - 25 V, f = 1.0 MHz, see fig. 9		-	490	-	pF
Output Capacitance	C _{oss}			-	320	-	
Reverse Transfer Capacitance	C _{rss}			-	70	-	
Total Gate Charge	Q _g	V _{GS} = - 10 V	I _D = - 9.7 A, V _{DS} = 0.8 x max. rating, see fig. 16 (Independent operating temperature)	-	9.4	14	nC
Gate-Source Charge	Q _{gs}			-	4.3	6.5	
Gate-Drain Charge	Q _{gd}			-	4.3	6.5	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 25 V, I _D = - 9.7 A, R _G = 18 Ω, R _D = 2.4 Ω, see fig. 15 (Independent operating temperature)		-	8.2	12	ns
Rise Time	t _r			-	57	66	
Turn-Off Delay Time	t _{d(off)}			-	12	18	
Fall Time	t _f			-	25	38	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact.		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	- 9.9	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	- 40	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = - 9.9 A, V _{GS} = 0 V ^b		-	-	- 6.3	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = - 9.7 A, dI/dt = 100 A/μs ^b		56	110	280	ns
Body Diode Reverse Recovery Charge	Q _{rr}			0.17	0.34	0.85	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 14).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

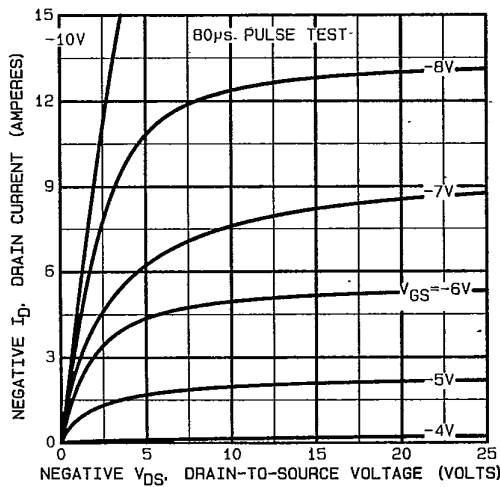


Fig. 1 - Typical Output Characteristics

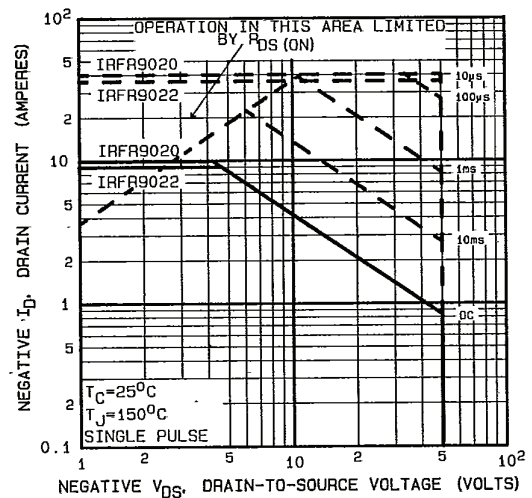


Fig. 4 - Maximum Safe Operating Area

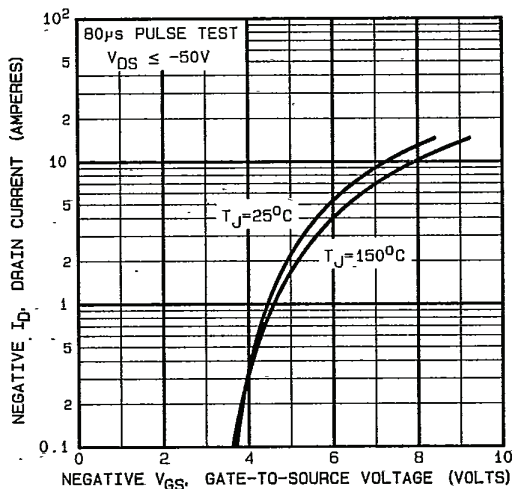


Fig. 2 - Typical Transfer Characteristics

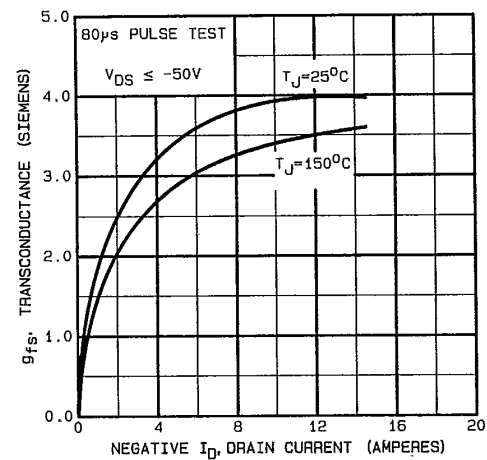


Fig. 5 - Typical Transconductance vs. Drain Current

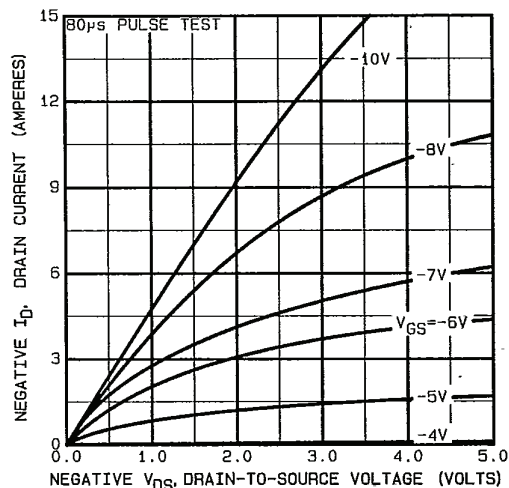


Fig. 3 - Typical Saturation Characteristics

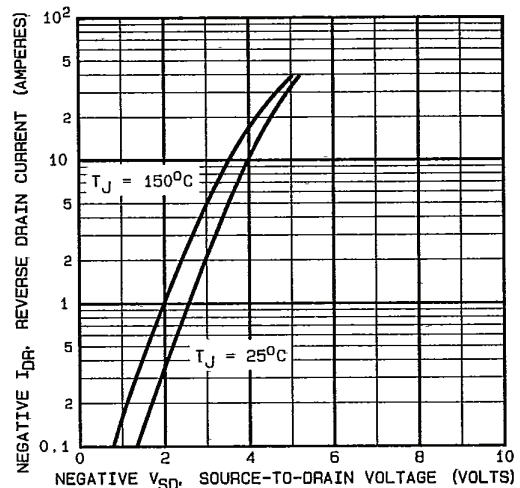
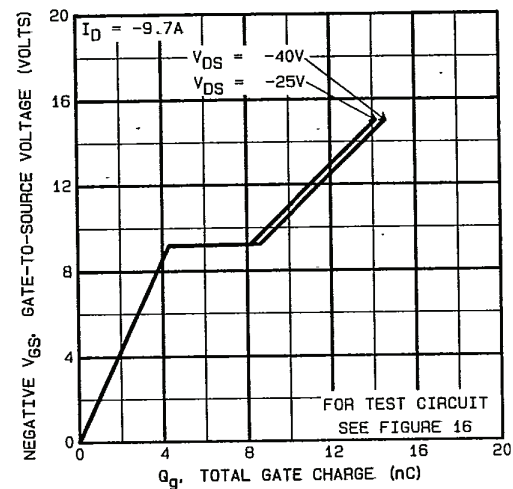
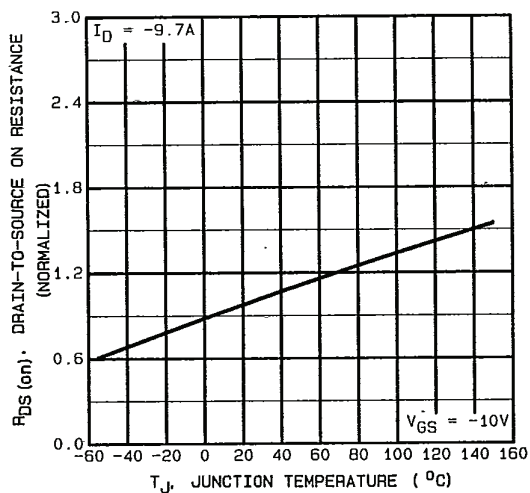
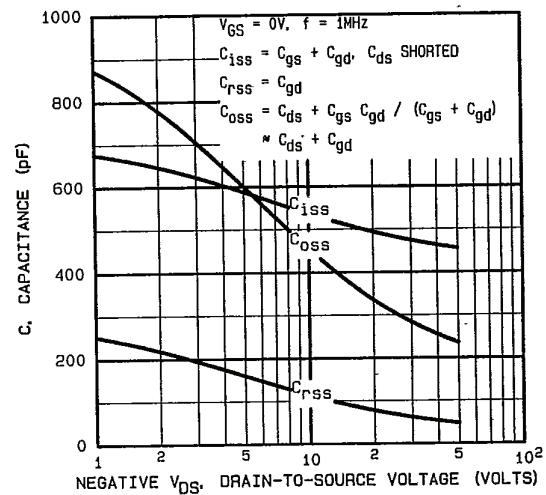
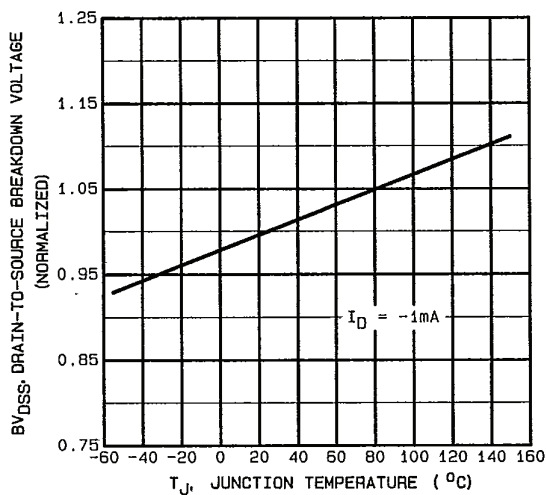


Fig. 6 - Typical Source-Drain Diode Forward Voltage



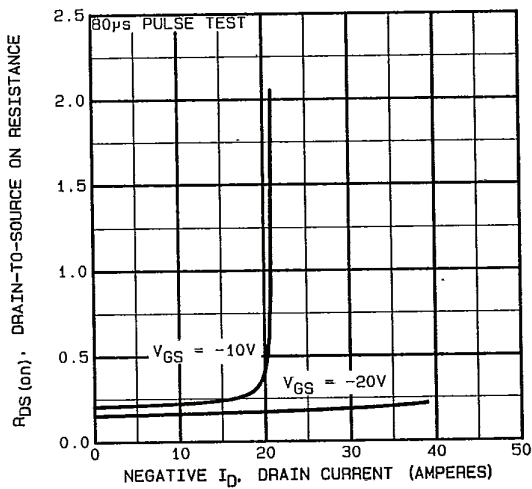


Fig. 11 - Typical On-Resistance vs. Drain Current

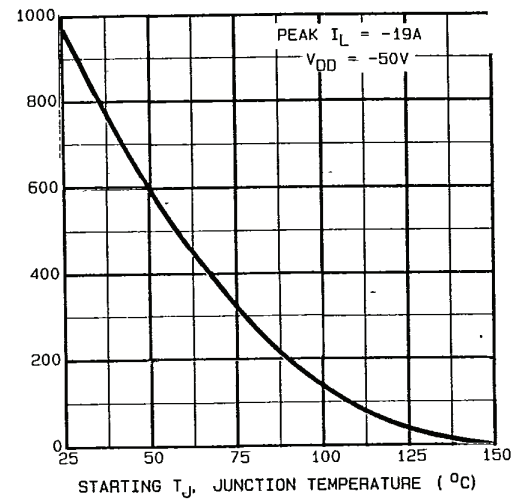


Fig. 13 - Maximum Avalanche vs. Starting Junction Temperature

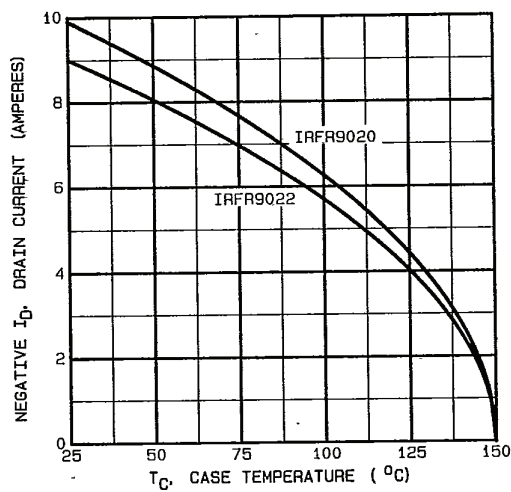


Fig. 12 - Maximum Drain Current vs. Case Temperature

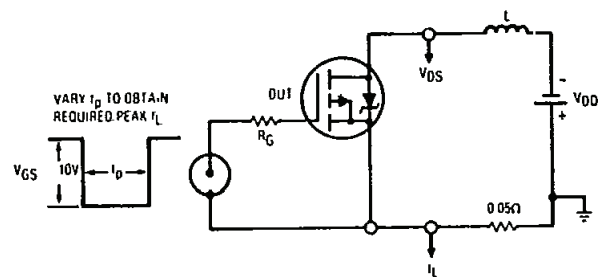


Fig. 13b - Unclamped Inductive Test Circuit

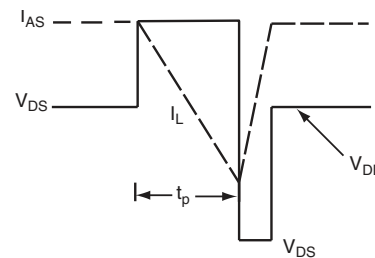


Fig. 13c - Unclamped Inductive Waveforms

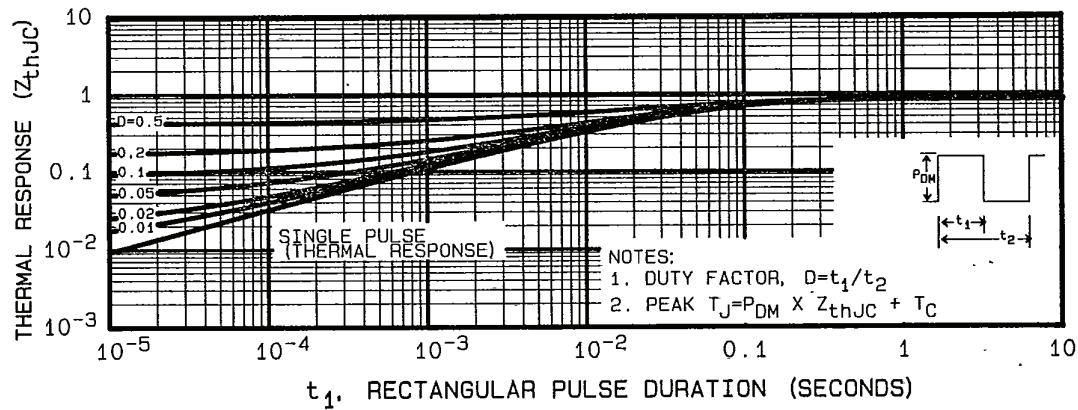


Fig. 14 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

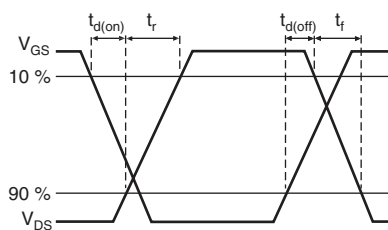


Fig. 15a - Switching Time Waveforms

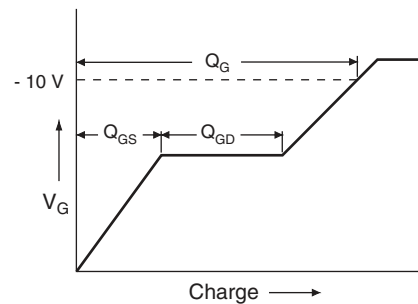


Fig. 16a - Basic Gate Charge Waveform

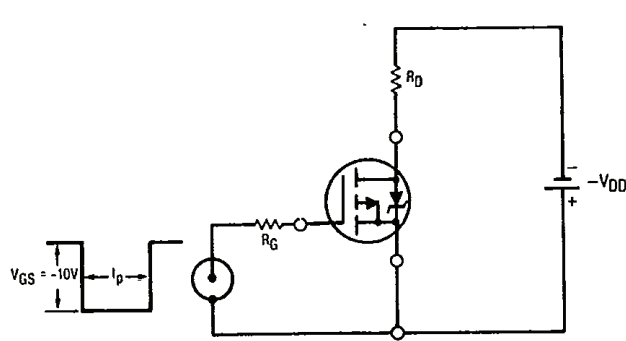


Fig. 15b - Switching Time Test Circuit

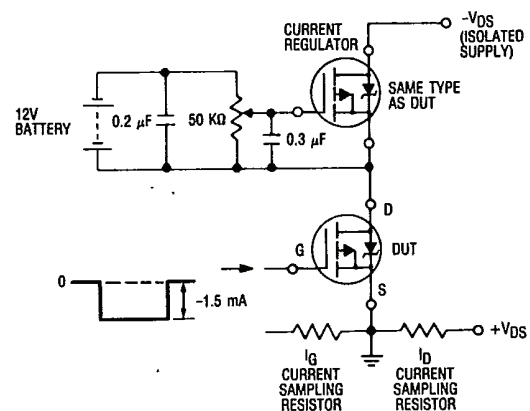
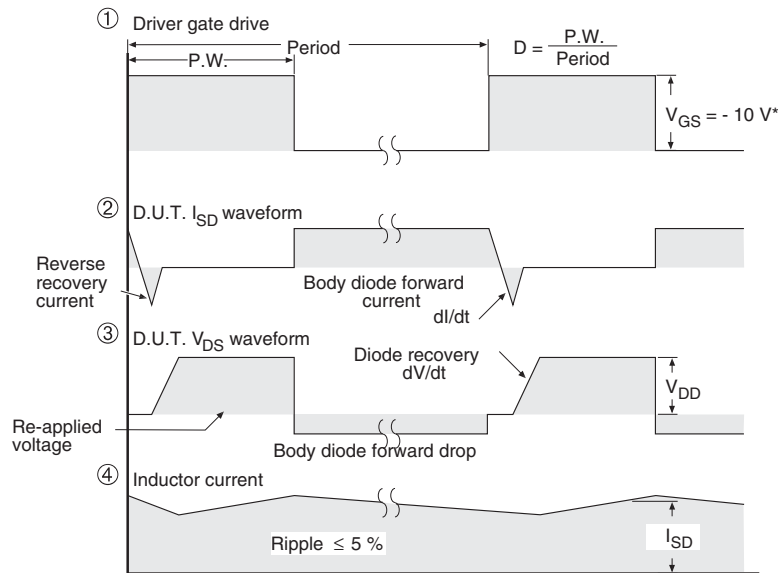
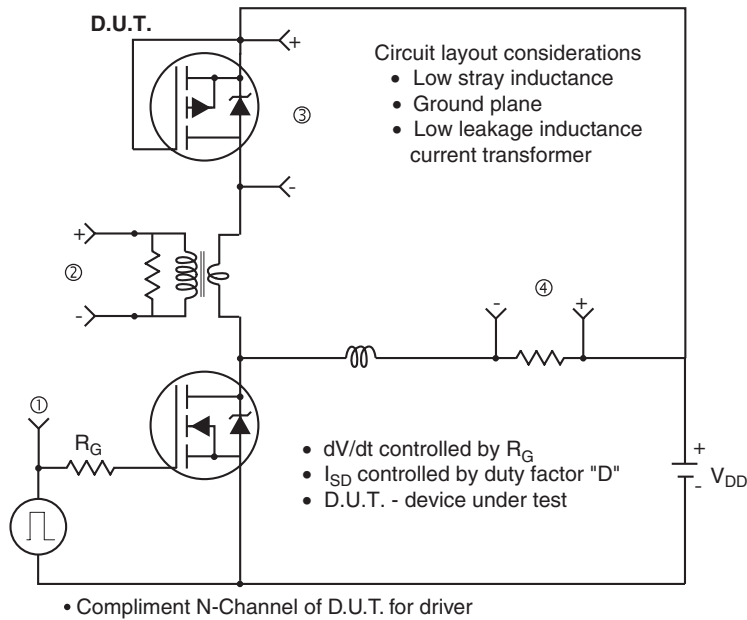


Fig. 16b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = -5\text{ V}$ for logic level and -3 V drive devices

Fig. 17 - For P-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg291349.

TO-252AA (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
E	6.40	6.73	0.252	0.265
L	1.40	1.77	0.055	0.070
L1	2.743 REF		0.108 REF	
L2	0.508 BSC		0.020 BSC	
L3	0.89	1.27	0.035	0.050
L4	0.64	1.01	0.025	0.040
D	6.00	6.22	0.236	0.245
H	9.40	10.40	0.370	0.409
b	0.64	0.88	0.025	0.035
b2	0.77	1.14	0.030	0.045
b3	5.21	5.46	0.205	0.215
e	2.286 BSC		0.090 BSC	
A	2.20	2.38	0.087	0.094
A1	0.00	0.13	0.000	0.005
c	0.45	0.60	0.018	0.024
c2	0.45	0.58	0.018	0.023
D1	5.30	-	0.209	-
E1	4.40	-	0.173	-
θ	0°	10°	0°	10°

ECN: S-81965-Rev. A, 15-Sep-08
DWG: 5973

Notes

1. Package body sizes exclude mold flash, protrusion or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 0.10 mm per side.
2. Package body sizes determined at the outermost extremes of the plastic body exclusive of mold flash, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. The package top may be smaller than the package bottom.
4. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10 mm total in excess of "b" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

TO-251AA (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

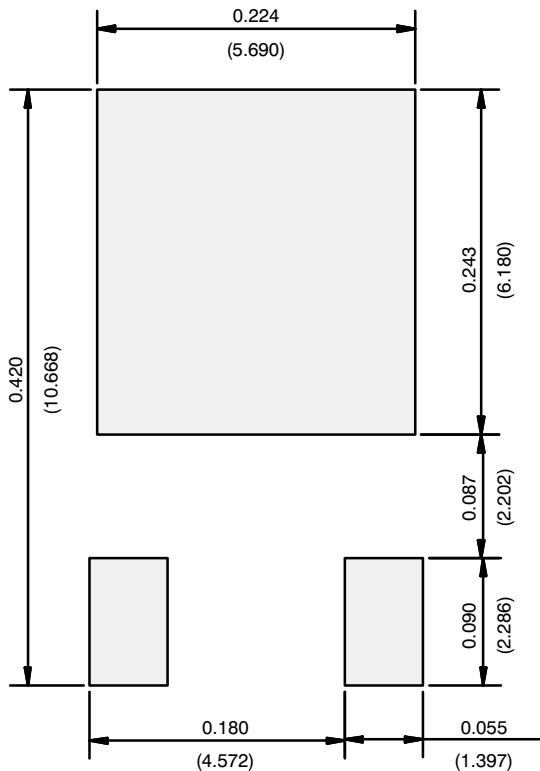
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
θ1	0°	15°	0°	15°
θ2	25°	35°	25°	35°

ECN: S-82111-Rev. A, 15-Sep-08
DWG: 5968

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension are shown in inches and millimeters.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions b4, L2, E1 and D1.
5. Lead dimension uncontrolled in L3.
6. Dimension b1, b3 and c1 apply to base metal only.
7. Outline conforms to JEDEC outline TO-251AA.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.