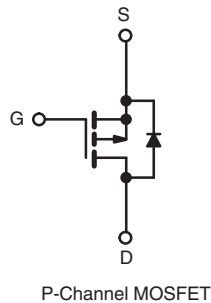
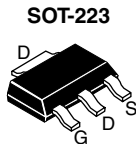


## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	- 60	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = - 10$ V	0.50
$Q_g$ (Max.) (nC)	12	
$Q_{gs}$ (nC)	3.8	
$Q_{gd}$ (nC)	5.1	
Configuration	Single	



### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Available in Tape and Reel
- Dynamic  $dV/dt$  Rating
- Repetitive Avalanche Rated
- P-Channel
- Fast Switching
- Ease of Paralleling
- Compliant to RoHS Directive 2002/95/EC



Available  
**RoHS\***  
 COMPLIANT  
**HALOGEN**  
**FREE**  
 Available

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mounting using vapor phase, infrared, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25 W is possible in a typical surface mount application.

ORDERING INFORMATION		
Package	SOT-223	SOT-223
Lead (Pb)-free and Halogen-free	SiHFL9014-GE3	-
Lead (Pb)-free	IRFL9014PbF	IRFL9014TRPbF <sup>a</sup>
	SiHFL9014-E3	SiHFL9014T-E3 <sup>a</sup>
SnPb	IRFL9014	IRFL9014TR <sup>a</sup>
	SiHFL9014	SiHFL9014T <sup>a</sup>

#### Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	- 60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current	$V_{GS}$ at - 10 V	$T_C = 25$ °C	- 1.8
		$T_C = 100$ °C	- 1.1
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	- 14	A
Linear Derating Factor		0.025	
Linear Derating Factor (PCB Mount) <sup>e</sup>		0.017	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	140	mJ
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	- 1.8	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	0.31	mJ

\* Pb containing terminations are not RoHS compliant, exemptions may apply

<b>ABSOLUTE MAXIMUM RATINGS</b> ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	3.1	W
Maximum Power Dissipation (PCB Mount) <sup>e</sup>	$T_A = 25\text{ }^\circ\text{C}$		2.0	
Peak Diode Recovery $dV/dt^c$		$dV/dt$	- 4.5	V/ns
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>	

**Notes**

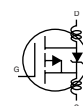
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b.  $V_{DD} = -25\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 50\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = -1.8\text{ A}$  (see fig. 12).
- c.  $I_{SD} \leq -6.7\text{ A}$ ,  $dI/dt \leq 90\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- d. 1.6 mm from case.
- e. When mounted on 1" square PCB (FR-4 or G-10 material).


<b>THERMAL RESISTANCE RATINGS</b>				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	60	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	40	

**Note**

- a. When mounted on 1" square PCB (FR-4 or G-10 material).

<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	- 60	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$	-	- 0.059	-	$\text{V}/^\circ\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	- 2.0	-	- 4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -60\text{ V}$ , $V_{GS} = 0\text{ V}$	-	-	- 100	$\mu\text{A}$
		$V_{DS} = -48\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^\circ\text{C}$	-	-	- 500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$ , $I_D = 1.1\text{ A}^b$	-	-	0.50	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = -25\text{ V}$ , $I_D = 1.1\text{ A}^b$	1.3	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 5	-	270	-	pF
Output Capacitance	$C_{oss}$		-	170	-	
Reverse Transfer Capacitance	$C_{rss}$		-	31	-	
Total Gate Charge	$Q_g$	$V_{GS} = -10\text{ V}$ , $I_D = -6.7\text{ A}$ , $V_{DS} = -48\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	12	nC
Gate-Source Charge	$Q_{gs}$		-	-	3.8	
Gate-Drain Charge	$Q_{gd}$		-	-	5.1	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -30\text{ V}$ , $I_D = -6.7\text{ A}$ , $R_g = 24\text{ }\Omega$ , $R_D = 4.0\text{ }\Omega$ , see fig. 10 <sup>b</sup>	-	11	-	ns
Rise Time	$t_r$		-	63	-	
Turn-Off Delay Time	$t_{d(off)}$		-	9.6	-	
Fall Time	$t_f$		-	31	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact	-	4.0	-	nH
Internal Source Inductance	$L_S$		-	6.0	-	

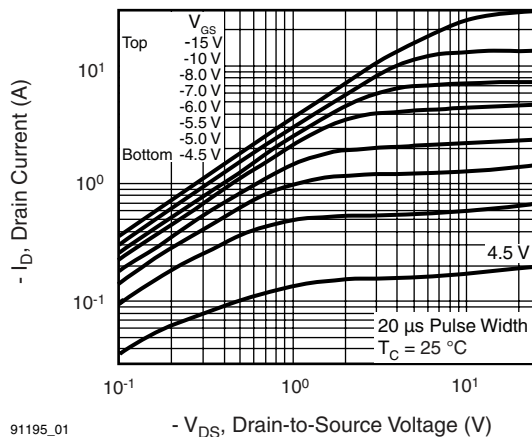


SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	- 1.8	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	- 14	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_S = -1.8\text{ A}$ , $V_{GS} = 0\text{ V}^b$	-	-	- 5.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_F = -6.7\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}^b$	-	80	160	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	0.096	0.19	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

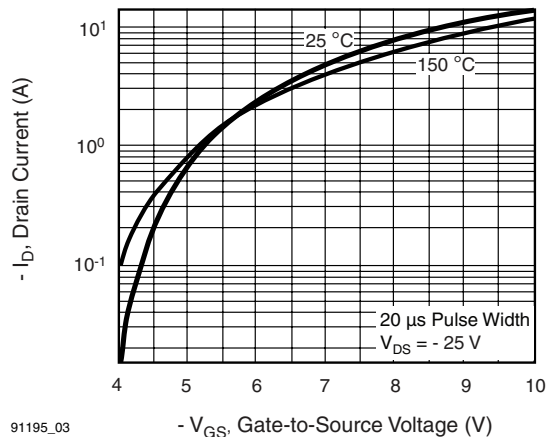
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

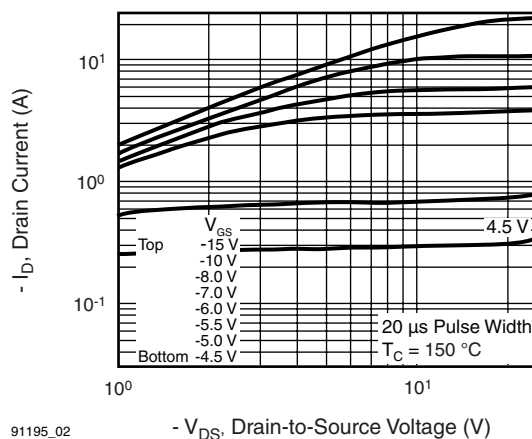
**TYPICAL CHARACTERISTICS ( $25\text{ }^\circ\text{C}$ , unless otherwise noted)**



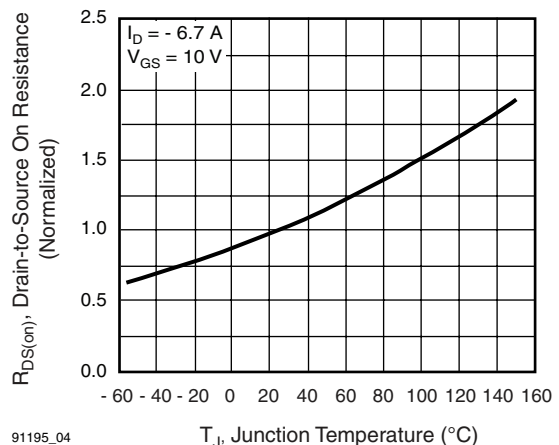
**Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

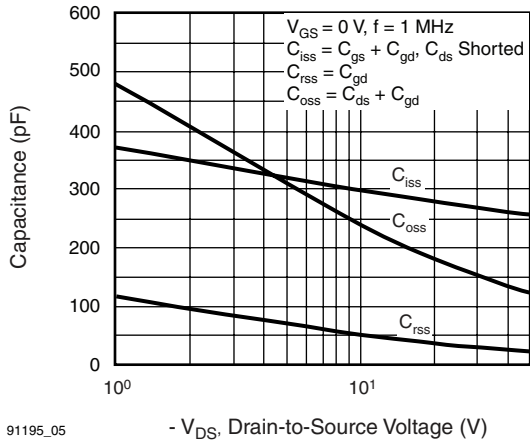


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

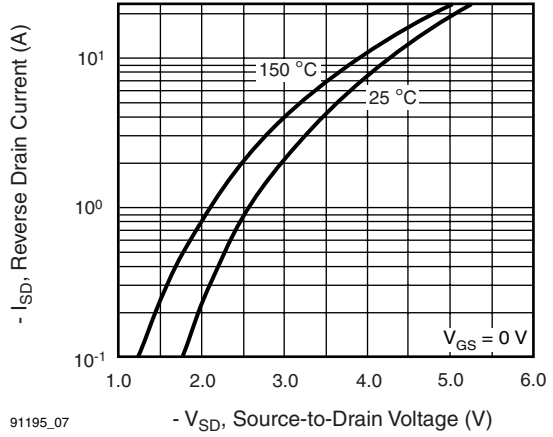


Fig. 7 - Typical Source-Drain Diode Forward Voltage

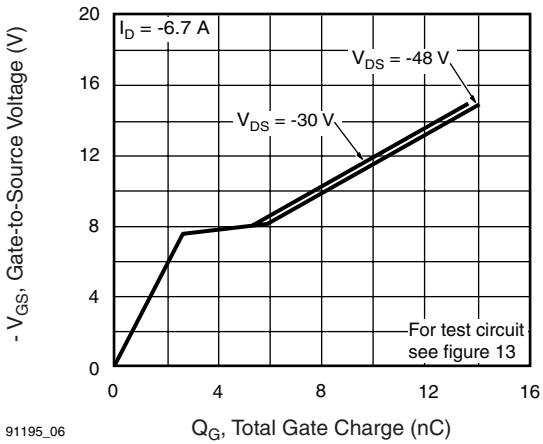


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

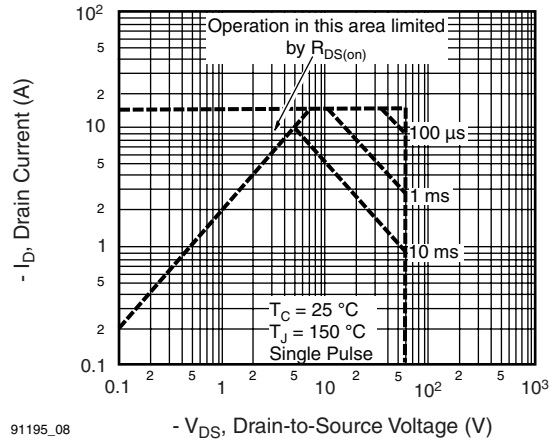
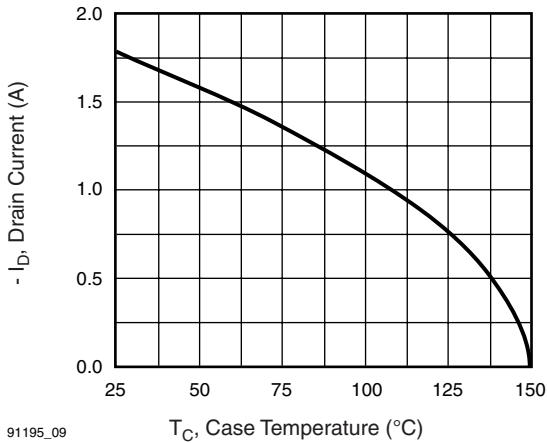
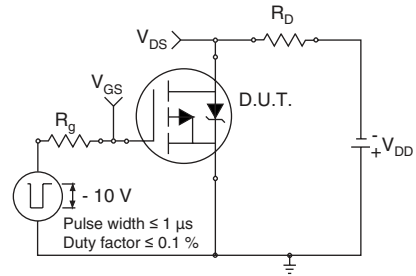


Fig. 8 - Maximum Safe Operating Area

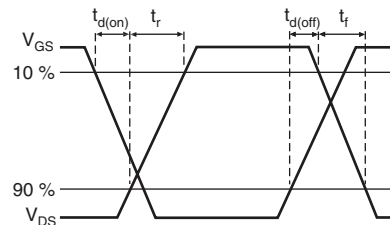


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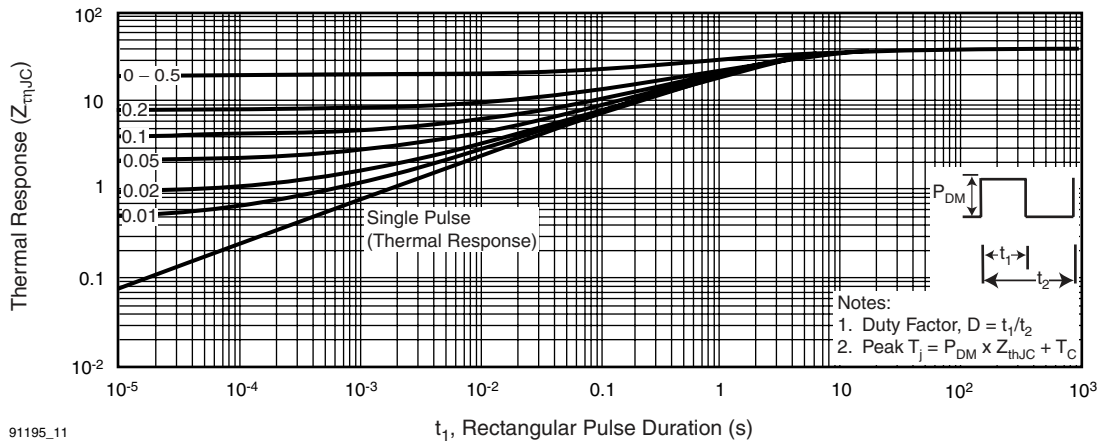
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



**Fig. 10a - Switching Time Test Circuit**



**Fig. 10b - Switching Time Waveforms**



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**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

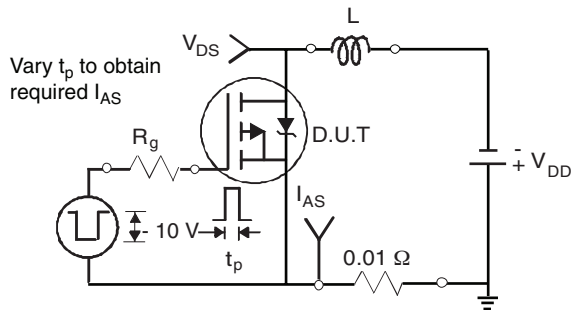


Fig. 12a - Unclamped Inductive Test Circuit

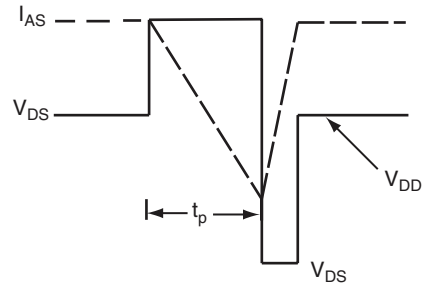


Fig. 12b - Unclamped Inductive Waveforms

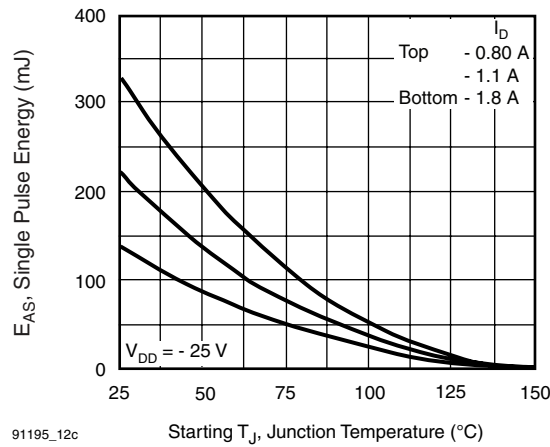


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

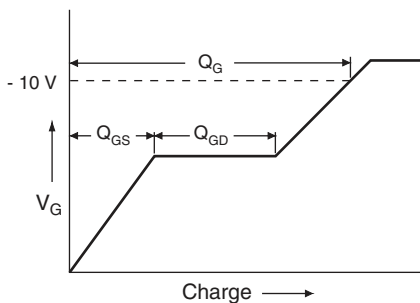


Fig. 13a - Basic Gate Charge Waveform

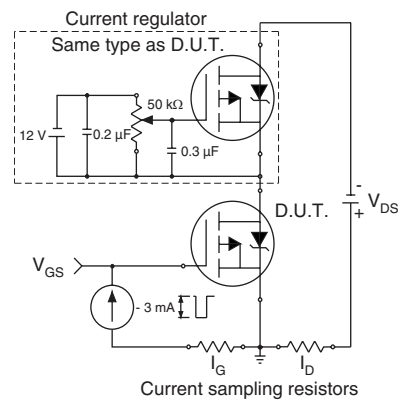
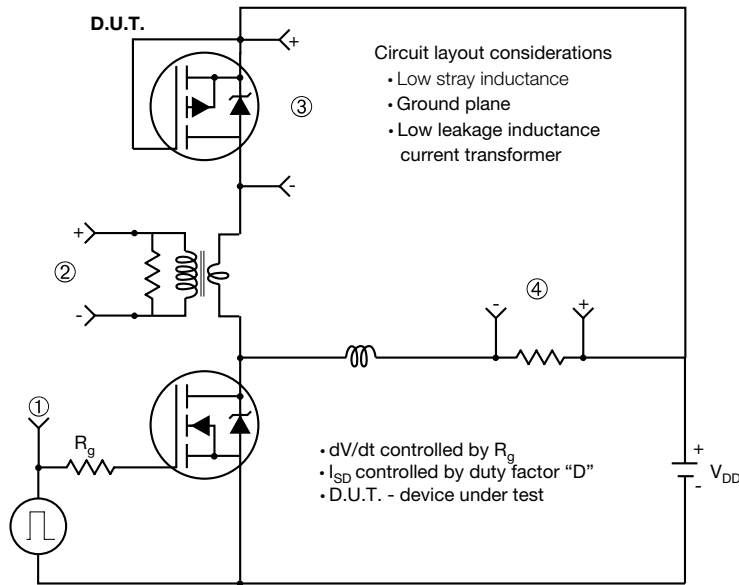
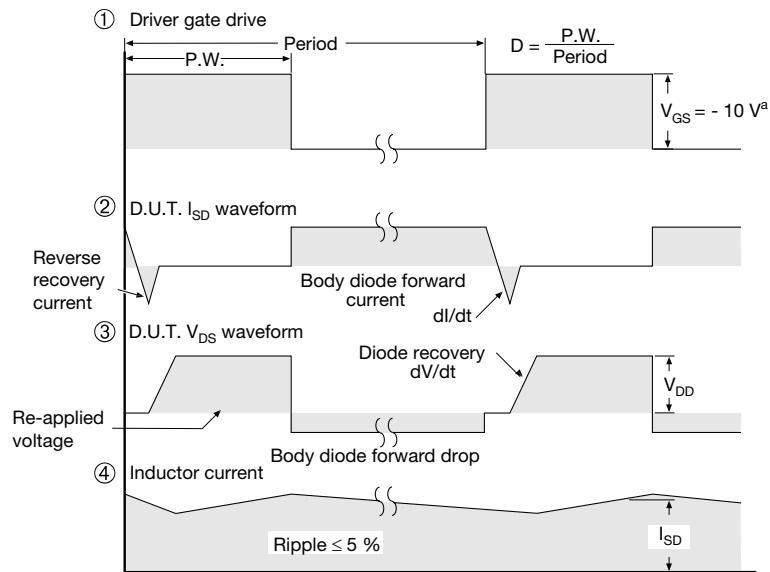


Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery dV/dt Test Circuit



**Note**  
• Compliment N-Channel of D.U.T. for driver



**Note**  
a.  $V_{GS} = -5\text{ V}$  for logic level and  $-3\text{ V}$  drive devices

**Fig.14 - For P-Channel**

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