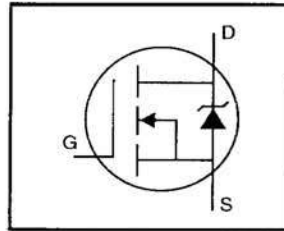


IRL640PbF

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Logic-Level Gate Drive
- RDS(on) Specified at VGS=4V & 5V
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead-Free

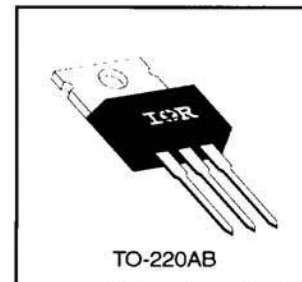


$V_{DSS} = 200V$
$R_{DS(on)} = 0.18\Omega$
$I_D = 17A$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



Absolute Maximum Ratings

Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	17	A
$I_D @ T_C = 100^\circ C$	11	
I_{DM}	68	
$P_D @ T_C = 25^\circ C$	125	W
	1.0	W/°C
V_{GS}	±10	V
E_{AS}	580	mJ
I_{AR}	10	A
E_{AR}	13	mJ
dv/dt	5.0	V/ns
T_J	-55 to +150	°C
T_{STG}		
	300 (1.6mm from case)	
	10 lbf•in (1.1 N•m)	


Thermal Resistance

Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	—	—	1.0	°C/W
$R_{\theta CS}$	—	0.50	—	
$R_{\theta JA}$	—	—	62	


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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Parameter	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	200	—	—	V	V _{GS} =0V, I _D =250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.27	—	V/°C	Reference to 25°C, I _D =1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.18	Ω	V _{GS} =5.0V, I _D =10A ④
		—	—	0.27		V _{GS} =4.0V, I _D =8.5A ④
V _{GS(th)}	Gate Threshold Voltage	1.0	—	2.0	V	V _{DS} =V _{GS} , I _D =250μA
g _{fs}	Forward Transconductance	16	—	—	S	V _{DS} =50V, I _D =10A ④
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} =200V, V _{GS} =0V
		—	—	250		V _{DS} =160V, V _{GS} =0V, T _J =125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} =10V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} =-10V
Q _g	Total Gate Charge	—	—	66	nC	I _D =17A
Q _{gs}	Gate-to-Source Charge	—	—	9.0		V _{DS} =160V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	38		V _{GS} =5.0V See Fig. 6 and 13 ④
t _{d(on)}	Turn-On Delay Time	—	8.0	—	ns	V _{DD} =100V
t _r	Rise Time	—	83	—		I _D =17A
t _{d(off)}	Turn-Off Delay Time	—	44	—		R _G =4.6Ω
t _f	Fall Time	—	52	—		R _D =5.7Ω See Figure 10 ④
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	1800	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	400	—		V _{DS} =25V
C _{rss}	Reverse Transfer Capacitance	—	120	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

Parameter	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	17	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	68		
V _{SD}	Diode Forward Voltage	—	—	2.0	V	T _J =25°C, I _S =17A, V _{GS} =0V ④
t _{rr}	Reverse Recovery Time	—	310	470	ns	T _J =25°C, I _F =17A
Q _{rr}	Reverse Recovery Charge	—	3.2	4.8	μC	di/dt=100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V_{DD}=50V, starting T_J=25°C, L=3.0mH R_G=25Ω, I_{AS}=17A (See Figure 12)
- ③ I_{SD}≤17A, di/dt≤150A/μs, V_{DD}≤V_{(BR)DSS}, T_J≤150°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.

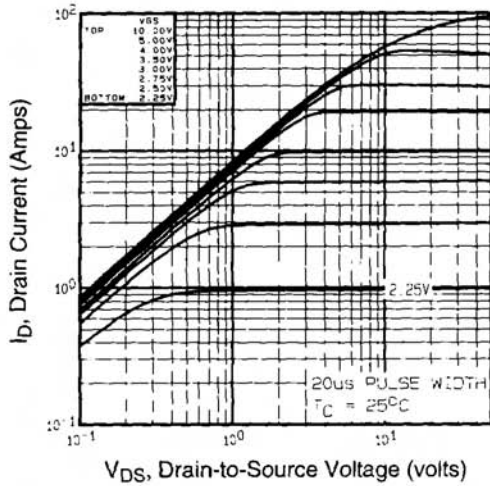


Fig 1. Typical Output Characteristics,
 $T_C=25^\circ\text{C}$

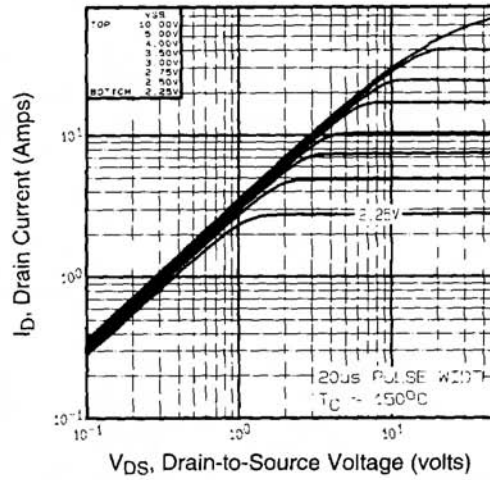


Fig 2. Typical Output Characteristics,
 $T_C=150^\circ\text{C}$

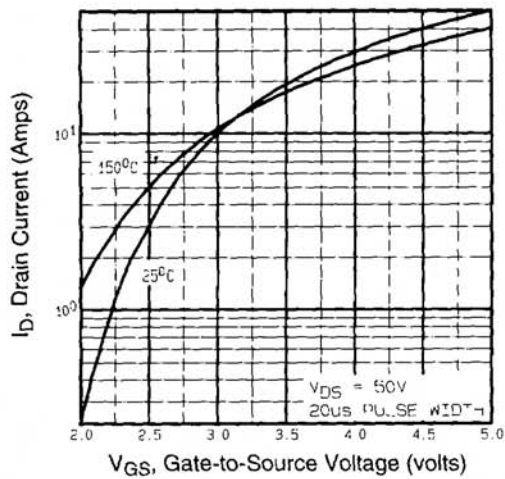


Fig 3. Typical Transfer Characteristics

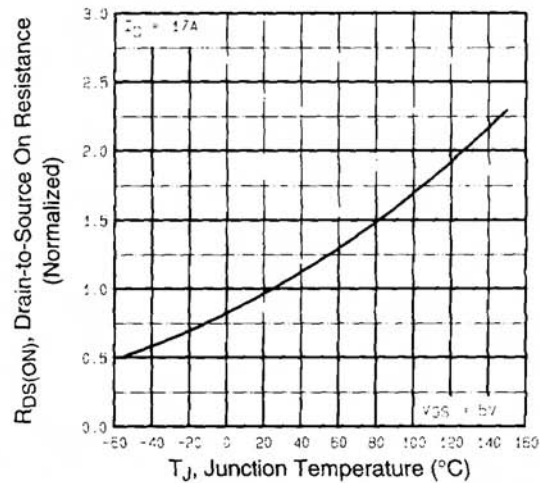


Fig 4. Normalized On-Resistance
 Vs. Temperature

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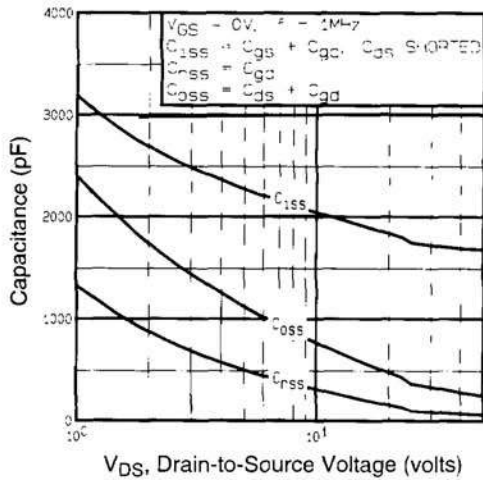


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

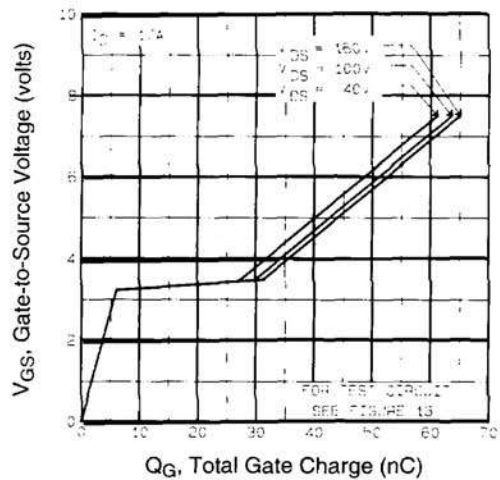


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

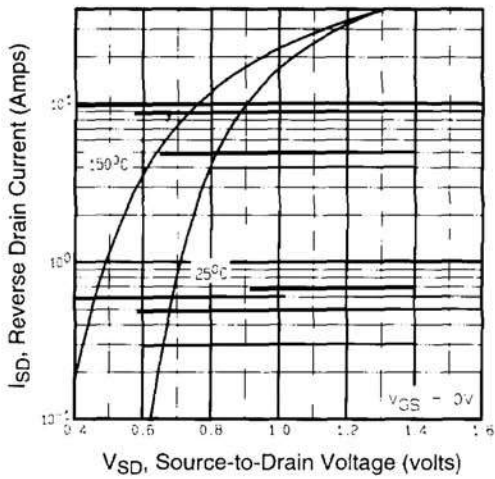


Fig 7. Typical Source-Drain Diode Forward Voltage

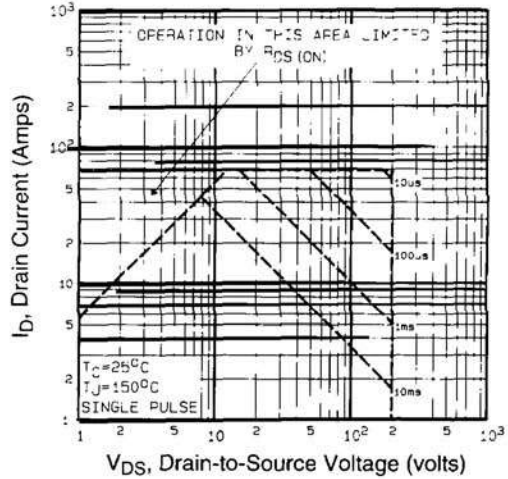


Fig 8. Maximum Safe Operating Area

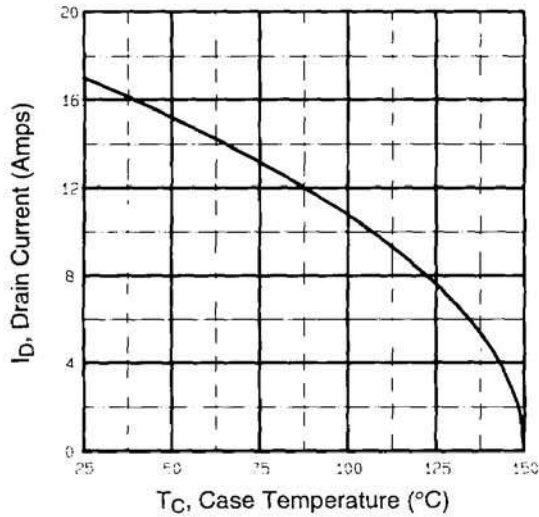


Fig 9. Maximum Drain Current Vs. Case Temperature

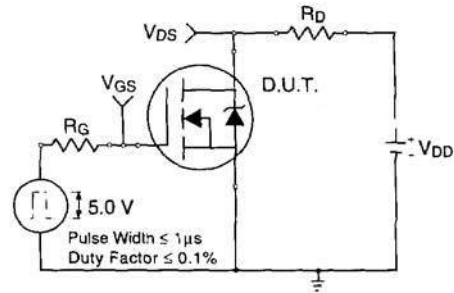


Fig 10a. Switching Time Test Circuit

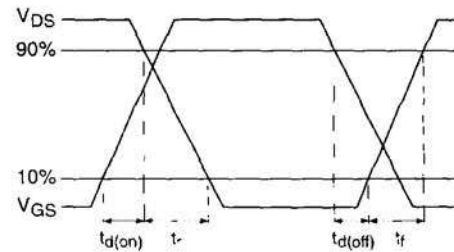


Fig 10b. Switching Time Waveforms

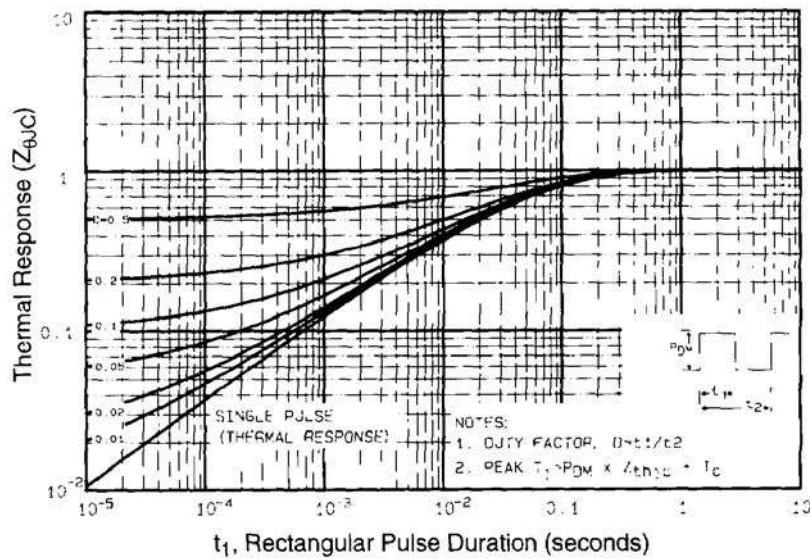


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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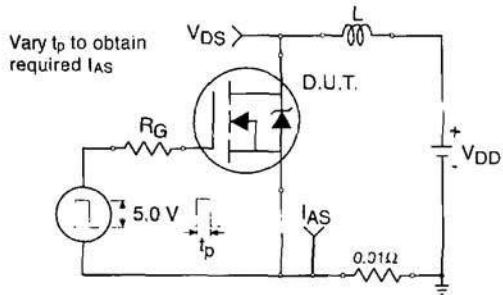


Fig 12a. Unclamped Inductive Test Circuit

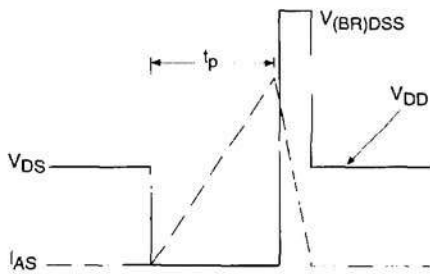


Fig 12b. Unclamped Inductive Waveforms

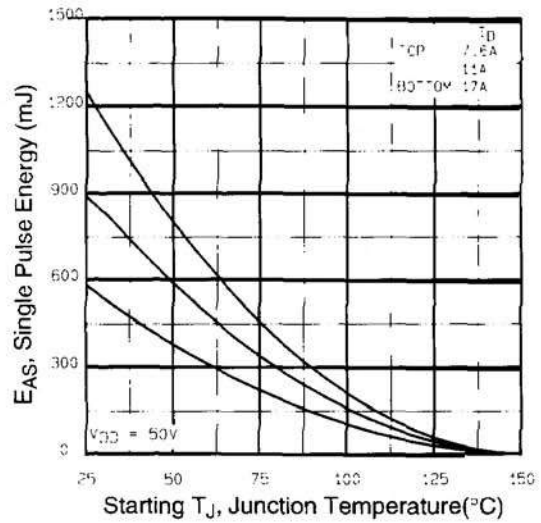


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

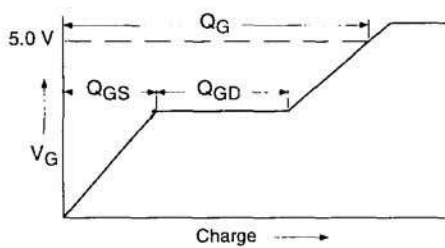


Fig 13a. Basic Gate Charge Waveform

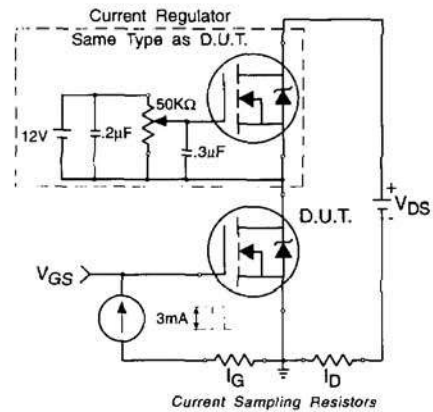


Fig 13b. Gate Charge Test Circuit

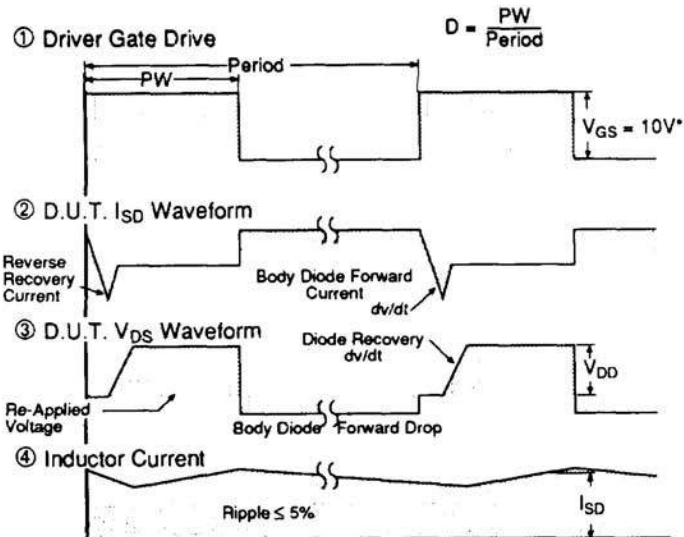
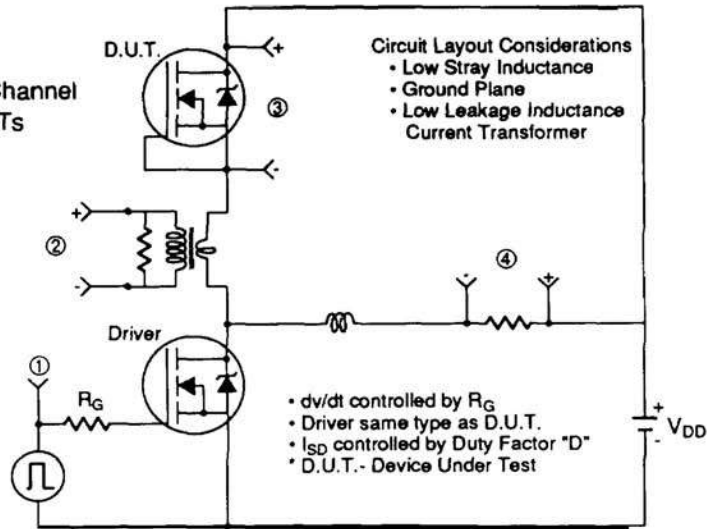
Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit

Appendix B: Package Outline Mechanical Drawing

Appendix A

Peak Diode Recovery dv/dt Test Circuit

Fig 14. For N-Channel HEXFETs



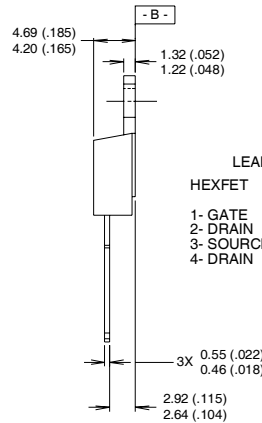
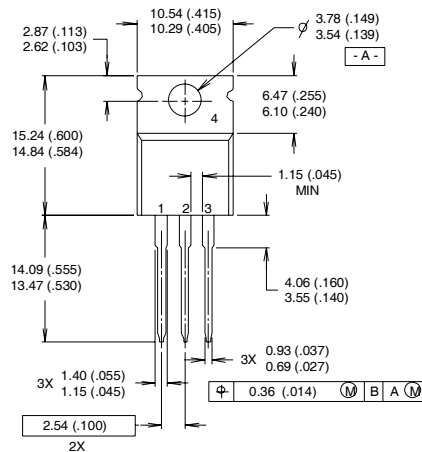
* V_{GS} = 5V for Logic Level Devices

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TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



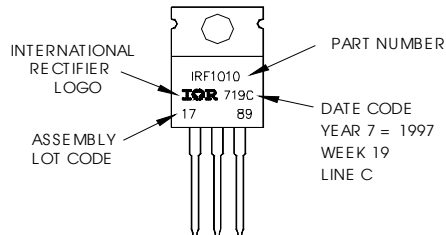
LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK
1- GATE	1- GATE
2- DRAIN	2- COLLECTOR
3- SOURCE	3- EMITTER
4- DRAIN	4- COLLECTOR

- NOTES:
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
 - 2 CONTROLLING DIMENSION : INCH
 - 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
 - 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"
Note: "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.



IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
 TAC Fax: (310) 252-7903
 01/04



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