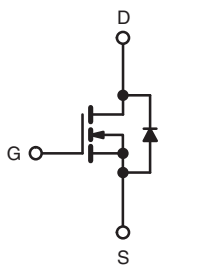
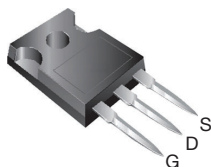


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	900	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	1.6
Q_g (Max.) (nC)	200	
Q_{gs} (nC)	24	
Q_{gd} (nC)	110	
Configuration	Single	

TO-247AC


N-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC


RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247AC package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220AB devices. The TO-247AC is similar but superior to the earlier TO-218 package because its isolated mounting hole. It also provides greater creepage distances between pins to meet the requirements of most safety specifications.

ORDERING INFORMATION

Package	TO-247AC
Lead (Pb)-free	IRFPF50PbF
	SiHFPF50-E3
SnPb	IRFPF50
	SiHFPF50

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	900	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25\text{ }^{\circ}\text{C}$	A
		$T_C = 100\text{ }^{\circ}\text{C}$	
Pulsed Drain Current ^a	I_{DM}	27	
Linear Derating Factor		1.5	W/ $^{\circ}\text{C}$
Single Pulse Avalanche Energy ^b	E_{AS}	880	mJ
Repetitive Avalanche Current ^a	I_{AR}	6.7	A
Repetitive Avalanche Energy ^a	E_{AR}	19	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	190
Peak Diode Recovery dV/dt ^c	dV/dt	1.5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^{\circ}\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

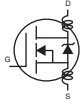
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 37\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 6.7\text{ A}$ (see fig. 12).
- $I_{SD} \leq 6.7\text{ A}$, $dI/dt \leq 130\text{ A}/\mu\text{s}$, $V_{DD} \leq 600$, $T_J \leq 150\text{ }^{\circ}\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

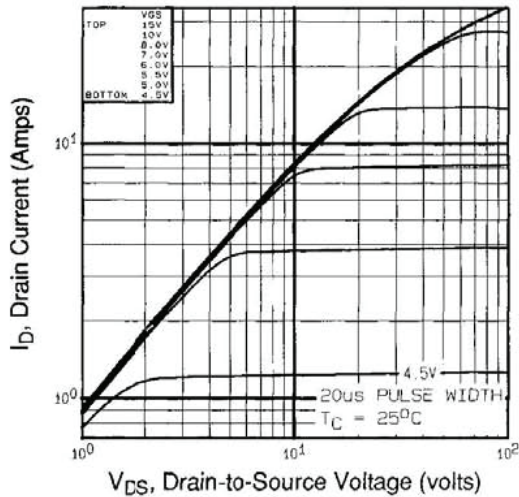
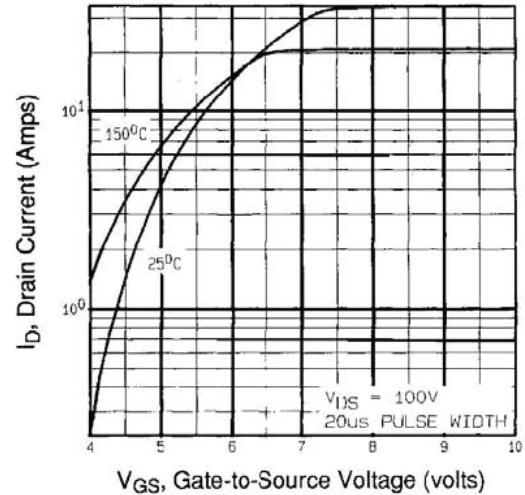
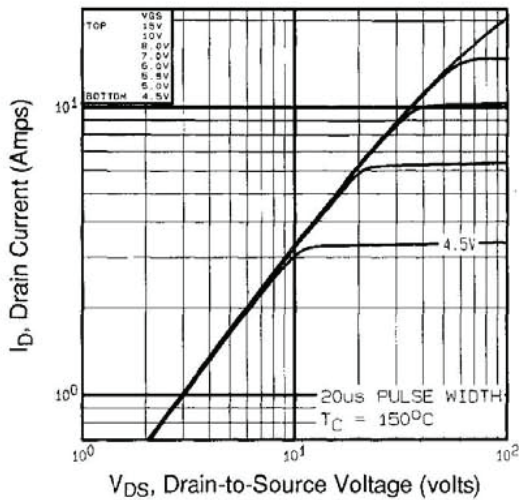
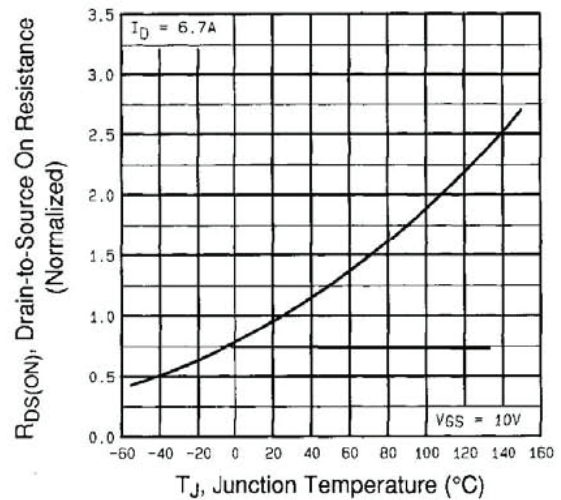
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.65	

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT		
Static									
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		900	-	-	V		
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	1.2	-	V/°C		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V		
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 900 V, V _{GS} = 0 V		-	-	100	μA		
		V _{DS} = 720 V, V _{GS} = 0 V, T _J = 125 °C		-	-	500			
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 4.0 A ^b	-	-	1.6	Ω		
Forward Transconductance	g _{fs}	V _{DS} = 100 V, I _D = 4.0 A ^b		4.9	-	-	S		
Dynamic									
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	2900	-	pF		
Output Capacitance	C _{oss}			-	270	-			
Reverse Transfer Capacitance	C _{rss}			-	92	-			
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 6.7 A, V _{DS} = 360 V, see fig. 6 and 13 ^b	-	-	200	nC		
Gate-Source Charge	Q _{gs}			-	-	24			
Gate-Drain Charge	Q _{gd}			-	-	110			
Turn-On Delay Time	t _{d(on)}	V _{DD} = 450 V, I _D = 6.7 A , R _G = 6.2 Ω, R _D = 67 Ω, see fig. 10 ^b		-	20	-	ns		
Rise Time	t _r			-	34	-			
Turn-Off Delay Time	t _{d(off)}			-	130	-			
Fall Time	t _f			-	37	-			
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact				-	5.0	-	nH
Internal Source Inductance	L _S					-	13	-	
Drain-Source Body Diode Characteristics									
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode				-	-	6.7	A
Pulsed Diode Forward Current ^a	I _{SM}					-	-	27	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 6.7 A, V _{GS} = 0 V ^b		-	-	1.8	V		
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 6.7 A, dI/dt = 100 A/μs ^b		-	610	920	ns		
Body Diode Reverse Recovery Charge	Q _{rr}			-	3.2	4.8	μC		
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)							

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

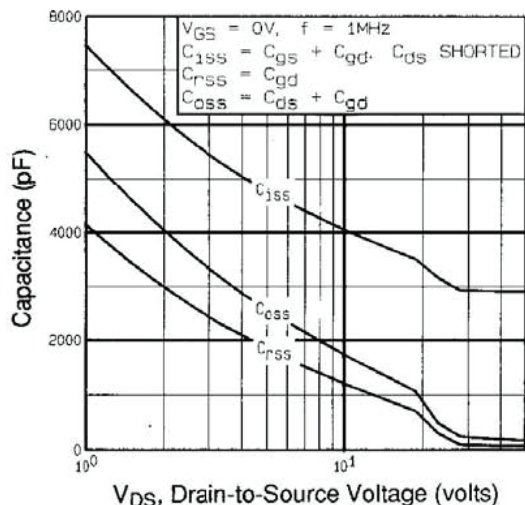


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

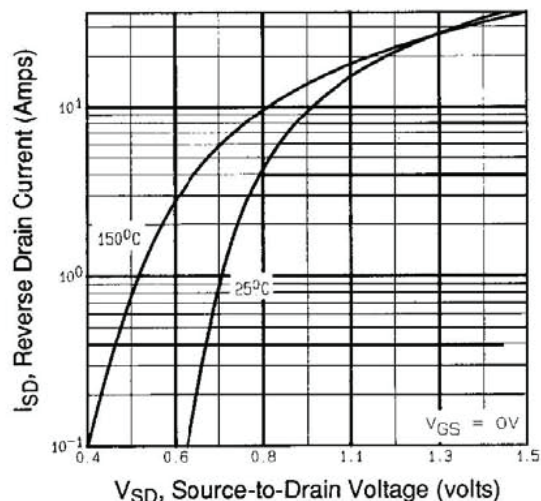


Fig. 7 - Typical Source-Drain Diode Forward Voltage

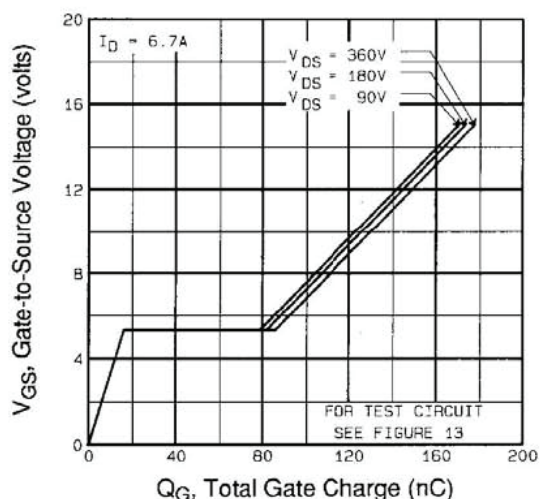


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

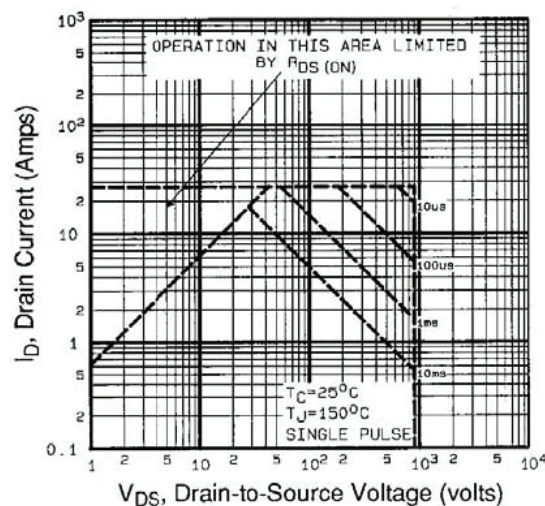


Fig. 8 - Maximum Safe Operating Area

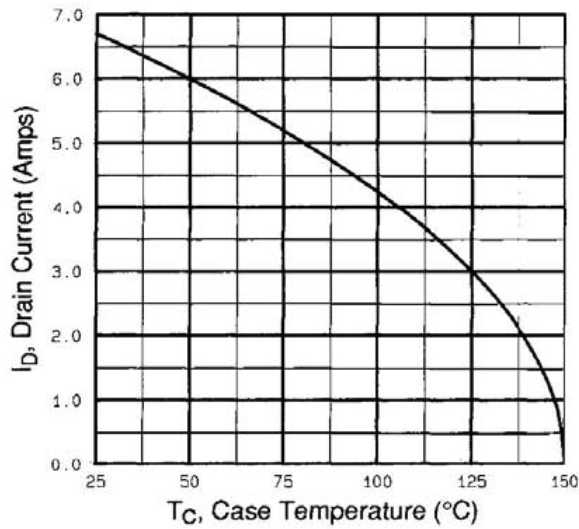


Fig. 9 - Maximum Drain Current vs. Case Temperature

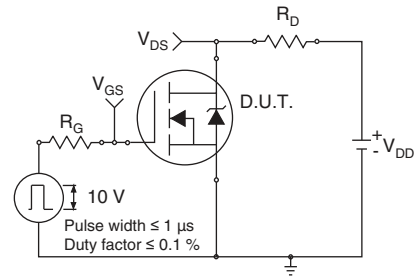


Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms

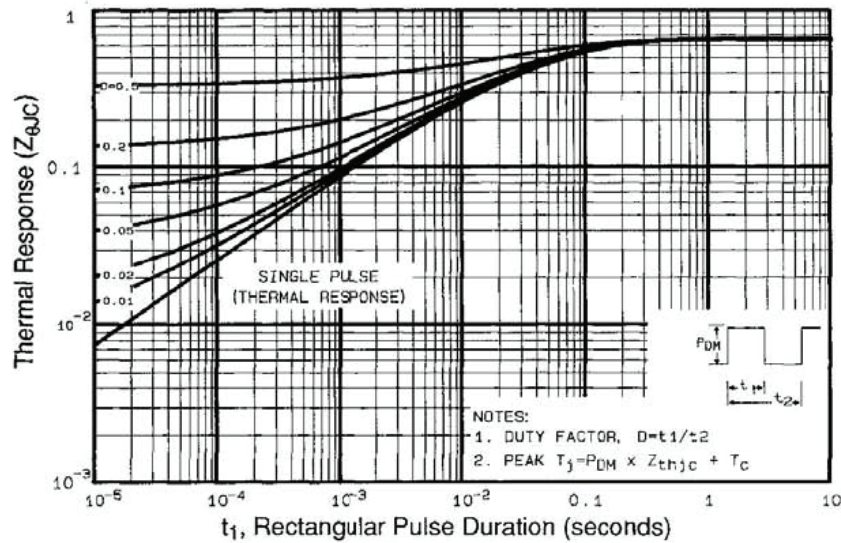


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

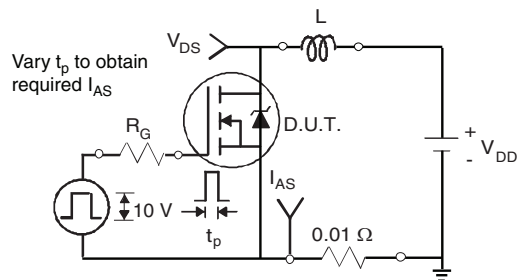


Fig. 12a - Unclamped Inductive Test Circuit

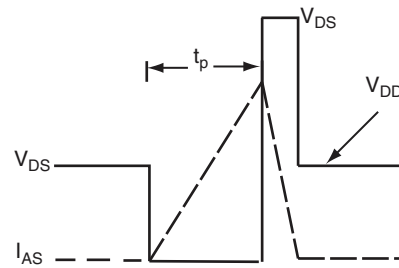


Fig. 12b - Unclamped Inductive Waveforms

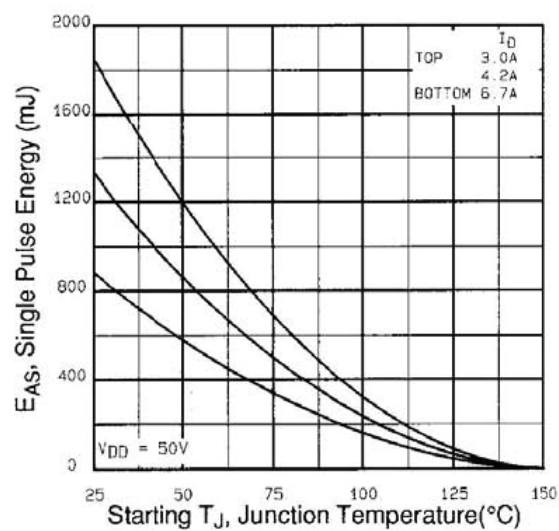


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

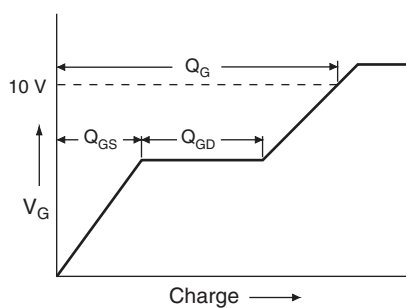


Fig. 13a - Basic Gate Charge Waveform

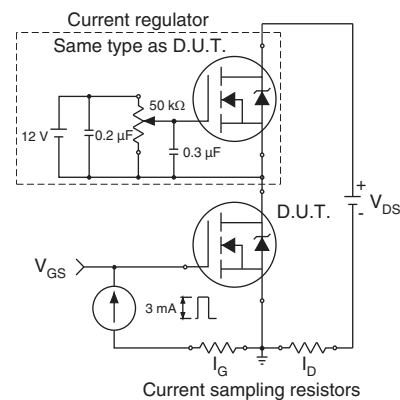


Fig. 13b - Gate Charge Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91251.



TO-247AC (High Voltage)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

ECN: X13-0103-Rev. D, 01-Jul-13
DWG: 5971

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
Ø k	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
Ø P	3.51	3.66	0.138	0.144
Ø P1	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Contour of slot optional.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions D1 and E1.
5. Lead finish uncontrolled in L1.
6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
7. Outline conforms to JEDEC outline TO-247 with exception of dimension c.
8. Xian and Mingxin actually photo.





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