

## QUAD LOW-CAPACITANCE ARRAY WITH $\pm 15$ -kV ESD PROTECTION

 Check for Samples: [TPD4E002](#)

### FEATURES

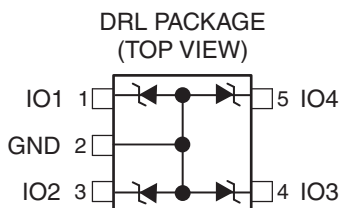
- Four Unidirectional Voltage Suppression Diodes for use in ESD Protection
- I/O Breakdown Voltage,  $V_{BR} = 6.1$  V Min
- Low I/O Capacitance (11 pF at 0 V)
- Low I/O Leakage Current  $<100$  nA
- 2.5-A Peak Pulse Current (8/20-ms Pulse)
- No Power Supply Routing is Required since there is no  $V_{DD}$  Pin
- Very Small Printed Circuit Board (PCB) Area  $<2.6$  mm<sup>2</sup>
- ESD Protection Exceeds
  - $\pm 15$ -kV Human Body Model (HBM)
  - $\pm 15$ -kV IEC 61000-4-2 Contact Discharge

### APPLICATIONS

- Where Transient Overvoltage Protection in ESD-Sensitive Equipment is Required, Such as:
  - Computers
  - Printers
  - Communication Systems and Cellular Phones
  - Video Equipment

### BENEFITS

- High ESD Protection Level
- High Integration
- Suitable for High-Density Boards



### DESCRIPTION/ORDERING INFORMATION

The TPD4E002 is a monolithic array designed to protect up to four lines against ESD transients. Monolithic circuit design allows superior matching between the channels and reduced crosstalk. This device is ideal for applications where both reduced line capacitance and board space-saving are required.

#### ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	1.6 x 1.6 DRL	Reel of 4000	TPD4E002DRLR	28S
			TPD4E002DRL2 <sup>(2)</sup>	

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) The TPD4E002DRL2 is the same exact device as the TPD4E002DRL. This special orderable offers 180 degree shift in device orientation in the reel compared to TI standard DRL package orientation in the reel. Refer to the tape and reel information section at the end of this datasheet for the details on orientation information.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

### Absolute Maximum Ratings

		MIN	MAX	UNIT
V <sub>PP</sub>	ESD discharge	Human Body Model (HBM)		±15
		IEC 61000-4-2 Contact Discharge		±15
T <sub>J</sub>	Junction temperature		125	°C
T <sub>stg</sub>	Storage temperature range	-55	150	°C
T <sub>op</sub>	Operating temperature range	-40	125	°C
	Peak pulse power	t <sub>p</sub> = 8/20 μs		35
	Peak pulse current	t <sub>p</sub> = 8/20 μs		2.5
				W
				A

### Thermal Resistance

PARAMETER		VALUE	UNIT
R <sub>θJA</sub>	Junction to ambient on printed circuit on recommended pad layout	220	°C/W

### Electrical Characteristics

T<sub>amb</sub> = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>BR</sub>	I/O Breakdown voltage	I <sub>R</sub> = 1 mA	6.1		7.2	V
I <sub>RM</sub>	I/O Leakage current	V <sub>RM</sub> = 3 V			0.1	μA
α <sub>T</sub>	Voltage temperature coefficient			45		10 <sup>-4</sup> /°C
C	I/O Capacitance per line			11		pF
R <sub>d</sub>	Dynamic resistance <sup>(1)</sup>			2		Ω

(1) R<sub>d</sub> is measured under reverse breakdown condition with inrush current in the range 1Amps using pulse technique

#### TYPICAL CHARACTERISTICS

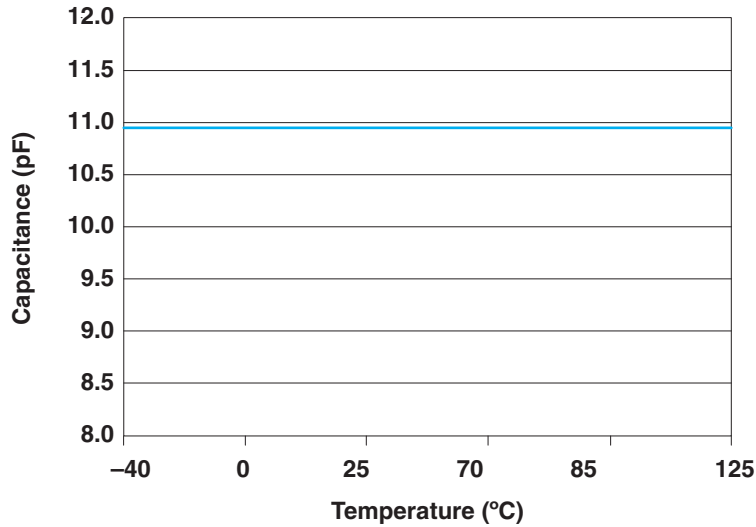


Figure 1. I/O Capacitance vs Temperature

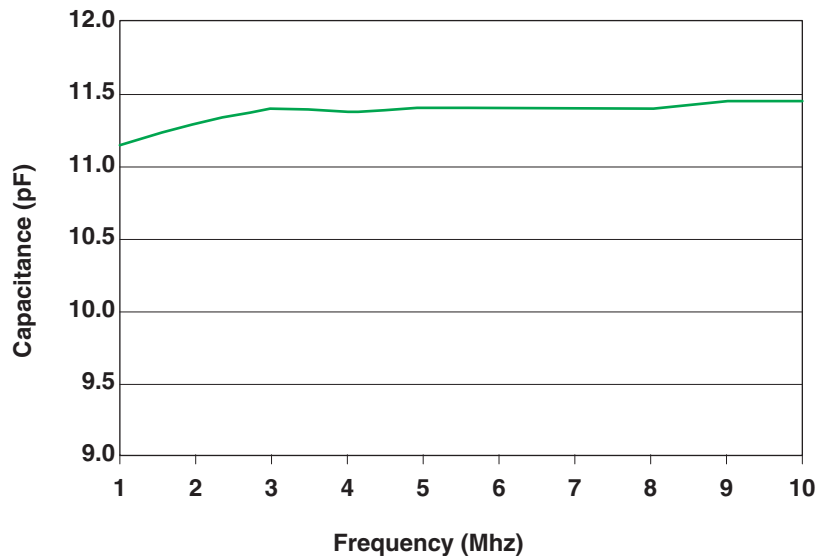
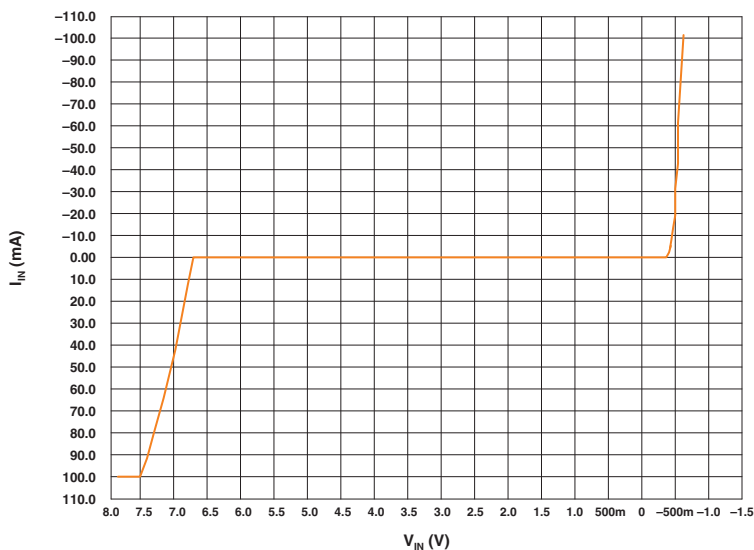
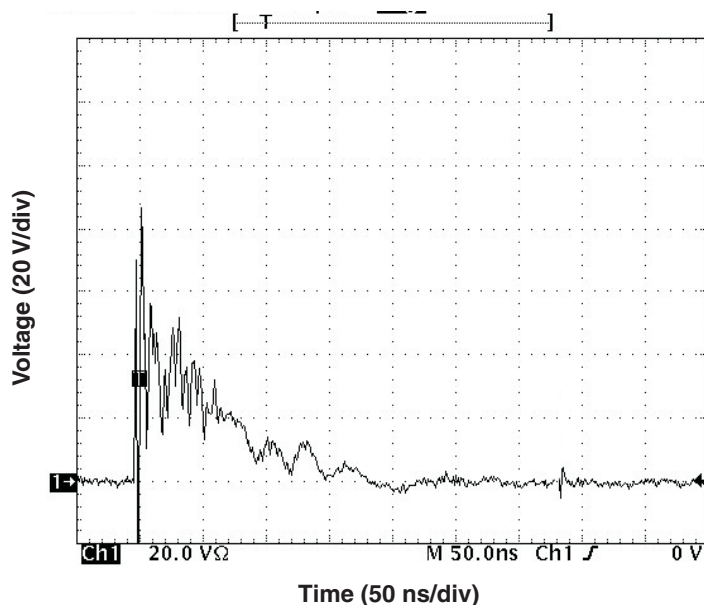


Figure 2. I/O Capacitance vs Frequency (Typical Values)

**TYPICAL CHARACTERISTICS (continued)**



**Figure 3. Diode Current Across I/O Voltage (Typical Values)**



**Figure 4. ESD Clamp Voltage At I/O Pins: IEC6100-4-2 15 kV Contact Discharge**

TYPICAL CHARACTERISTICS (continued)

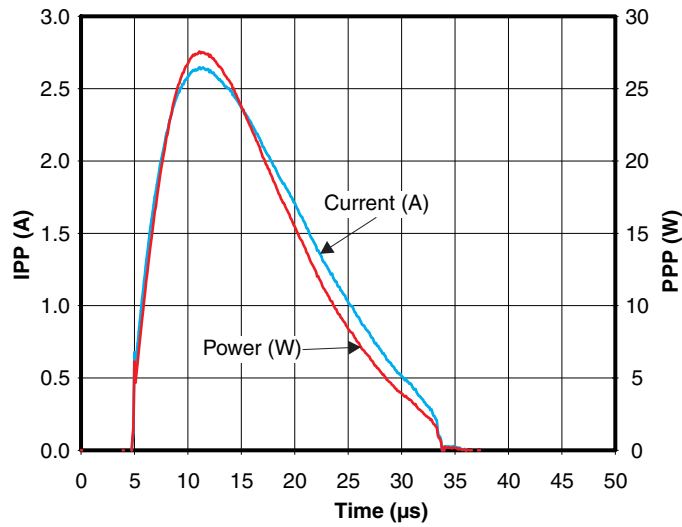


Figure 5. Pulse Waveform (8/20 µs Pulse)

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TPD4E002DRL2	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Request Free Samples</a>
TPD4E002DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Request Free Samples</a>
TPD4E002DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	<a href="#">Request Free Samples</a>

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

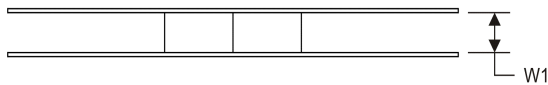
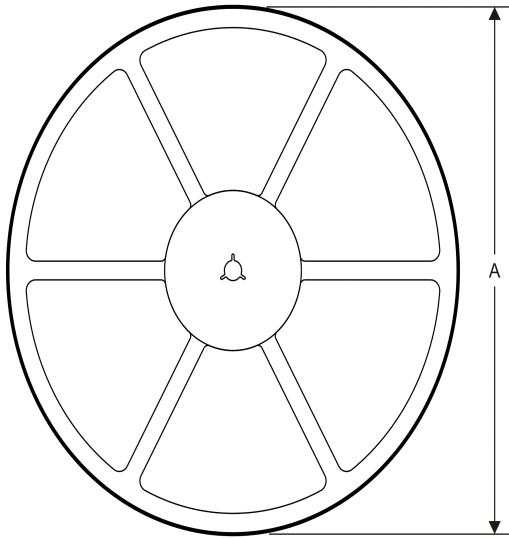
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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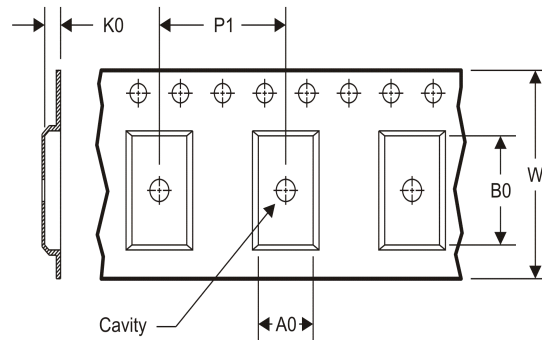
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**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

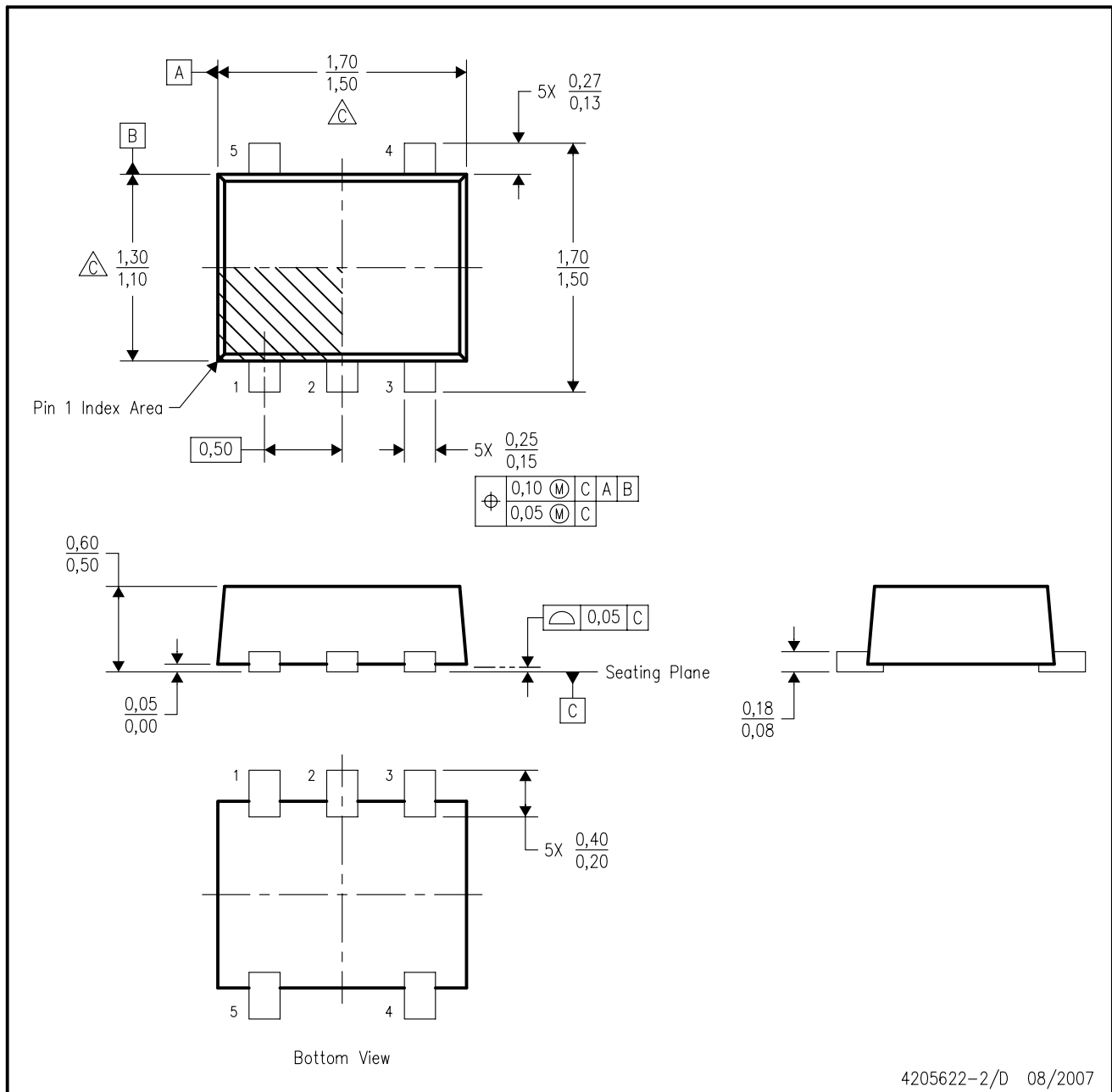
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E002DRL2	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q2
TPD4E002DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

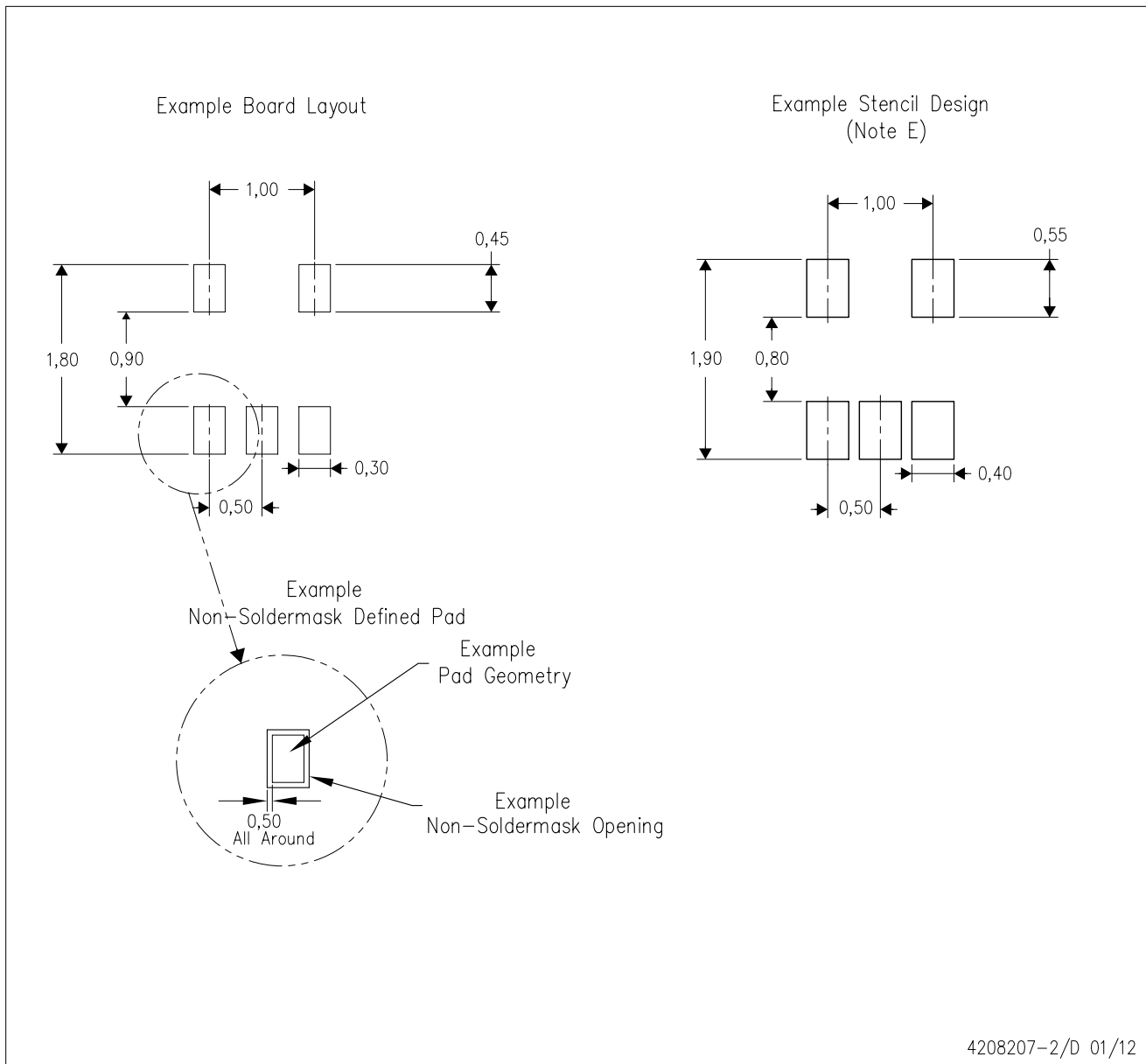
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E002DRL2	SOT	DRL	5	4000	202.0	201.0	28.0
TPD4E002DRLR	SOT	DRL	5	4000	202.0	201.0	28.0



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
  - D. JEDEC package registration is pending.



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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