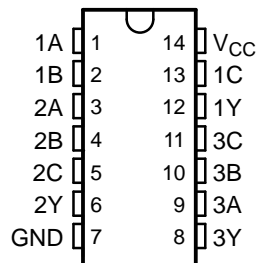


## FEATURES

- Operates From 1.65 V to 3.6 V
- Max  $t_{pd}$  of 3 ns at 3.3 V
- $\pm 24$ -mA Output Drive at 3.3 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

D, DGV, NS, OR PW PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

This triple 3-input positive-NAND gate is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74ALVC10 performs the Boolean function  $Y = \overline{A \cdot B \cdot C}$  or  $Y = \overline{A} + \overline{B} + \overline{C}$  in positive logic.

### ORDERING INFORMATION

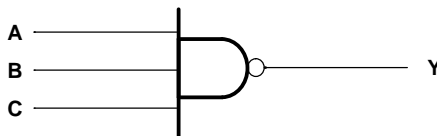
T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC - D	Tube	SN74ALVC10D	ALVC10
		Tape and reel	SN74ALVC10DR	
	SOP - NS	Tape and reel	SN74ALVC10NSR	ALVC10
	TSSOP - PW	Tape and reel	SN74ALVC10PWR	VA10
	TVSOP - DGV	Tape and reel	SN74ALVC10DGVR	VA10

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

### LOGIC DIAGRAM, EACH GATE (POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN74ALVC10

## TRIPLE 3-INPUT POSITIVE-NAND GATE

SCES106H–JULY 1997–REVISED OCTOBER 2004

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	4.6	V
$V_O$	Output voltage range <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$I_O$	Continuous output current		$\pm 50$	mA
	Continuous current through $V_{CC}$ or GND		$\pm 100$	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	D package	86	°C/W
		DGV package	127	
		NS package	76	
		PW package	113	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

### RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	1.65	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7	
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0.8	
$V_I$	Input voltage	0	3.6	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 1.65\text{ V}$	-4	mA
		$V_{CC} = 2.3\text{ V}$	-12	
		$V_{CC} = 2.7\text{ V}$	-12	
		$V_{CC} = 3\text{ V}$	-24	
$I_{OL}$	Low-level output current	$V_{CC} = 1.65\text{ V}$	4	mA
		$V_{CC} = 2.3\text{ V}$	12	
		$V_{CC} = 2.7\text{ V}$	12	
		$V_{CC} = 3\text{ V}$	24	
$\Delta t/\Delta v$	Input transition rise or fall rate		5	ns/V
$T_A$	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> - 0.2			V	
	I <sub>OH</sub> = -4 mA	1.65 V	1.2				
	I <sub>OH</sub> = -6 mA	2.3 V	2				
	I <sub>OH</sub> = -12 mA		2.3 V	1.7			
			2.7 V	2.2			
			3 V	2.4			
I <sub>OH</sub> = -24 mA	3 V	2					
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.2	V	
	I <sub>OL</sub> = 4 mA	1.65 V			0.45		
	I <sub>OL</sub> = 6 mA	2.3 V			0.4		
	I <sub>OL</sub> = 12 mA		2.3 V				0.7
			2.7 V				0.4
	I <sub>OL</sub> = 24 mA	3 V			0.55		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V			±5	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			10	μA	
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		4		pF	

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

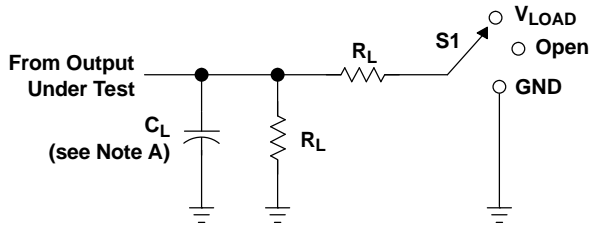
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A, B, or C	Y	1.1	4.8	1	3	3.3		1	3	ns

## OPERATING CHARACTERISTICS

T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
		TYP	TYP	TYP	
C <sub>pd</sub> Power dissipation capacitance per gate	C <sub>L</sub> = 0, f = 10 MHz	23	24	26	pF

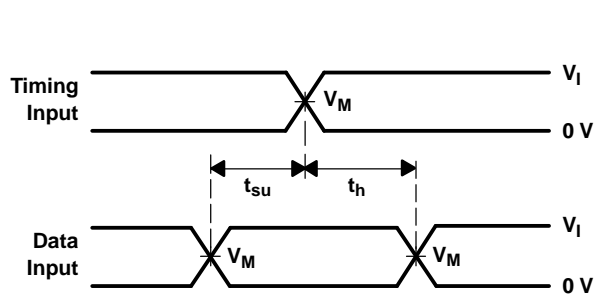
PARAMETER MEASUREMENT INFORMATION



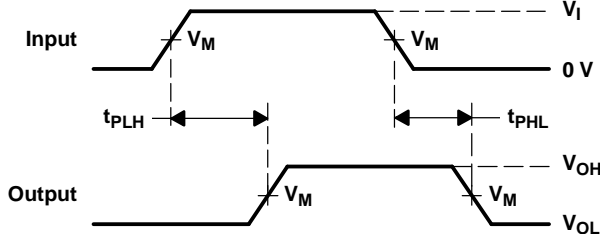
LOAD CIRCUIT

TEST	S1
$t_{pd}$ $t_{PLZ}/t_{PZL}$ $t_{PHZ}/t_{PZH}$	Open $V_{LOAD}$ GND

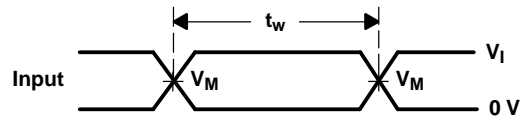
$V_{CC}$	INPUT		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8 V \pm 0.15 V$	$V_{CC}$	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5 V \pm 0.2 V$	$V_{CC}$	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3 V \pm 0.3 V$	2.7 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



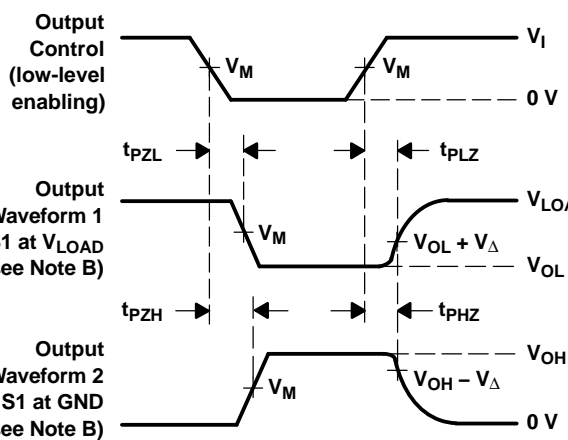
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74ALVC10D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC10DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC10DGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC10DGVRE4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC10DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC10DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC10NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC10NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC10PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC10PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC10PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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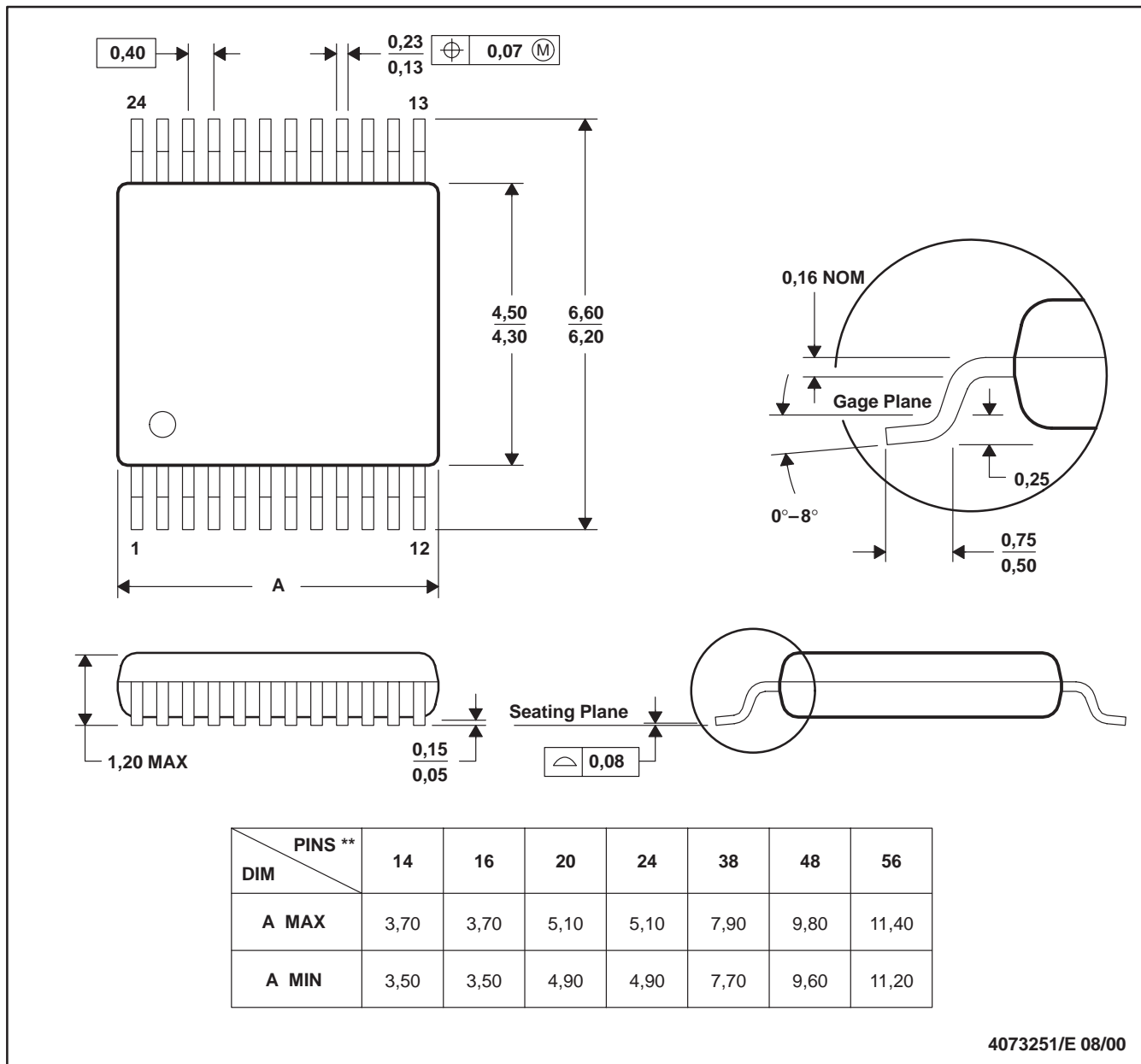
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DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AB.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
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