

LOW-POWER DIFFERENTIAL LINE DRIVER AND RECEIVER PAIRS

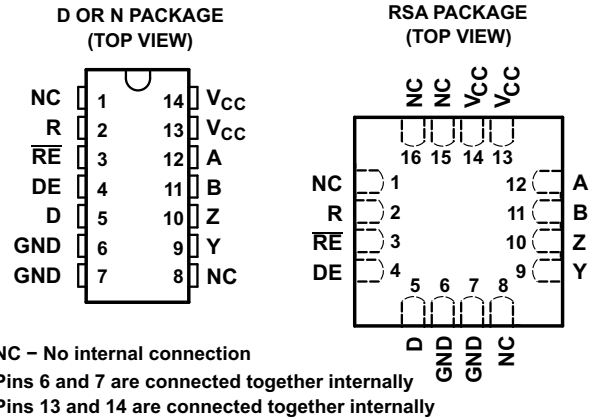
FEATURES

- Designed for High-Speed Multipoint Data Transmission Over Long Cables
- Operate With Pulse Durations as Low as 30 ns
- Low Supply Current . . . 5 mA Max
- Meet or Exceed the Requirements of ANSI Standard RS-485 and ISO 8482:1987(E)
- 3-State Outputs for Party-Line Buses
- Common-Mode Voltage Range of -7 V to 12 V
- Thermal Shutdown Protection Prevents Driver Damage From Bus Contention
- Positive and Negative Output Current Limiting
- Pin Compatible With the SN75ALS180

DESCRIPTION

The SN65LBC180 and SN75LBC180 differential driver and receiver pairs are monolithic integrated circuits designed for bidirectional data communication over long cables that take on the characteristics of transmission lines. They are balanced, or differential, voltage mode devices that meet or exceed the requirements of industry standards ANSI RS-485 and ISO 8482:1987(E). Both devices are designed using TI's proprietary LinBiCMOS™ with the low-power consumption of CMOS and the precision and robustness of bipolar transistors in the same circuit.

Both the SN65LBC180 and SN75LBC180 combine a differential line driver and receiver with 3-state outputs and operate from a single 5-V supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are connected to separate terminals for full-duplex operation and are designed to present minimum loading to the bus whether disabled or powered off ($V_{CC} = 0$). These parts feature a wide common-mode voltage range making them suitable for point-to-point or multipoint data-bus applications.



Function Tables

DRIVER

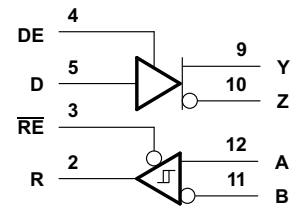
INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A–B	ENABLE \overline{RE}	OUTPUT R
$V_{ID} \geq 0.2\text{ V}$	L	H
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	L	?
$V_{ID} \leq -0.2\text{ V}$	L	L
X	H	Z
Open circuit	L	H

H = high level, L = low level, ? = indeterminate, x = irrelevant
Z = high impedance (off)

logic diagram (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinBiCMOS is a trademark of Texas Instruments.



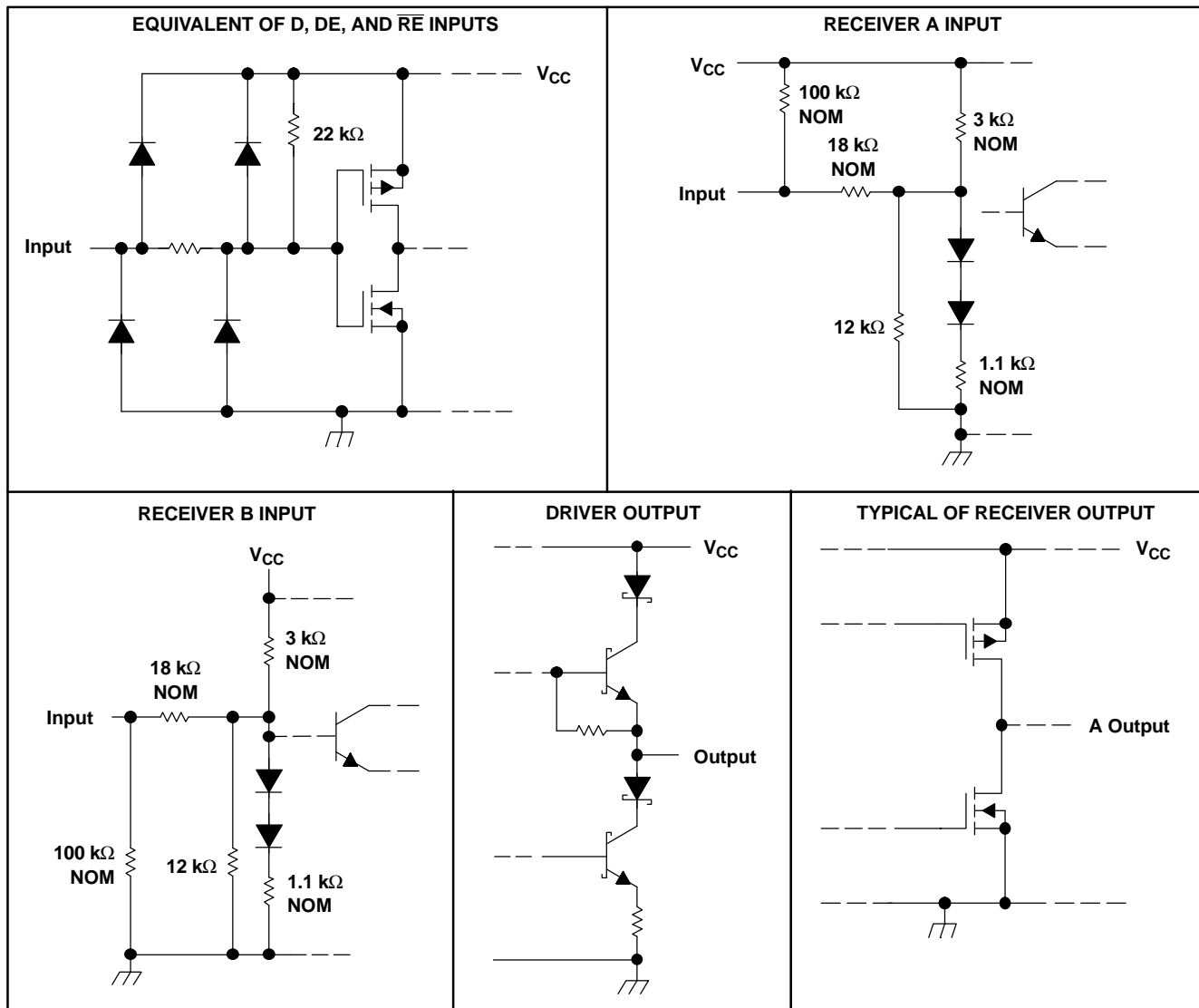
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The devices also provide positive and negative output-current limiting and thermal shutdown for protection from line fault conditions. The line driver shuts down at a junction temperature of approximately 172°C.

The SN65LBC180 and SN75LBC180 are available in the 14-pin dual-in-line and small-outline packages. The SN75LBC180 is characterized for operation over the commercial temperature range of 0°C to 70°C. The SN65LBC180 is characterized over the industrial temperature range of -40°C to 85°C.

SCHEMATICS OF INPUTS AND OUTPUTS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			UNIT
V _{CC}	Supply voltage range ⁽²⁾	-0.3 to 7	V
V _{BUS}	Bus voltage range (A, B, Y, Z) ⁽²⁾	-10 to 15	V
	Voltage range at D, R, DE, \overline{RE} ⁽²⁾	-0.3 to V _{CC} + 0.5	V
	Continuous total power dissipation ⁽³⁾	Internally limited	
	Total power dissipation	See Dissipation Rating Table	
T _A	Operating free-air temperature range	SN65LBC180	-40 to 85 °C
		SN75LBC180	0 to 70 °C
T _{stg}	Storage temperature range	-65 to 150	°C
I _O	Receiver output current range	-50 to 50	mA
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

DISSIPATION RATING TABLE

PACKAGE ⁽¹⁾	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW
RSA	3333 mW	26.67 mW/°C	2133 mW	1733 mW

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.75	5	5.25	V
V _{IH}	High-level input voltage	D, DE, and \overline{RE}	2			V
V _{IL}	Low-level input voltage	D, DE, and \overline{RE}			0.8	V
V _{ID}	Differential input voltage		-6 ⁽¹⁾		6	V
V _O , V _I , or V _{IC}	Voltage at any bus terminal (separately or common mode)	A, B, Y, or Z	-7 ⁽¹⁾		12	V
I _{OH}	High-level output current	Y or Z			-60	mA
		R			-8	
I _{OL}	Low-level output current	Y or Z			60	mA
		R			8	
T _A	Operating free-air temperature	SN65LBC180	-40		85	°C
		SN75LBC180	0		70	

- (1) The algebraic convention where the least positive (more negative) limit is designated minimum, is used in this data sheet for the differential input voltage, voltage at any bus terminal, operating temperature, input threshold voltage, and common-mode output voltage.

DRIVER SECTION

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18 \text{ mA}$				-1.5	V
$ V_{OD} $	Differential output voltage magnitude ⁽²⁾	$R_L = 54 \Omega$, See Figure 1	SN65LBC180	1.1	2.5	5	V
			SN75LBC180	1.5	2.5	5	
		$R_L = 60 \Omega$, See Figure 2	SN65LBC180	1.1	2	5	
			SN75LBC180	1.5	2	5	
$\Delta V_{OD} $	Change in magnitude of differential output voltage ⁽³⁾	See Figure 1 and Figure 2				± 0.2	V
V_{OC}	Common-mode output voltage			1	2.5	3	V
$\Delta V_{OC} $	Change in magnitude of common-mode output voltage ⁽³⁾	$R_L = 54 \Omega$,	See Figure 1			± 0.2	V
I_O	Output current with power off	$V_{CC} = 0$,	$V_O = -7 \text{ V to } 12 \text{ V}$			± 100	μA
I_{OZ}	High-impedance-state output current	$V_O = -7 \text{ V to } 12 \text{ V}$				± 100	μA
I_{IH}	High-level input current	$V_I = 2.4 \text{ V}$				100	μA
I_{IL}	Low-level input current	$V_I = 0.4 \text{ V}$				100	μA
I_{OS}	Short-circuit output current	$-7 \text{ V} \leq V_O \leq 12 \text{ V}$				± 250	mA
I_{CC}	Supply current	Receiver disabled	Outputs enabled			5	mA
			Outputs disabled			3	

(1) All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

(2) The minimum V_{OD} specification of the SN65LBC180 may not fully comply with ANSI RS-485 at operating temperatures below 0°C . System designers should take the possibly lower output signal into account in determining the maximum signal-transmission distance.

(3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in the steady-state magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

SWITCHING CHARACTERISTICS

$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	$R_L = 54 \Omega$,	See Figure 3	7	12	18	ns
$t_{t(OD)}$	Differential output transition time			5	10	20	ns
t_{PZH}	Output enable time to high level	$R_L = 110 \Omega$,	See Figure 4			35	ns
t_{PZL}	Output enable time to low level	$R_L = 110 \Omega$,	See Figure 5			35	ns
t_{PHZ}	Output disable time from high level	$R_L = 110 \Omega$,	See Figure 4			50	ns
t_{PLZ}	Output disable time from low level	$R_L = 110 \Omega$,	See Figure 5			35	ns

RECEIVER SECTION

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$I_O = -8$ mA			0.2	V
V_{IT-}	Negative-going input threshold voltage	$I_O = 8$ mA	-0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			45		mV
V_{IK}	Enable-input clamp voltage	$I_I = -18$ mA			-1.5	V
V_{OH}	High-level output voltage	$V_{ID} = 200$ mV, $I_{OH} = -8$ mA	3.5	4.5		V
V_{OL}	Low-level output voltage	$V_{ID} = -200$ mV, $I_{OL} = 8$ mA		0.3	0.5	V
I_{OZ}	High-impedance-state output current	$V_O = 0$ V to V_{CC}			± 20	μ A
I_{IH}	High-level enable-input current	$V_{IH} = 2.4$ V			-50	μ A
I_{IL}	Low-level enable-input current	$V_{IL} = 0.4$ V			-100	μ A
I_I	Bus input current	$V_I = 12$ V, $V_{CC} = 5$ V, Other input at 0 V		0.7	1	mA
		$V_I = 12$ V, $V_{CC} = 0$ V, Other input at 0 V		0.8	1	
		$V_I = -7$ V, $V_{CC} = 5$ V, Other input at 0 V		-0.5	-0.8	
		$V_I = -7$ V, $V_{CC} = 0$ V, Other input at 0 V		-0.5	-0.8	
I_{CC}	Supply current	Driver disabled	Outputs enabled		5	mA
			Outputs disabled		3	

SWITCHING CHARACTERISTICS

$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	$V_{ID} = -1.5$ V to 1.5 V, See Figure 6	11	22	33	ns
t_{PLH}	Propagation delay time, low- to high-level output		11	22	33	ns
$t_{sk(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $)			3	6	ns
t_t	Transition time			5	8	ns
t_{PZH}	Output enable time to high level	See Figure 7			35	ns
t_{PZL}	Output enable time to low level				30	ns
t_{PHZ}	Output disable time from high level				35	ns
t_{PLZ}	Output disable time from low level				30	ns

PARAMETER MEASUREMENT INFORMATION

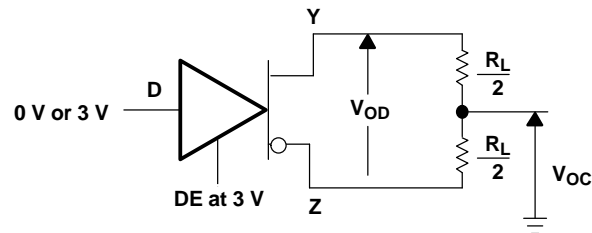


Figure 1. Differential and Common-Mode Output Voltages

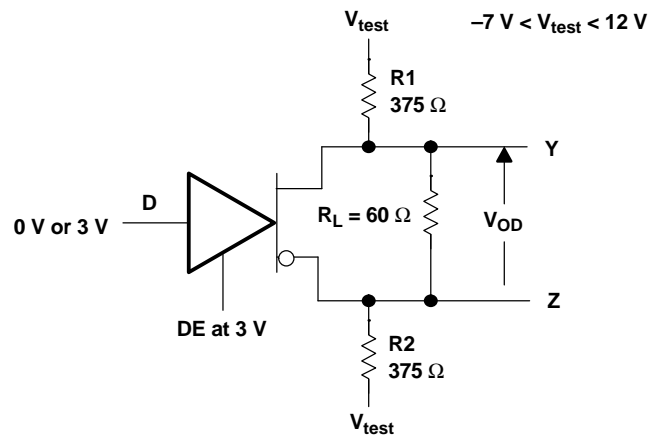
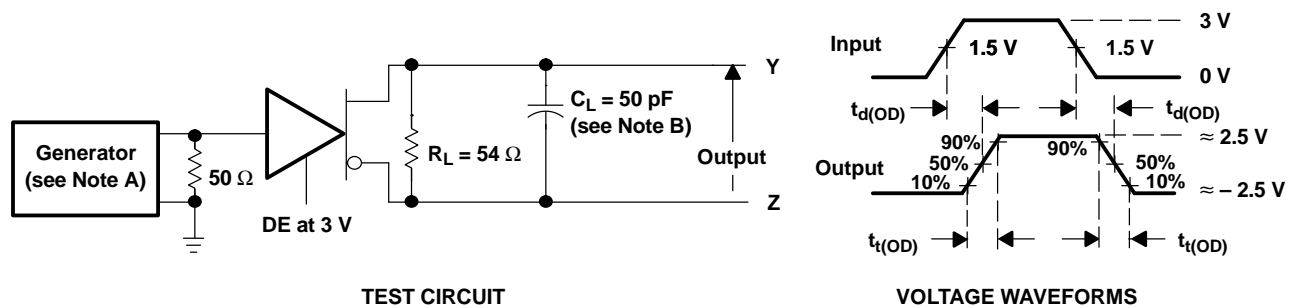


Figure 2. Driver V_{OD} Test Circuit



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR > 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Differential Output Delay and Transition Time Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

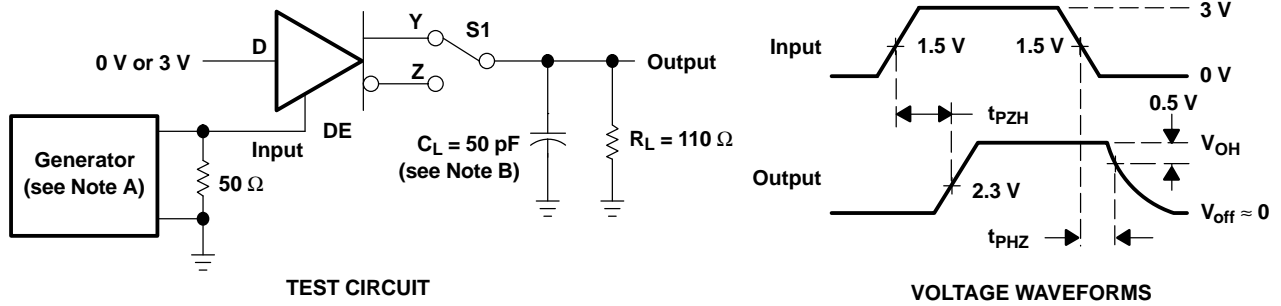


Figure 4. Driver Test Circuit and Enable and Disable Time Waveforms

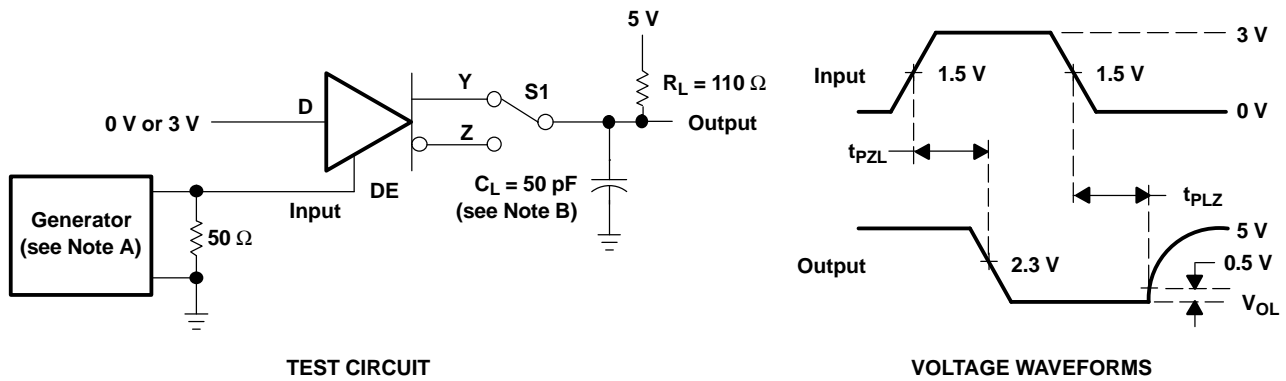
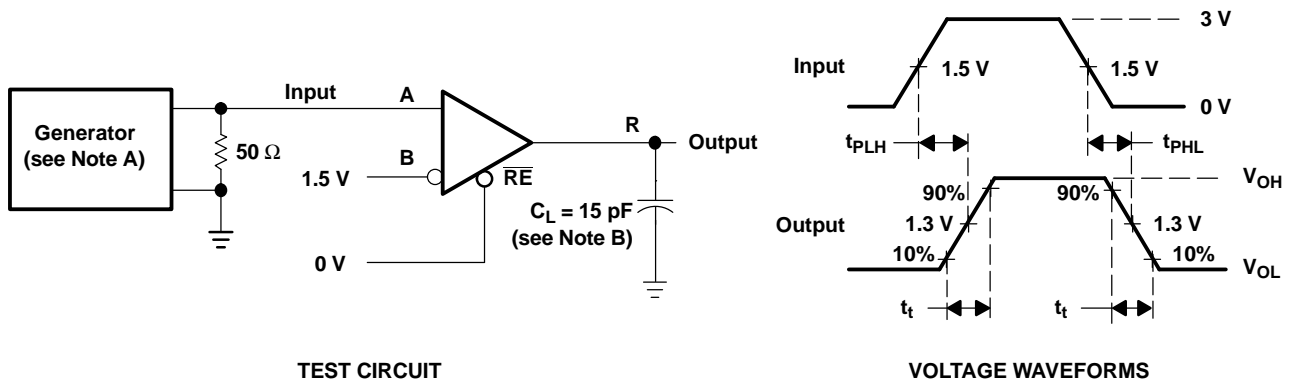


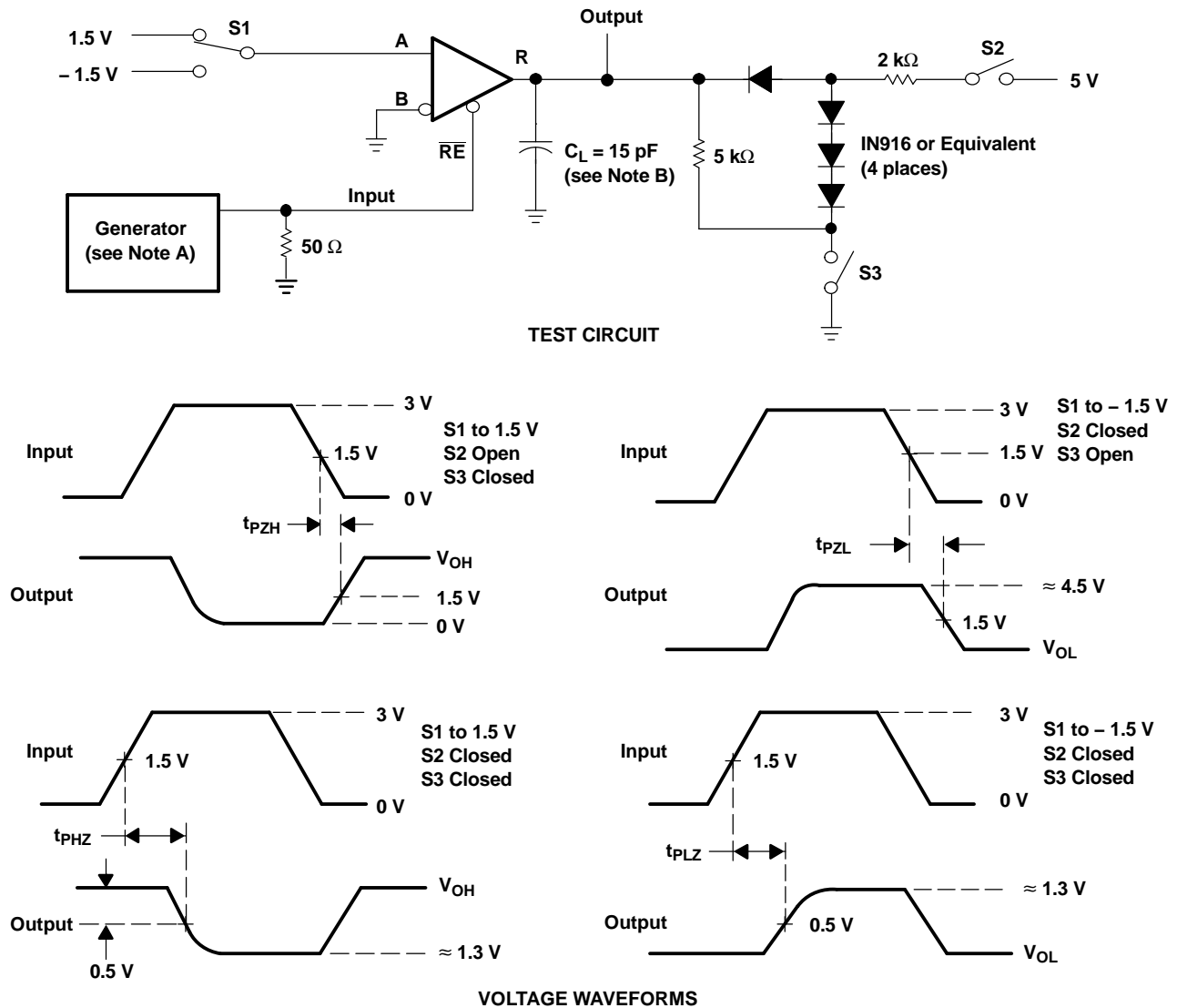
Figure 5. Driver Test Circuit and Enable and Disable Time Voltage Waveforms



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_0 = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Propagation Delay Time Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 7. Receiver Output Enable and Disable Times

TYPICAL CHARACTERISTICS

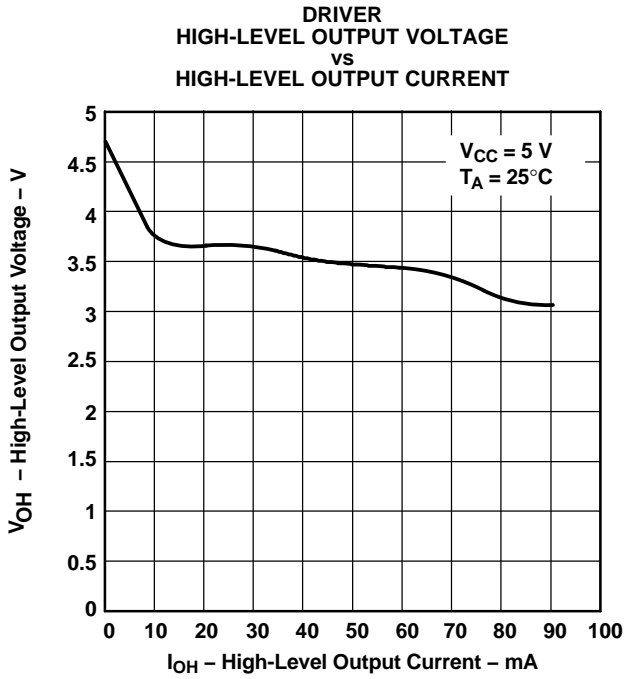


Figure 8.

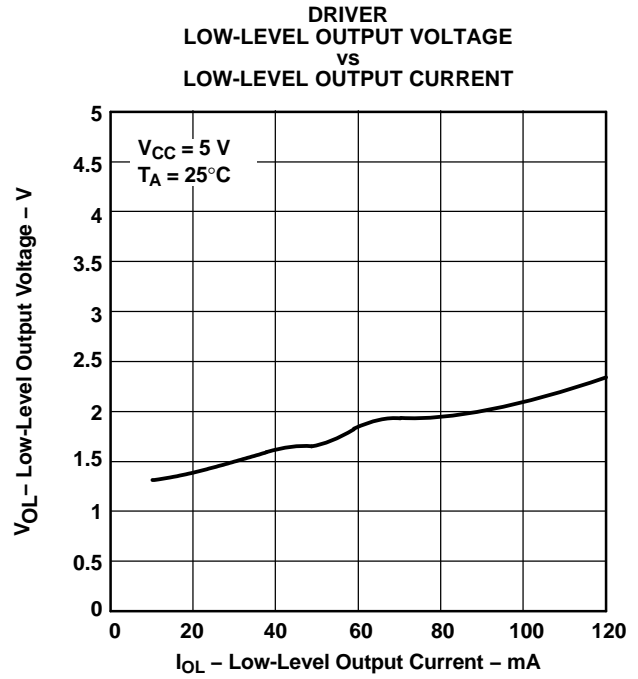


Figure 9.

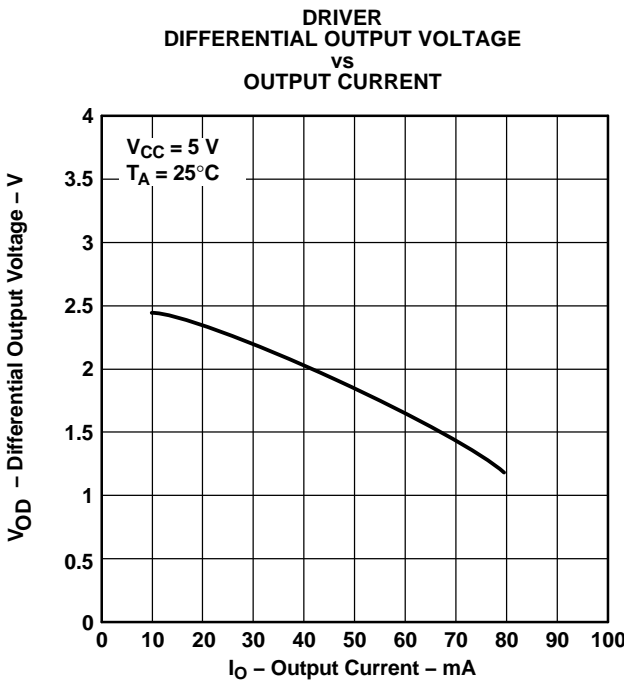


Figure 10.

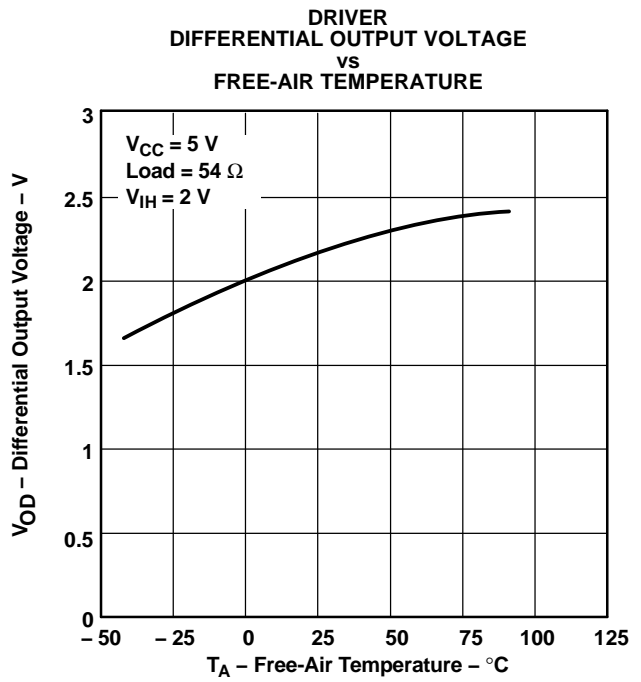


Figure 11.

TYPICAL CHARACTERISTICS (continued)

DRIVER
DIFFERENTIAL DELAY TIMES
VS
FREE-AIR TEMPERATURE

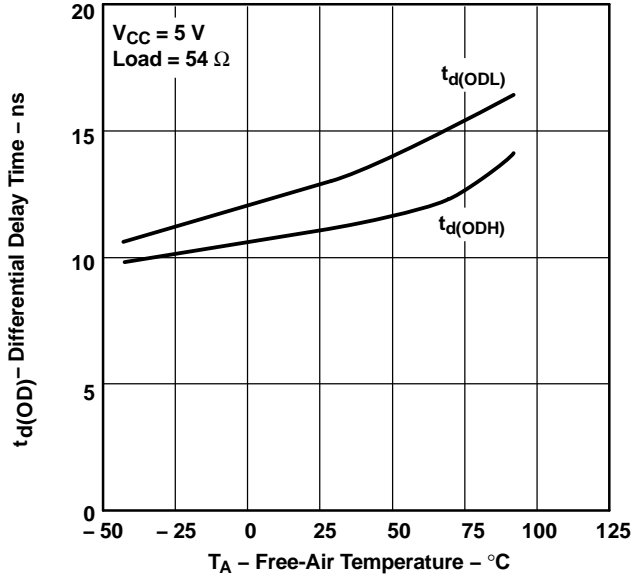


Figure 12.

DRIVER
OUTPUT CURRENT
VS
SUPPLY VOLTAGE

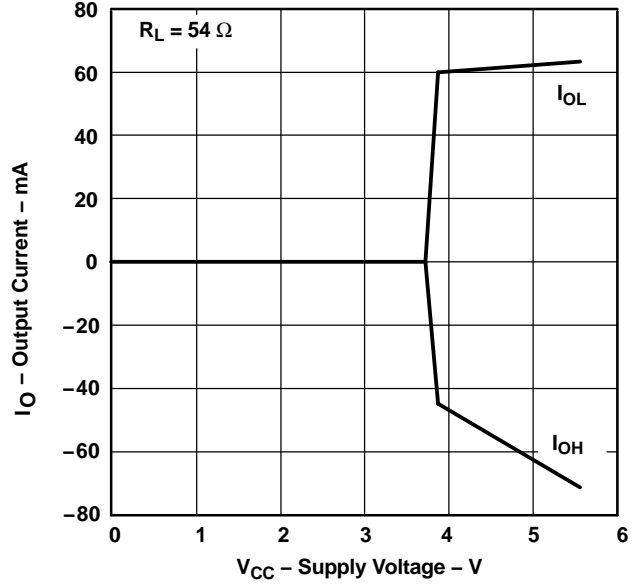


Figure 13.

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT

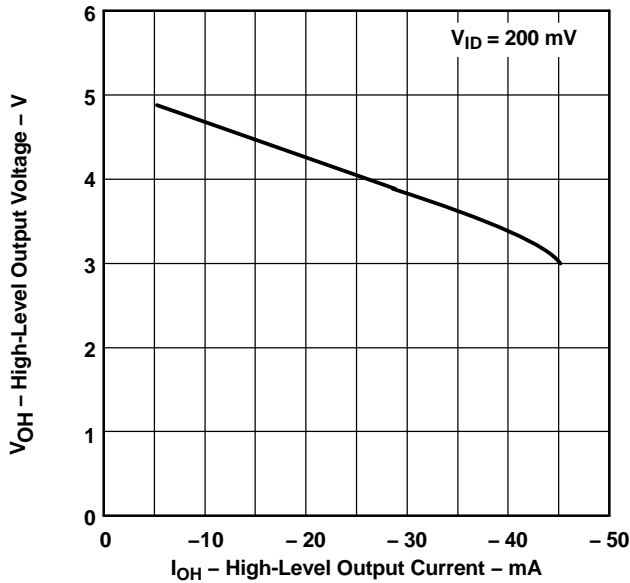


Figure 14.

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT

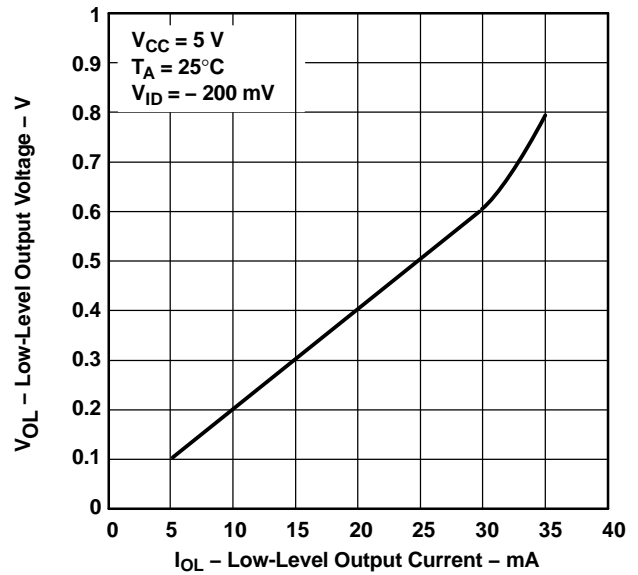
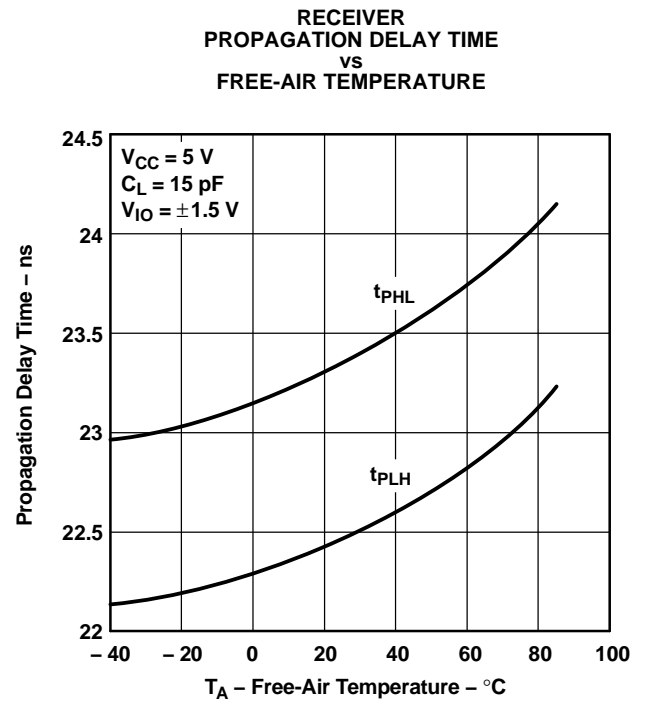
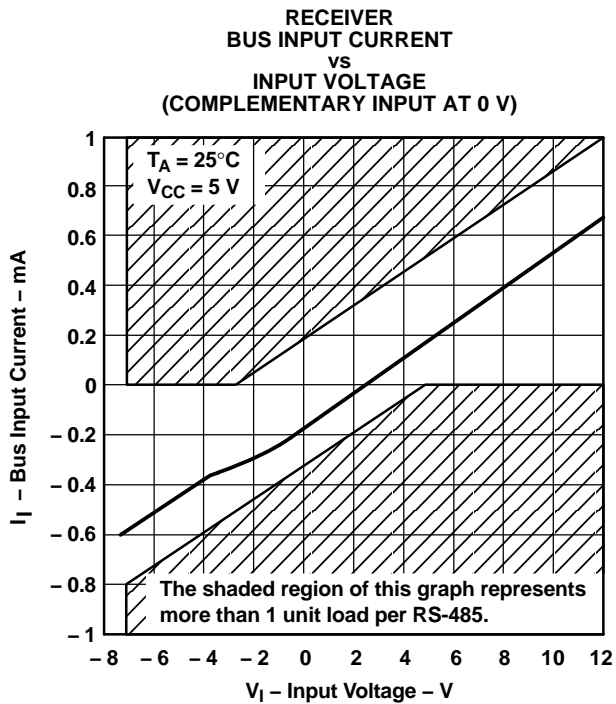
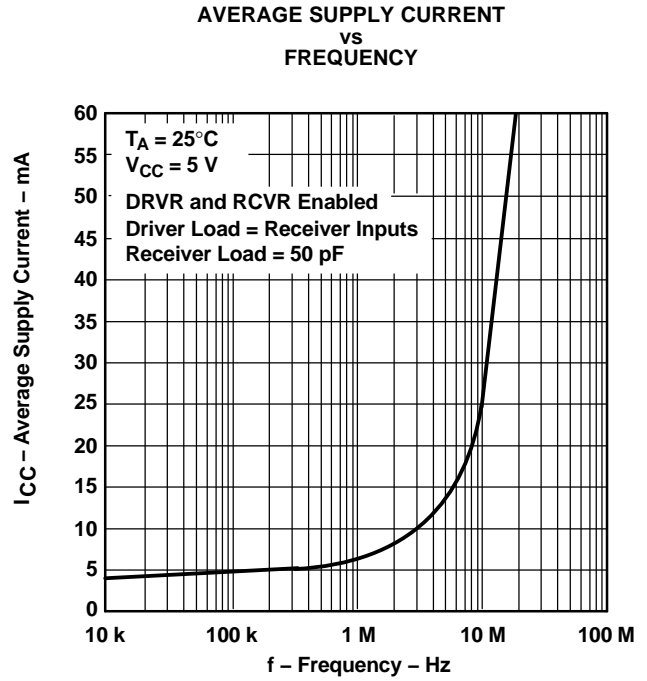
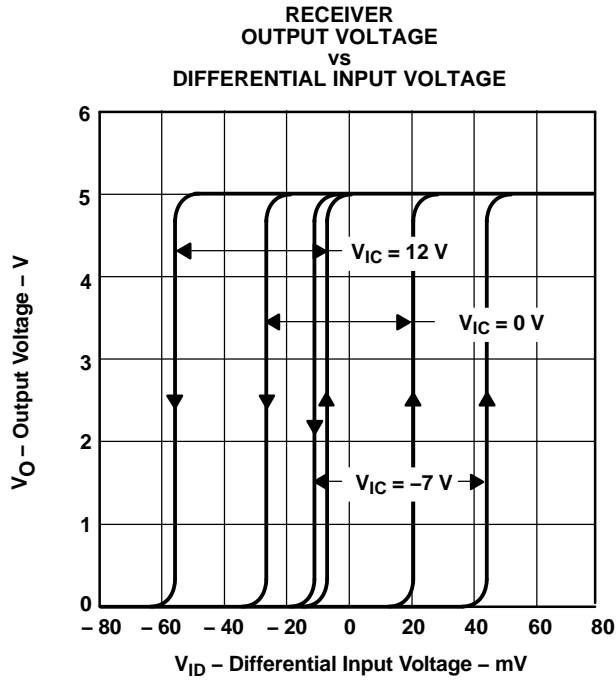


Figure 15.

TYPICAL CHARACTERISTICS (continued)



APPLICATION INFORMATION

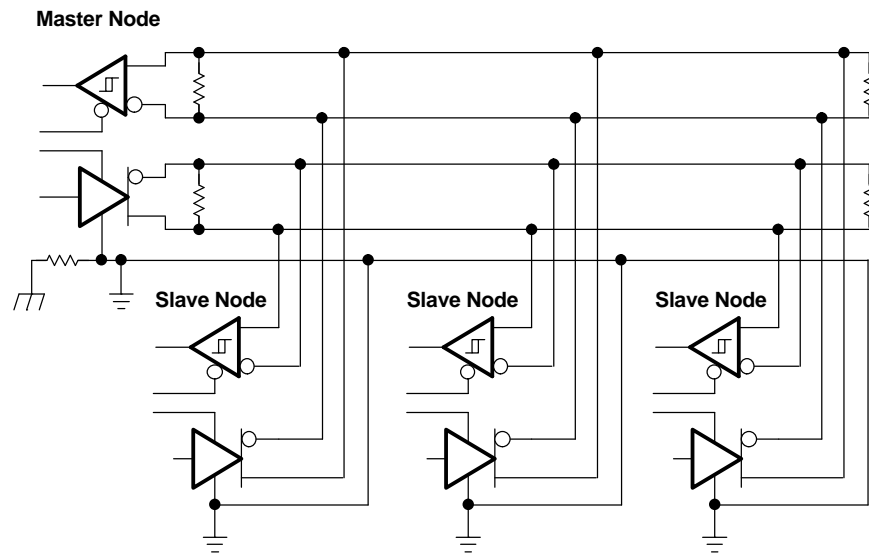


Figure 20. Full Duplex Application Circuit

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65LBC180D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
SN65LBC180DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
SN65LBC180DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
SN65LBC180DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
SN65LBC180N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65LBC180NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65LBC180RSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LBC180RSARG4	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LBC180RSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LBC180RSATG4	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LBC180D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC180DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC180DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC180DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC180N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75LBC180NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75LBC180RSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LBC180RSARG4	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LBC180RSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LBC180RSATG4	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

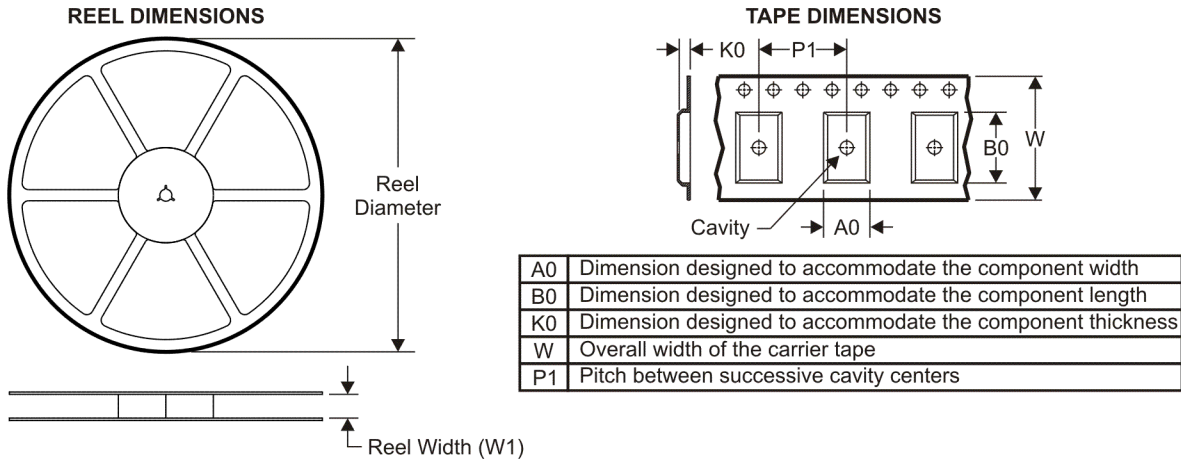
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

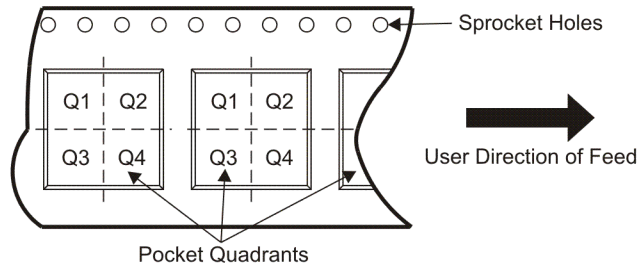
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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC180DR	SOIC	D	14	2500	330.0	16.0	7.0	9.0	2.0	8.0	16.0	Q1
SN65LBC180DR	SOIC	D	14	2500	330.0	16.0	7.0	9.0	2.0	8.0	16.0	Q1
SN65LBC180RSAR	QFN	RSA	16	3000	330.0	12.0	4.0	4.0	2.0	8.0	12.0	Q2
SN65LBC180RSAT	QFN	RSA	16	250	180.0	12.0	4.0	4.0	2.0	8.0	12.0	Q2
SN75LBC180DR	SOIC	D	14	2500	330.0	16.0	7.0	9.0	2.0	8.0	16.0	Q1
SN75LBC180DR	SOIC	D	14	2500	330.0	16.0	7.0	9.0	2.0	8.0	16.0	Q1
SN75LBC180RSAR	QFN	RSA	16	3000	330.0	12.0	4.0	4.0	2.0	8.0	12.0	Q2
SN75LBC180RSAT	QFN	RSA	16	250	180.0	12.0	4.0	4.0	2.0	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC180DR	SOIC	D	14	2500	343.0	346.0	29.0
SN65LBC180DR	SOIC	D	14	2500	346.0	346.0	33.0
SN65LBC180RSAR	QFN	RSA	16	3000	346.0	346.0	29.0
SN65LBC180RSAT	QFN	RSA	16	250	191.0	213.0	32.0
SN75LBC180DR	SOIC	D	14	2500	343.0	346.0	29.0
SN75LBC180DR	SOIC	D	14	2500	346.0	346.0	33.0
SN75LBC180RSAR	QFN	RSA	16	3000	346.0	346.0	29.0
SN75LBC180RSAT	QFN	RSA	16	250	191.0	213.0	32.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

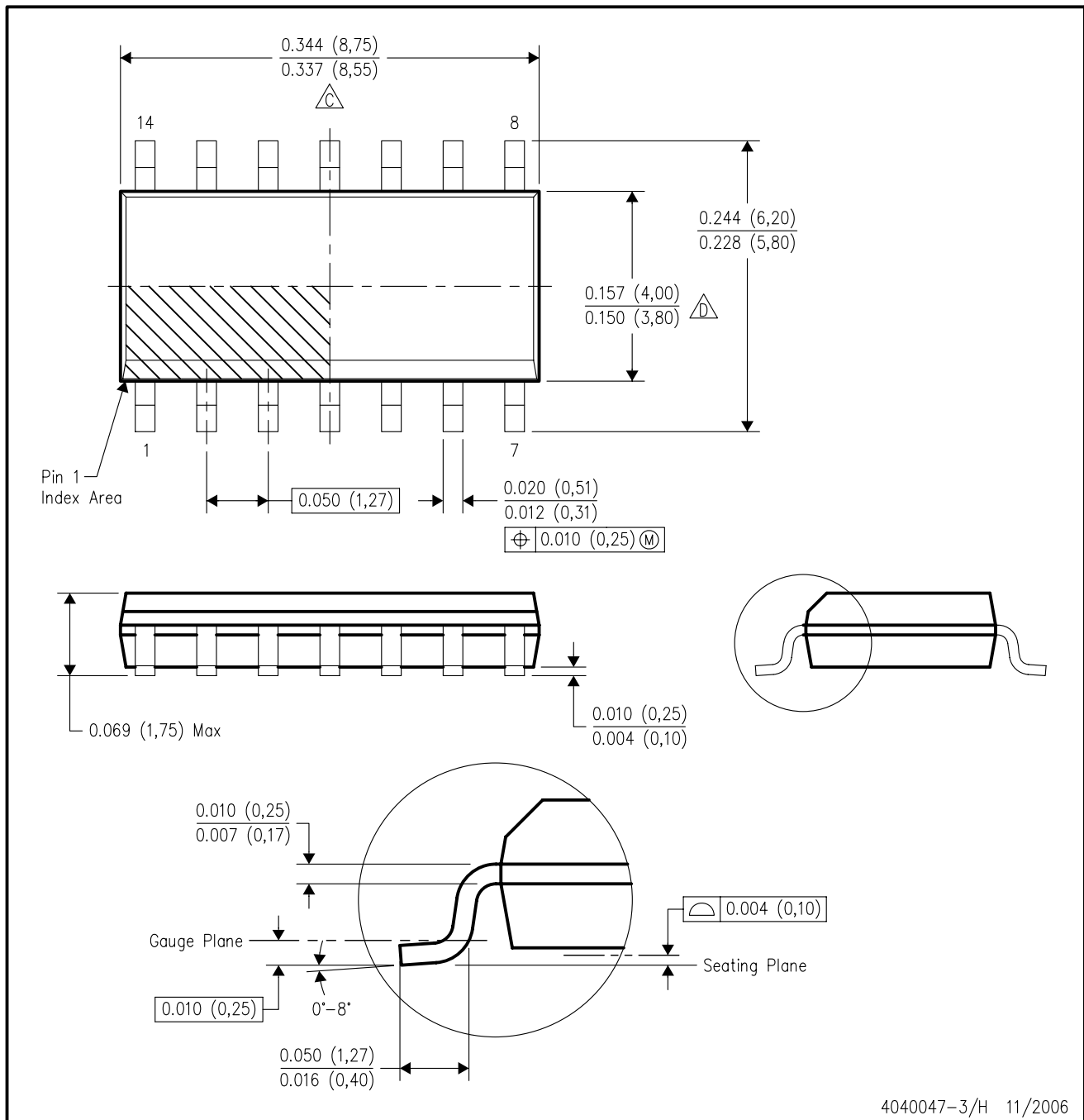
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

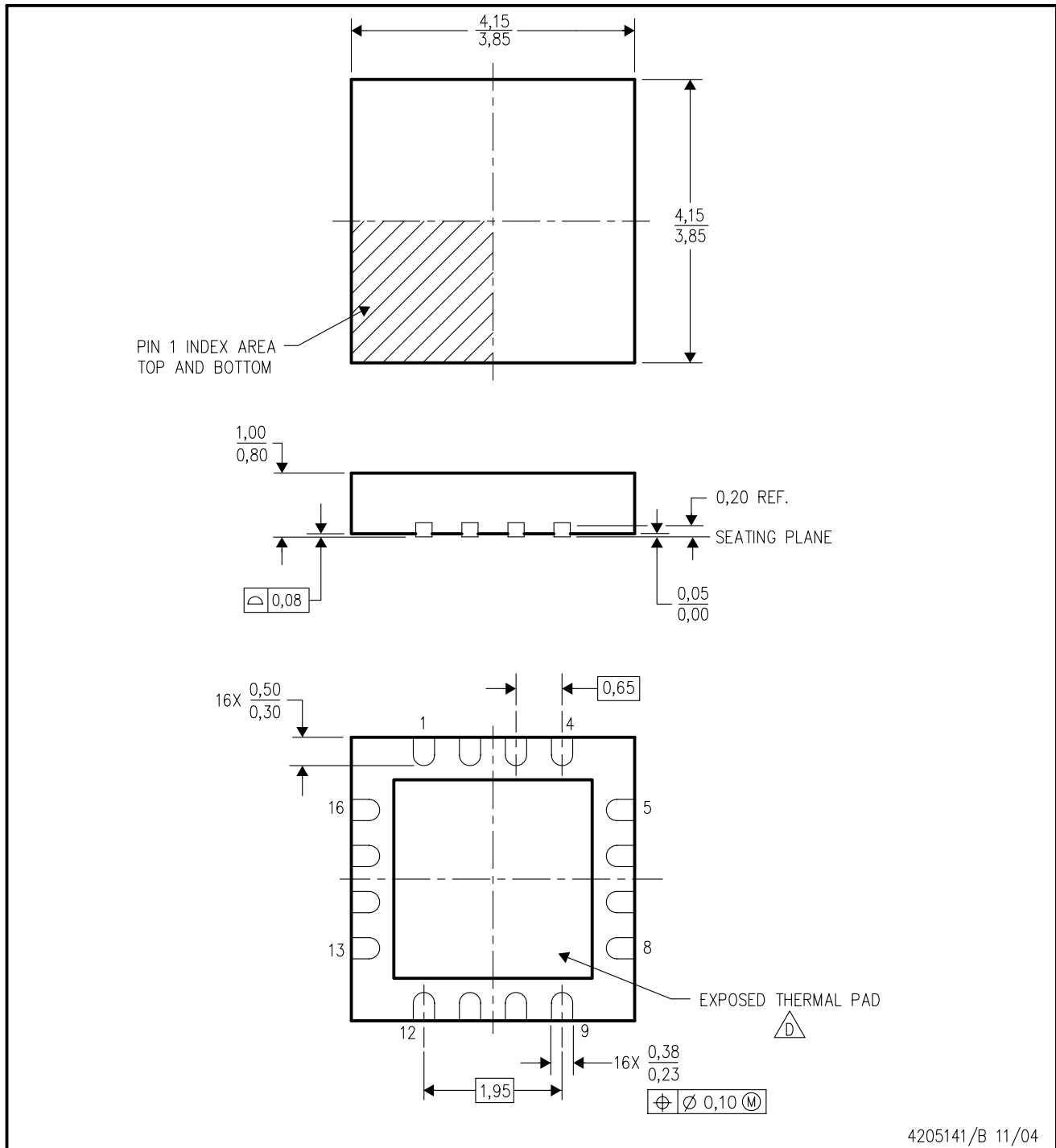
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AB.

RSA (S-PQFP-N16)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - △ The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.

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