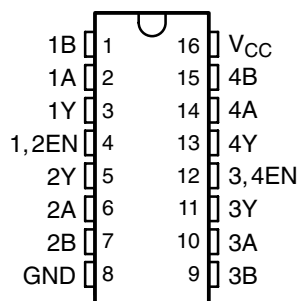


# SN65175, SN75175 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS145C – OCTOBER 1990 – REVISED NOVEMBER 2006

- Meet or Exceed the Requirements of ANSI Standard EIA/TIA-422-B, RS-423-B, and RS-485
- Meet ITU Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range –12 V to 12 V
- Input Sensitivity . . .  $\pm 200$  mV
- Input Hysteresis . . . 50 mV Typ
- High Input Impedance . . . 12 k $\Omega$  Min
- Operate From Single 5-V Supply
- Low-Power Requirements
- Plug-In Replacement for MC3486

D OR N PACKAGE  
(TOP VIEW)



## description

The SN65175 and SN75175 are monolithic quadruple differential line receivers with 3-state outputs. They are designed to meet the requirements of ANSI Standards EIA/TIA-422-B, RS-423-B, and RS-485, and several ITU recommendations. These standards are for balanced multipoint bus transmission at rates up to 10 megabits per second. Each of the two pairs of receivers has a common active-high enable.

The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of  $\pm 200$  mV over a common-mode input voltage range of  $\pm 12$  V. The SN65175 and SN75175 are designed for optimum performance when used with the SN75172 or SN75174 quadruple differential line drivers.

The SN65175 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The SN75175 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE  
(each receiver)

| DIFFERENTIAL<br>A – B       | ENABLE | OUTPUT<br>Y |
|-----------------------------|--------|-------------|
| $V_{ID} \geq 0.2$ V         | H      | H           |
| $-0.2$ V $< V_{ID} < 0.2$ V | H      | ?           |
| $V_{ID} \leq -0.2$ V        | H      | L           |
| X                           | L      | Z           |
| Open circuit                | H      | ?           |

H = high level, L = low level, ? = indeterminate,  
X = irrelevant, Z = high impedance (off)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

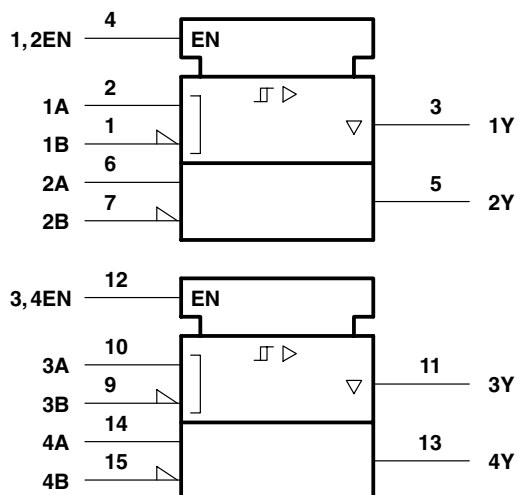
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# SN65175, SN75175 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

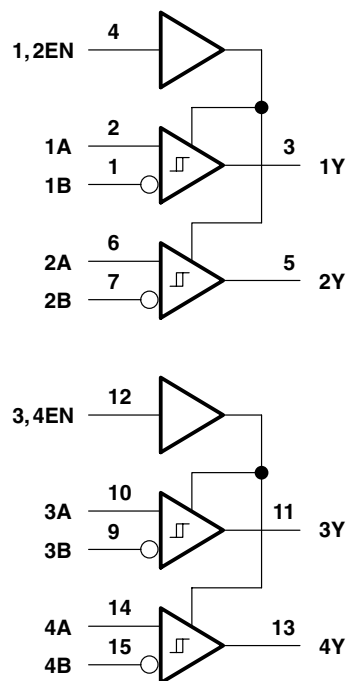
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## logic symbol†

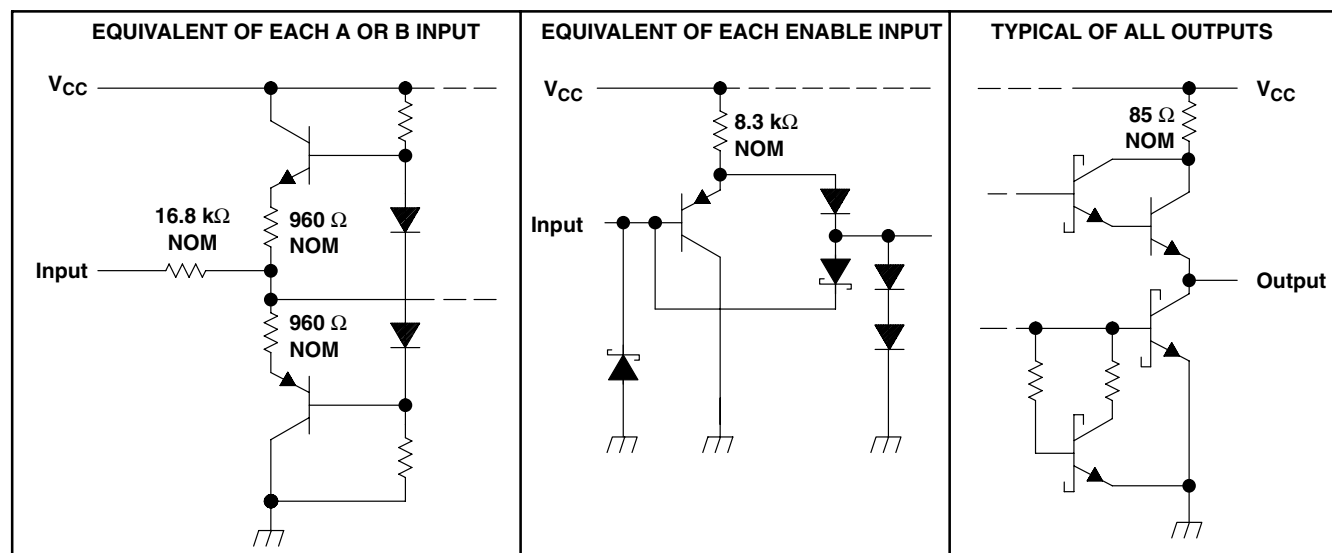


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## schematics of inputs and outputs



# SN65175, SN75175 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                              |                                                |
|--------------------------------------------------------------|------------------------------------------------|
| Supply voltage, $V_{CC}$ (see Note 1)                        | 7 V                                            |
| Input voltage $V_I$ , (A or B inputs)                        | $\pm 25$ V                                     |
| Differential input voltage, $V_{ID}$ (see Note 2)            | $\pm 25$ V                                     |
| Enable input voltage, $V_I$ , EN                             | 7 V                                            |
| Low-level output current, $I_{OL}$                           | 50 mA                                          |
| Continuous total dissipation                                 | See Dissipation Rating Table                   |
| Operating free-air temperature range, $T_A$ : SN65175        | $-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$  |
| SN75175                                                      | $0^{\circ}\text{C}$ to $70^{\circ}\text{C}$    |
| Storage temperature range, $T_{stg}$                         | $-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$ |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | $260^{\circ}\text{C}$                          |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.  
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^{\circ}\text{C}$<br>POWER RATING | DERATING<br>FACTOR         | $T_A = 70^{\circ}\text{C}$<br>POWER RATING | $T_A = 85^{\circ}\text{C}$<br>POWER RATING |
|---------|-----------------------------------------------|----------------------------|--------------------------------------------|--------------------------------------------|
| D       | 950 mW                                        | 7.6 mW/ $^{\circ}\text{C}$ | 608 mW                                     | 494 mW                                     |
| N       | 1150 mW                                       | 9.2 mW/ $^{\circ}\text{C}$ | 736 mW                                     | 598 mW                                     |

## recommended operating conditions

|                                           |         | MIN   | NOM | MAX      | UNIT               |
|-------------------------------------------|---------|-------|-----|----------|--------------------|
| Supply voltage, $V_{CC}$                  |         | 4.75  | 5   | 5.25     | V                  |
| Common-mode input voltage, $V_{IC}$       |         |       |     | $\pm 12$ | V                  |
| Differential input voltage, $V_{ID}$      |         |       |     | $\pm 12$ | V                  |
| High-level enable-input voltage, $V_{IH}$ |         | 2     |     |          | V                  |
| Low-level enable-input voltage, $V_{IL}$  |         |       |     | 0.8      | V                  |
| High-level output current, $I_{OH}$       |         |       |     | $-400$   | $\mu\text{A}$      |
| Low-level output current, $I_{OL}$        |         |       |     | 16       | mA                 |
| Operating free-air temperature, $T_A$     | SN65175 | $-40$ |     | 85       | $^{\circ}\text{C}$ |
|                                           | SN75175 | 0     |     | 70       |                    |



# SN65175, SN75175

## QUADRUPLE DIFFERENTIAL LINE RECEIVERS

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**electrical characteristics over recommended ranges of common-mode input voltage, supply voltage and operating free-air temperature**

| PARAMETER                                            | TEST CONDITIONS                                                              | MIN   | TYP† | MAX      | UNIT             |
|------------------------------------------------------|------------------------------------------------------------------------------|-------|------|----------|------------------|
| $V_{IT+}$ Positive-going input threshold voltage     | $V_O = 2.7\text{ V}$ , $I_O = -0.4\text{ mA}$                                |       |      | 0.2      | V                |
| $V_{IT-}$ Negative-going input threshold voltage     | $V_O = 0.5\text{ V}$ , $I_O = 16\text{ mA}$                                  | -0.2‡ |      |          | V                |
| $V_{hys}$ Hysteresis voltage ( $V_{IT+} - V_{IT-}$ ) | See Figure 4                                                                 |       | 50   |          | mV               |
| $V_{IK}$ Enable-input clamp voltage                  | $I_I = -18\text{ mA}$                                                        |       |      | -1.5     | V                |
| $V_{OH}$ High-level output voltage                   | $V_{ID} = 200\text{ mV}$ , $I_{OH} = -400\text{ }\mu\text{A}$ , See Figure 1 | 2.7   |      |          | V                |
| $V_{OL}$ Low-level output voltage                    | $V_{ID} = -200\text{ mV}$ , See Figure 1                                     |       |      | 0.45     | V                |
|                                                      |                                                                              |       |      | 0.5      |                  |
| $I_{OZ}$ High-impedance-state output current         | $V_O = 0.4\text{ V to }2.4\text{ V}$                                         |       |      | $\pm 20$ | $\mu\text{A}$    |
| $I_I$ Line input current                             | Other input at 0 V, See Note 3                                               |       |      | 1        | mA               |
|                                                      |                                                                              |       |      | -0.8     |                  |
| $I_{IH}$ High-level enable-input current             | $V_{IH} = 2.7\text{ V}$                                                      |       |      | 20       | $\mu\text{A}$    |
| $I_{IL}$ Low-level enable-input current              | $V_{IL} = 0.4\text{ V}$                                                      |       |      | -100     | $\mu\text{A}$    |
| $r_i$ Input resistance                               |                                                                              | 12    |      |          | $\text{k}\Omega$ |
| $I_{OS}$ Short-circuit output current§               |                                                                              | -15   |      | -85      | mA               |
| $I_{CC}$ Supply current                              | Outputs disabled                                                             |       |      | 70       | mA               |

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 3: Refer to ANSI Standards EIA/TIA-422-B, RS-423-B, and RS-485 for exact conditions.

**switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 15\text{ pF}$ ,  $T_A = 25^\circ\text{C}$**

| PARAMETER                                                   | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------------------------------|-----------------|-----|-----|-----|------|
| $t_{PLH}$ Propagation delay time, low- to high-level output | See Figure 2    | 22  | 35  |     | ns   |
| $t_{PHL}$ Propagation delay time, high- to low-level output |                 | 25  | 35  |     | ns   |
| $t_{PZH}$ Output enable time to high level                  | See Figure 3    | 13  | 30  |     | ns   |
| $t_{PZL}$ Output enable time to low level                   |                 | 19  | 30  |     | ns   |
| $t_{PHZ}$ Output disable time from high level               | See Figure 3    | 26  | 35  |     | ns   |
| $t_{PLZ}$ Output disable time from low level                |                 | 25  | 35  |     | ns   |

## PARAMETER MEASUREMENT INFORMATION

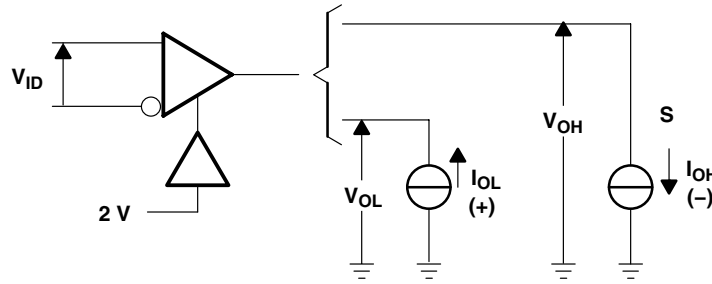
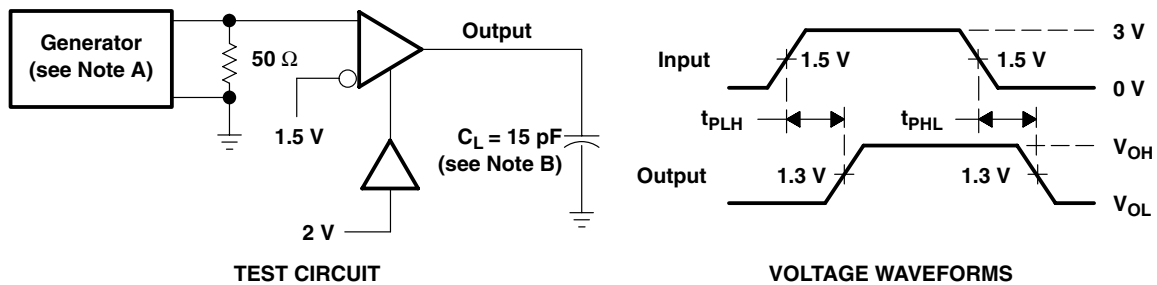


Figure 1.  $V_{OH}$ ,  $V_{OL}$



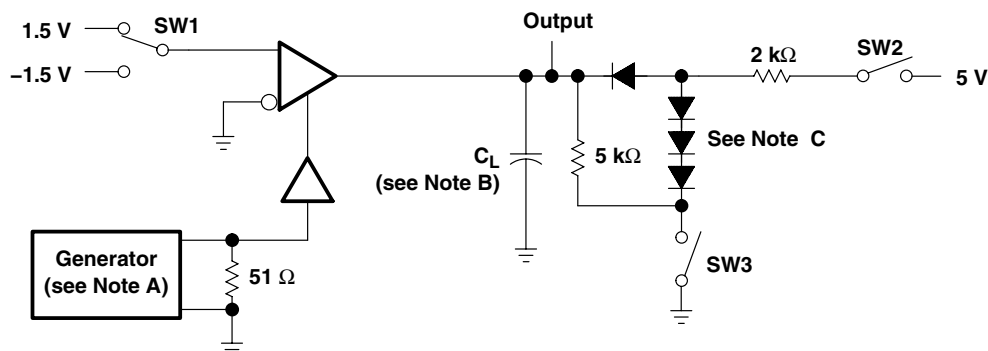
- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1 \text{ MHz}$ , duty cycle = 50%,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ ,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and stray capacitance.

Figure 2. Test Circuit and Voltage Waveforms

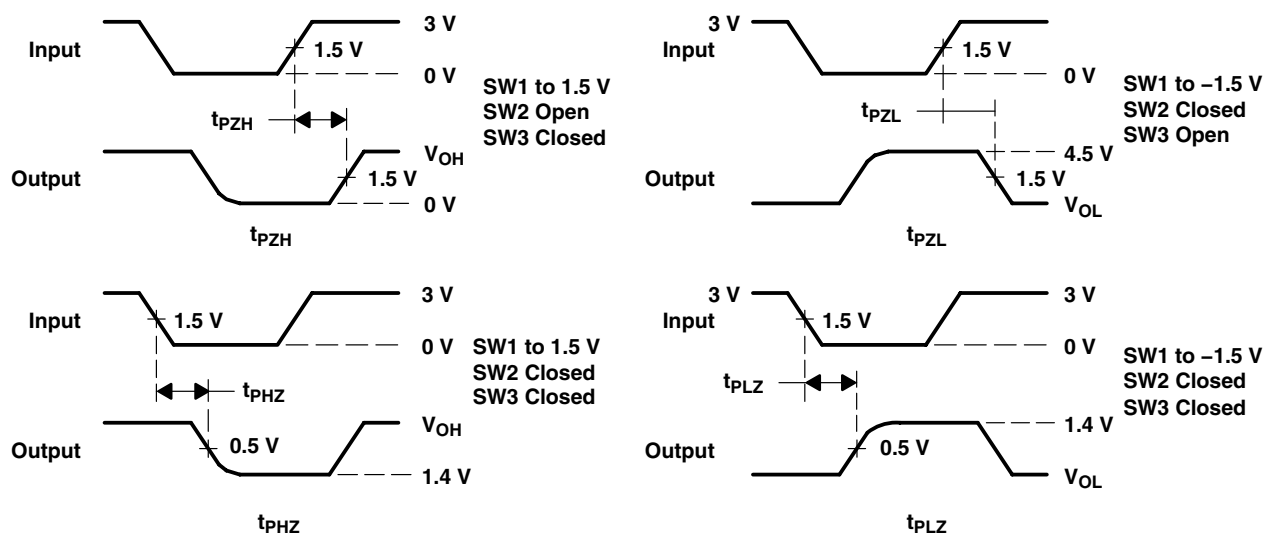
# SN65175, SN75175 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

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## PARAMETER MEASUREMENT INFORMATION



## TEST CIRCUIT



## VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1 \text{ MHz}$ , duty cycle = 50%,  $t_f \leq 6 \text{ ns}$ ,  $t_r \leq 6 \text{ ns}$ ,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and stray capacitance.  
C. All diodes are 1N916 or equivalent.

Figure 3. Test Circuit and Voltage Waveforms

# TYPICAL CHARACTERISTICS

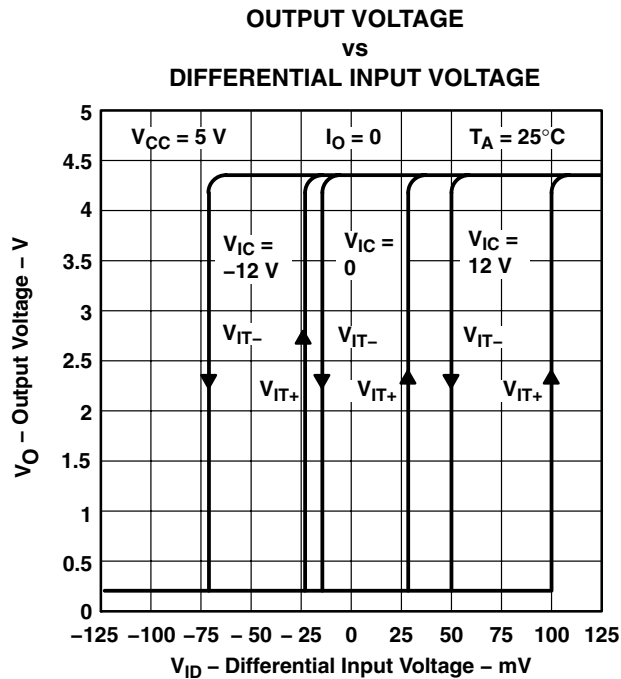


Figure 4

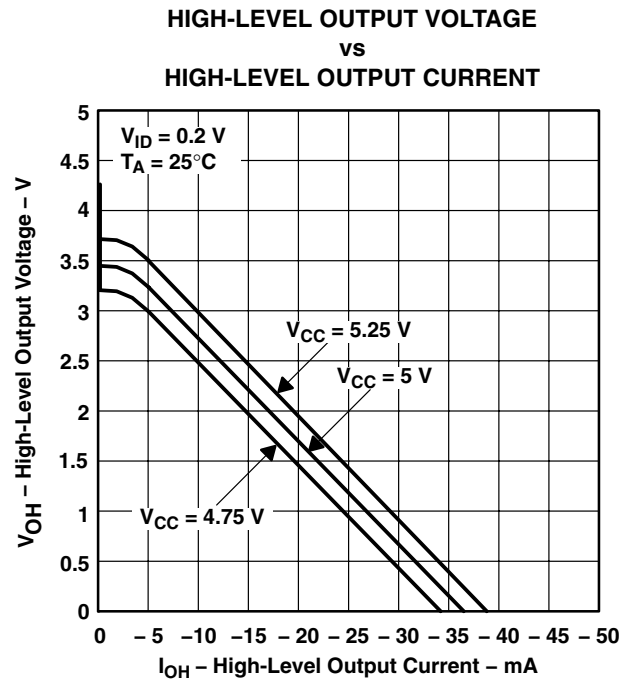


Figure 5

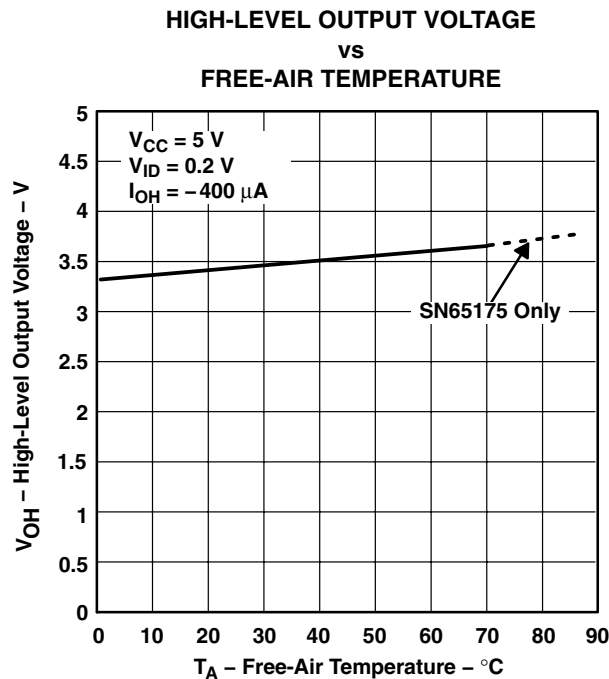


Figure 6

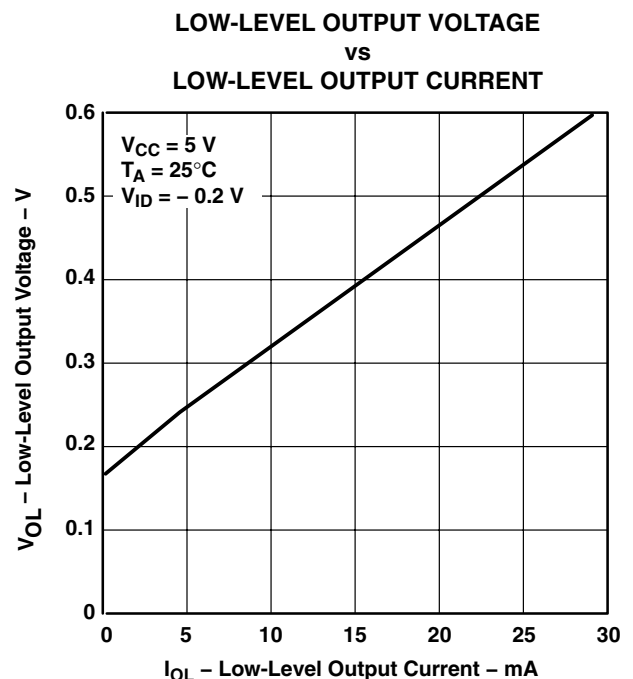


Figure 7

# SN65175, SN75175 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

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## TYPICAL CHARACTERISTICS

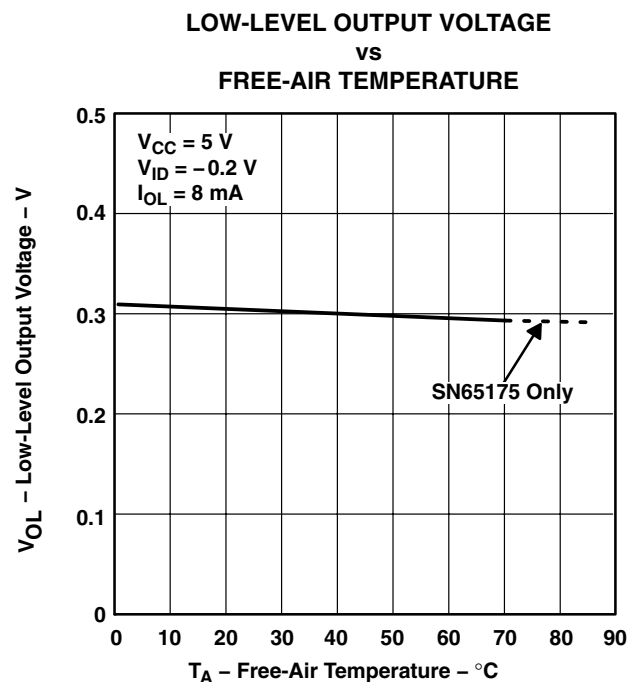


Figure 8

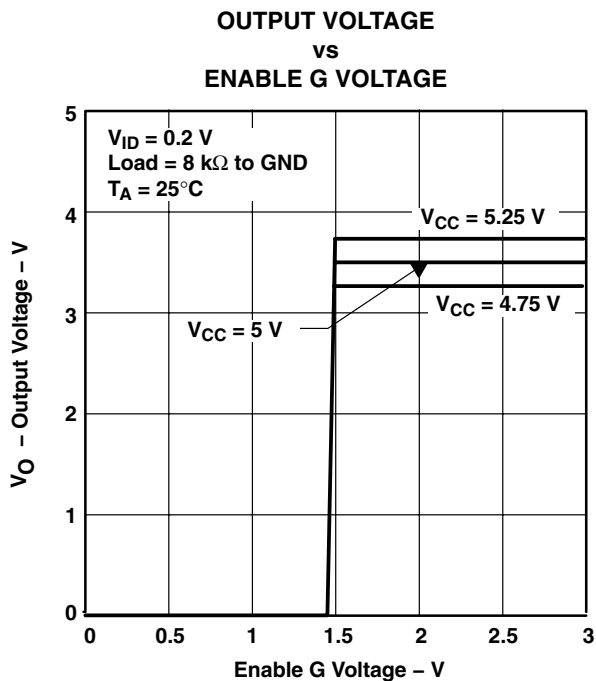


Figure 9

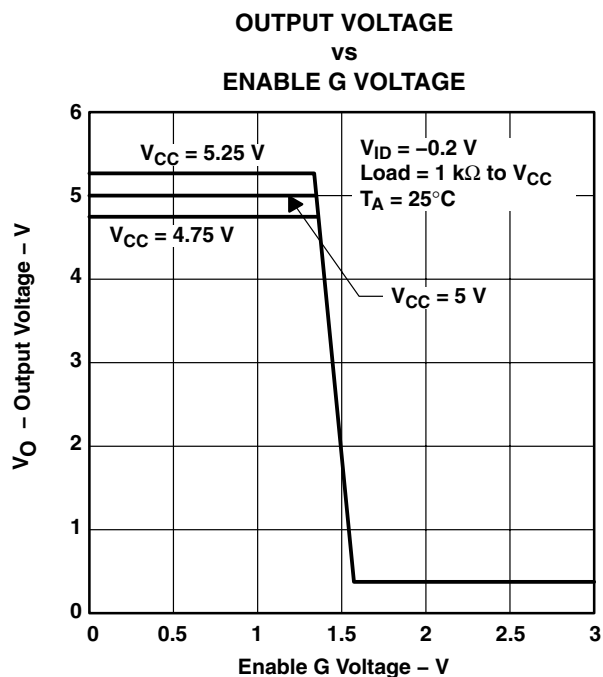


Figure 10

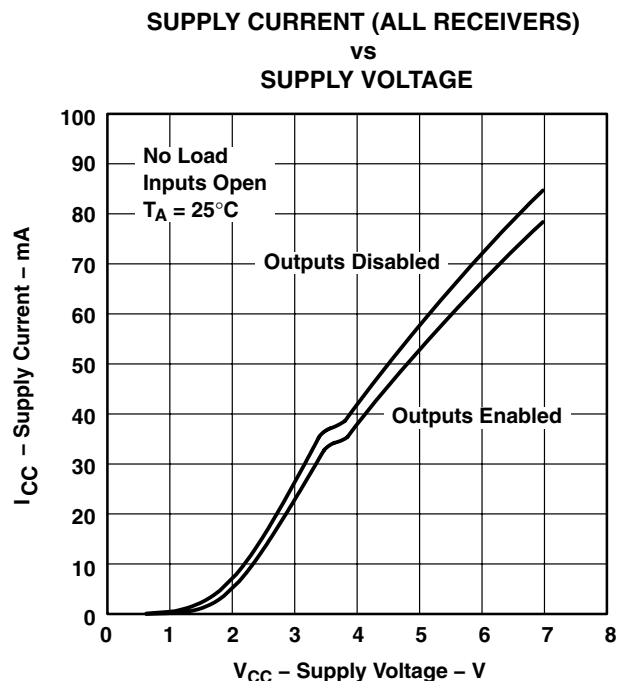


Figure 11

## TYPICAL CHARACTERISTICS

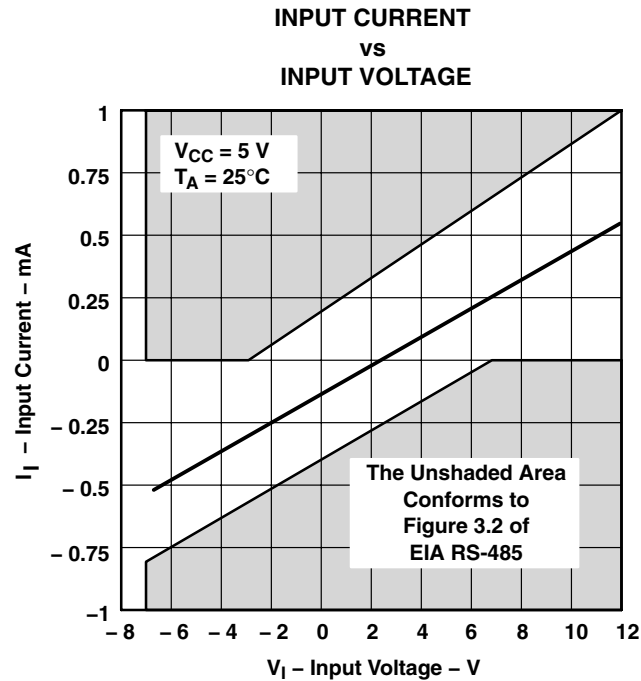
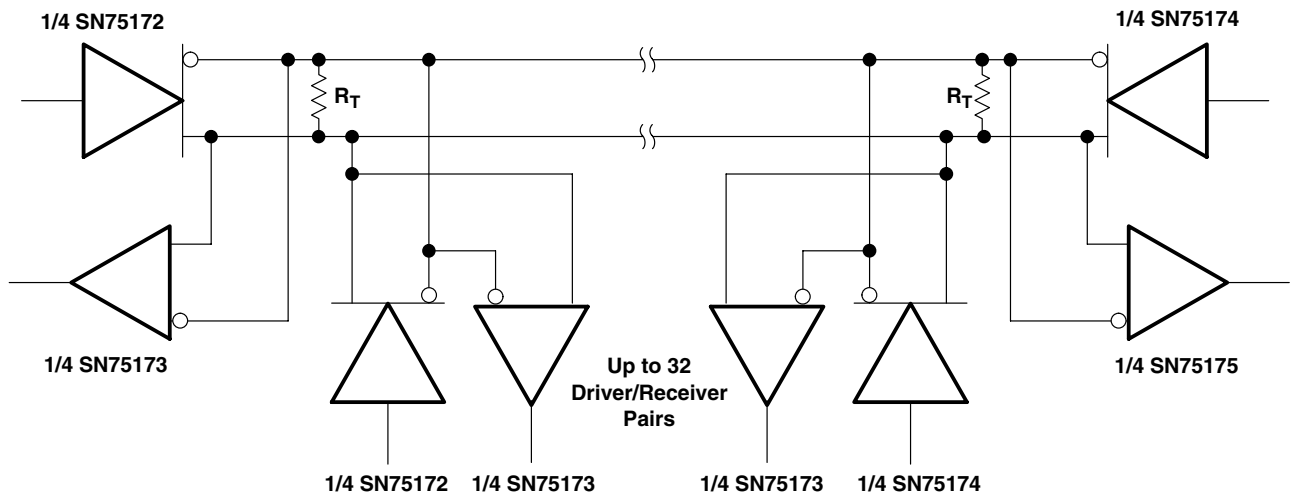


Figure 12

## APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance ( $R_T = Z_0$ ). Stub lengths off the main line should be kept as short as possible.

Figure 13. Typical Application Circuit

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN65175D         | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN65175DE4       | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN65175DG4       | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN65175DR        | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN65175DRE4      | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN65175DRG4      | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75175D         | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75175DE4       | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75175DG4       | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75175DR        | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75175DRE4      | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75175DRG4      | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75175J         | OBSOLETE              | CDIP         | J               | 16   |             | TBD                     | Call TI          | Call TI                      |
| SN75175N         | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN75175NE4       | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN75175NSR       | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75175NSRE4     | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75175NSRG4     | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS

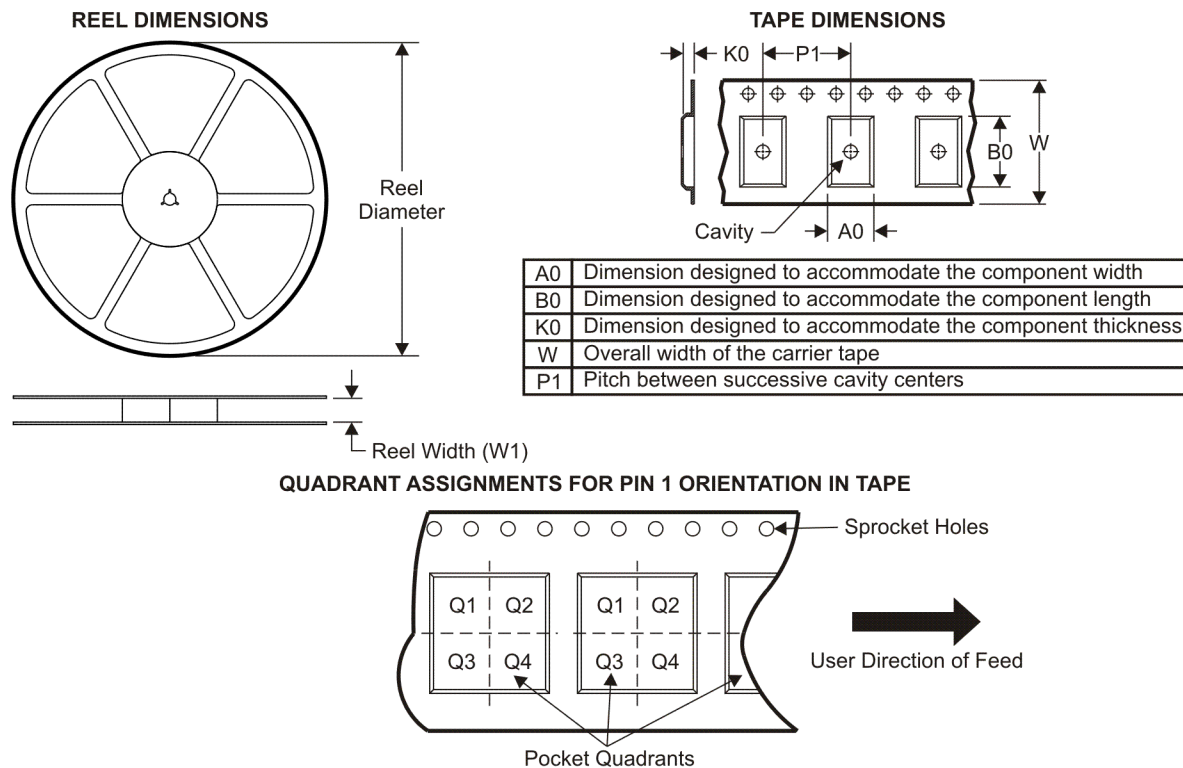
compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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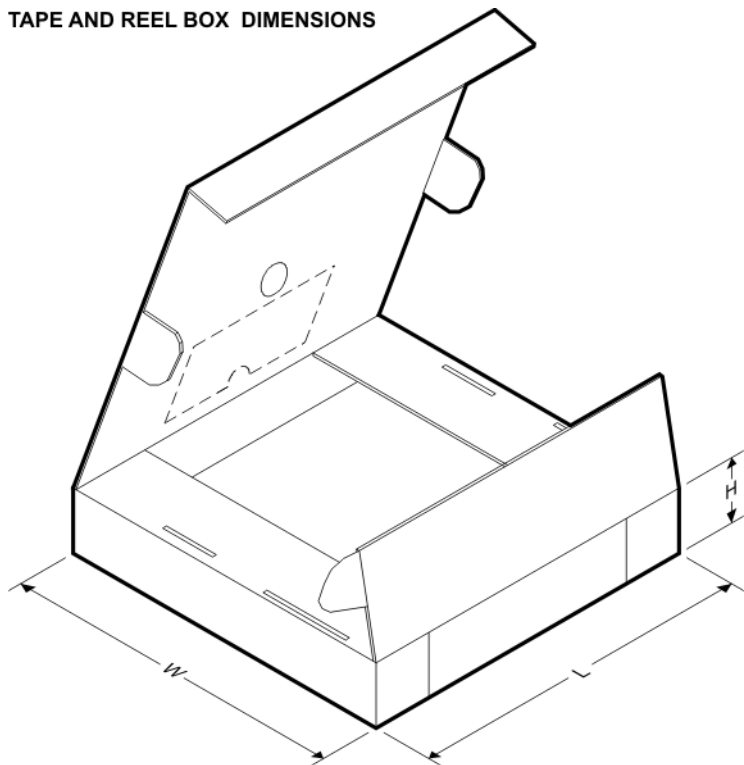
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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65175DR  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN75175DR  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN75175NSR | SO           | NS              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



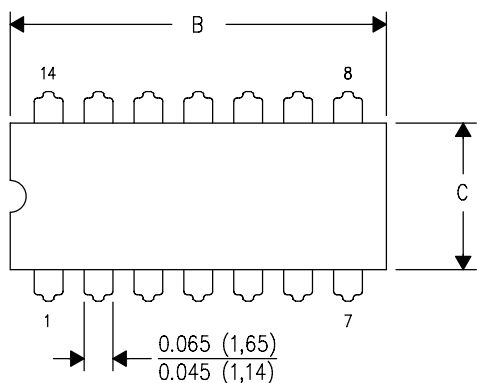
\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65175DR  | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| SN75175DR  | SOIC         | D               | 16   | 2500 | 346.0       | 346.0      | 33.0        |
| SN75175NSR | SO           | NS              | 16   | 2000 | 346.0       | 346.0      | 33.0        |

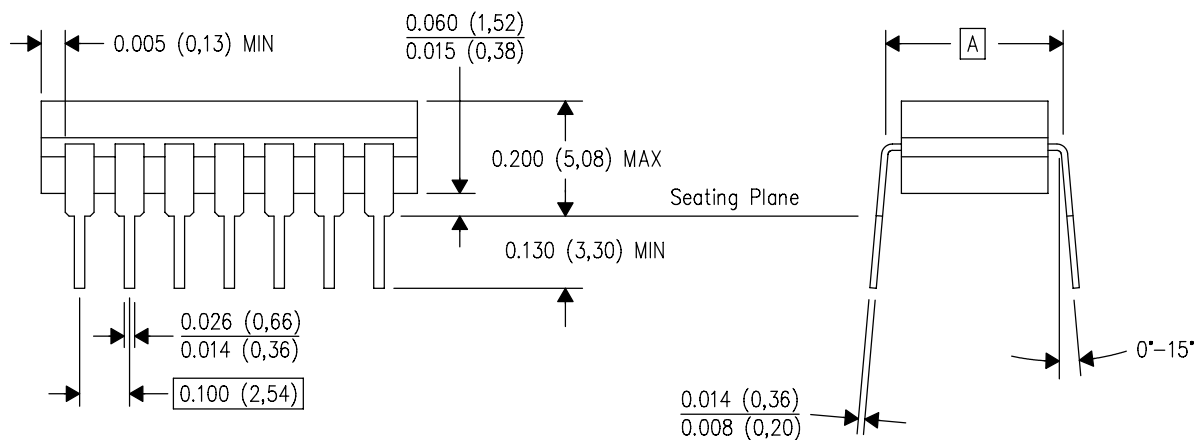
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



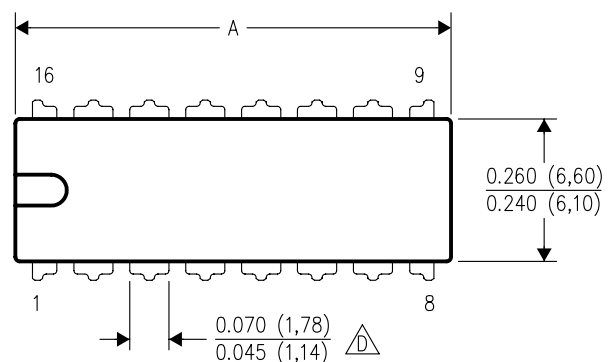
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

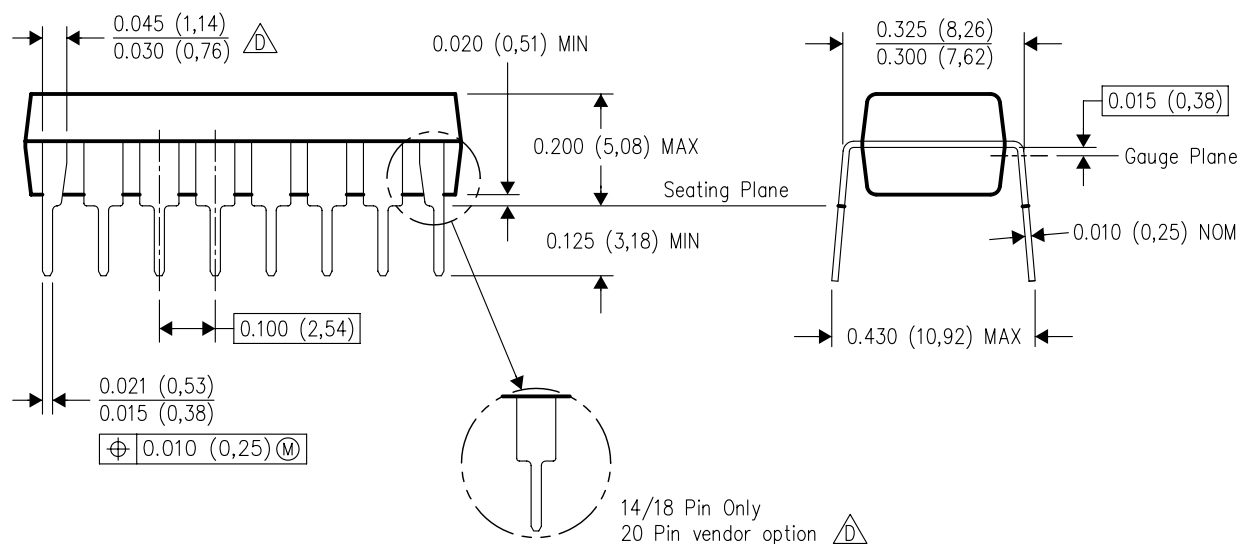
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |

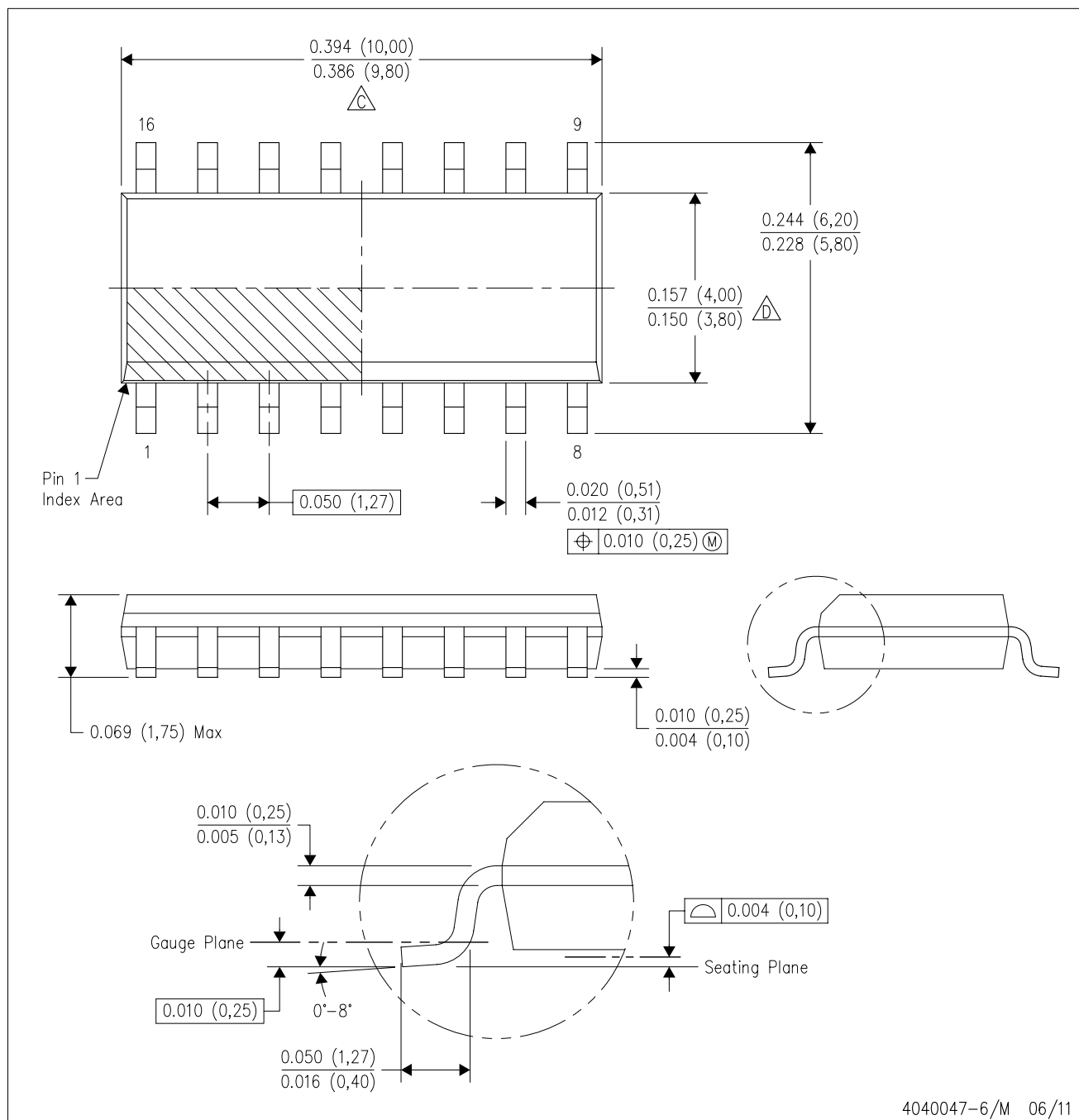


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

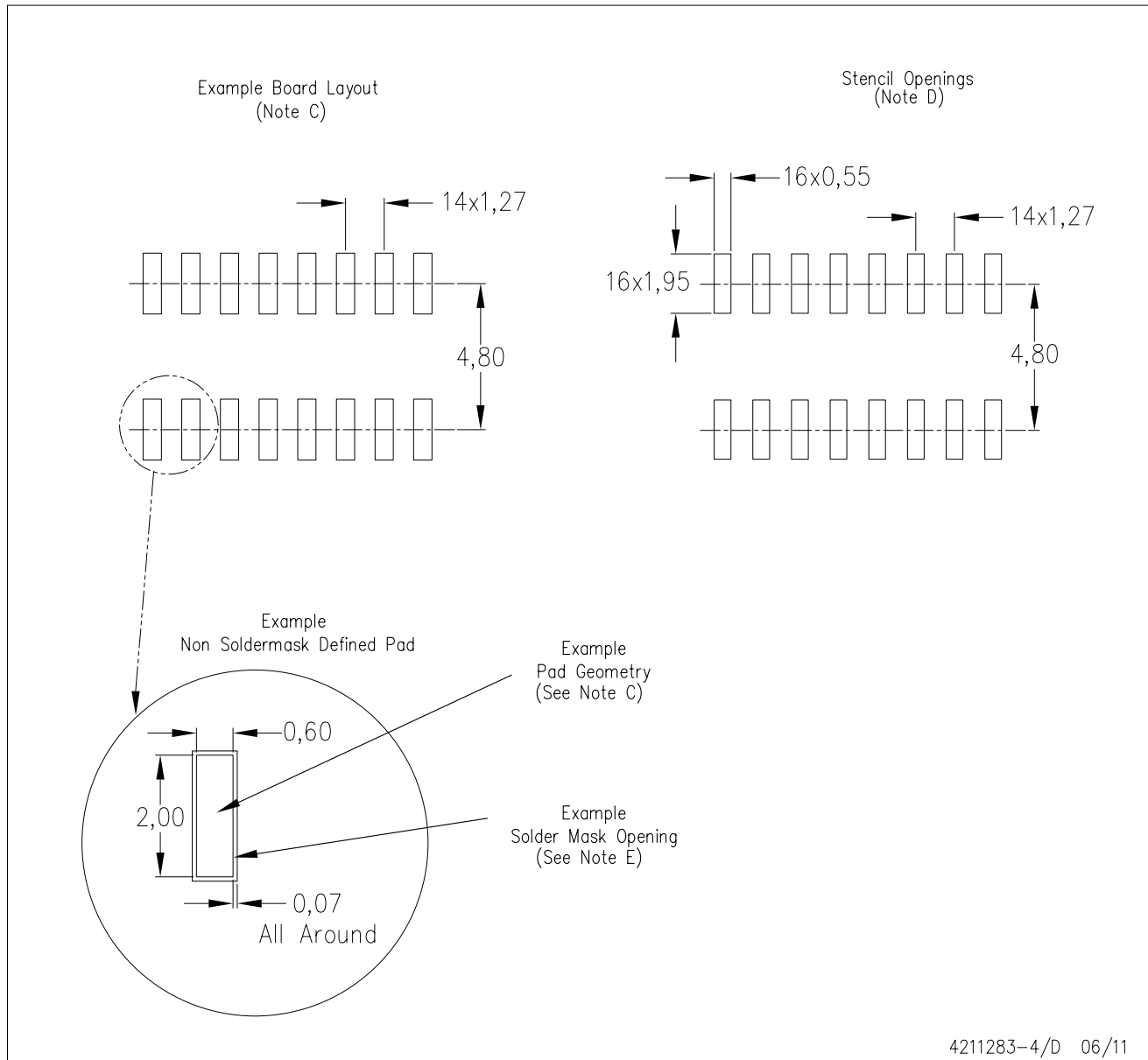
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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|                               |                                                                                          |
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