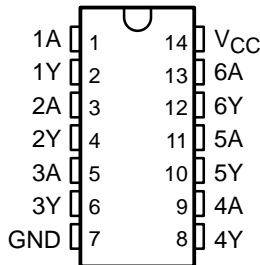


SN54LV14A, SN74LV14A HEX SCHMITT-TRIGGER INVERTERS

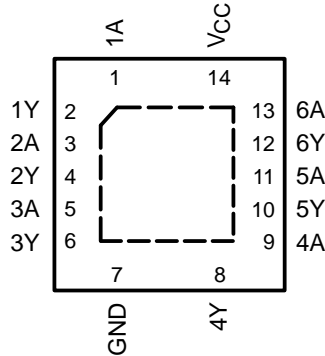
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- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 10 V at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

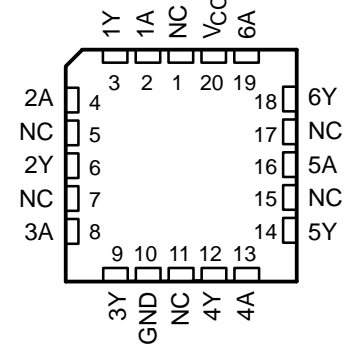
SN54LV14A . . . J OR W PACKAGE
SN74LV14A . . . D, DB, DGV, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LV14A . . . RGY PACKAGE
(TOP VIEW)



SN54LV14A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These hex Schmitt-trigger inverters are designed for 2-V to 5.5-V V_{CC} operation.

The 'LV14A devices contain six independent inverters. These devices perform the Boolean function $Y = \bar{A}$.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Tape and reel	SN74LV14ARGYR	LV14A
	SOIC – D	Tube	SN74LV14AD	LV14A
		Tape and reel	SN74LV14ADR	
	SOP – NS	Tape and reel	SN74LV14ANSR	74LV14A
	SSOP – DB	Tape and reel	SN74LV14ADBR	LV14A
	TSSOP – PW	Tape and reel	SN74LV14APWR	LV14A
TVSOP – DGV	Tape and reel	SN74LV14ADGVR	LV14A	
-55°C to 125°C	CDIP – J	Tube	SNJ54LV14AJ	SNJ54LV14AJ
	CFP – W	Tube	SNJ54LV14AW	SNJ54LV14AW
	LCCC – FK	Tube	SNJ54LV14AFK	SNJ54LV14AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
INSTRUMENTS**

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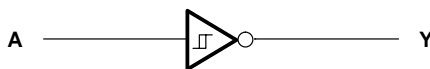
SN54LV14A, SN74LV14A HEX SCHMITT-TRIGGER INVERTERS

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FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	86°C/W
(see Note 3): DB package	96°C/W
(see Note 3): DGV package	127°C/W
(see Note 3): NS package	76°C/W
(see Note 3): PW package	113°C/W
(see Note 4): RGY package	47°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

SN54LV14A, SN74LV14A HEX SCHMITT-TRIGGER INVERTERS

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recommended operating conditions (see Note 5)

		SN54LV14A		SN74LV14A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	V _{CC} × 0.3		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	-50	-50		μA
		V _{CC} = 2.3 V to 2.7 V	-2	-2		mA
		V _{CC} = 3 V to 3.6 V	-6	-6		
		V _{CC} = 4.5 V to 5.5 V	-12	-12		
I _{OL}	Low-level output current	V _{CC} = 2 V	50	50		μA
		V _{CC} = 2.3 V to 2.7 V	2	2		mA
		V _{CC} = 3 V to 3.6 V	6	6		
		V _{CC} = 4.5 V to 5.5 V	12	12		
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LV14A, SN74LV14A HEX SCHMITT-TRIGGER INVERTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV14A			SN74LV14A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{T+} Positive-going threshold		2.5 V	1.75			1.75			V
		3.3 V	2.31			2.31			
		5 V	3.5			3.5			
V _{T-} Negative-going threshold		2.5 V	0.75			0.75			V
		3.3 V	0.99			0.99			
		5 V	1.5			1.5			
ΔV _T Hysteresis (V _{T+} – V _{T-})		2.5 V	0.25	1		0.25	1		V
		3.3 V	0.33	1.32		0.33	1.32		
		5 V	0.5	2		0.5	2		
V _{OH}	I _{OH} = –50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = –2 mA	2.3 V	2			2			
	I _{OH} = –6 mA	3 V	2.48			2.48			
	I _{OH} = –12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I _{OL} = 2 mA	2.3 V	0.4			0.4			
	I _{OL} = 6 mA	3 V	0.44			0.44			
	I _{OL} = 12 mA	4.5 V	0.55			0.55			
I _I	V _I = V _{CC} or GND	0 V to 5.5 V	±1			±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V	5			5			μA
C _i	V _I = V _{CC} or GND	3.3 V	2.3			2.3			pF
		5 V	2.3			2.3			

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV14A		SN74LV14A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	C _L = 15 pF	10.2*	19.7*	1*	22*	1	22	ns	
			C _L = 50 pF	13.3	24	1	27	1	27		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54LV14A		SN74LV14A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	C _L = 15 pF	7.3*	12.8*	1*	15.9*	1	15	ns	
			C _L = 50 pF	9.6	16.3	1	19.4	1	18.5		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV14A		SN74LV14A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	$C_L = 15\text{ pF}$	5.1*	8.6*	1*	10*	1	10	ns	
			$C_L = 50\text{ pF}$	6.7	10.6	1	12	1	12		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 6)

PARAMETER		SN74LV14A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}	0.2	0.8		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	-0.1	-0.8		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	3.1			V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage		0.99		V

NOTE 6: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	8.8	pF
			5 V	9.6	

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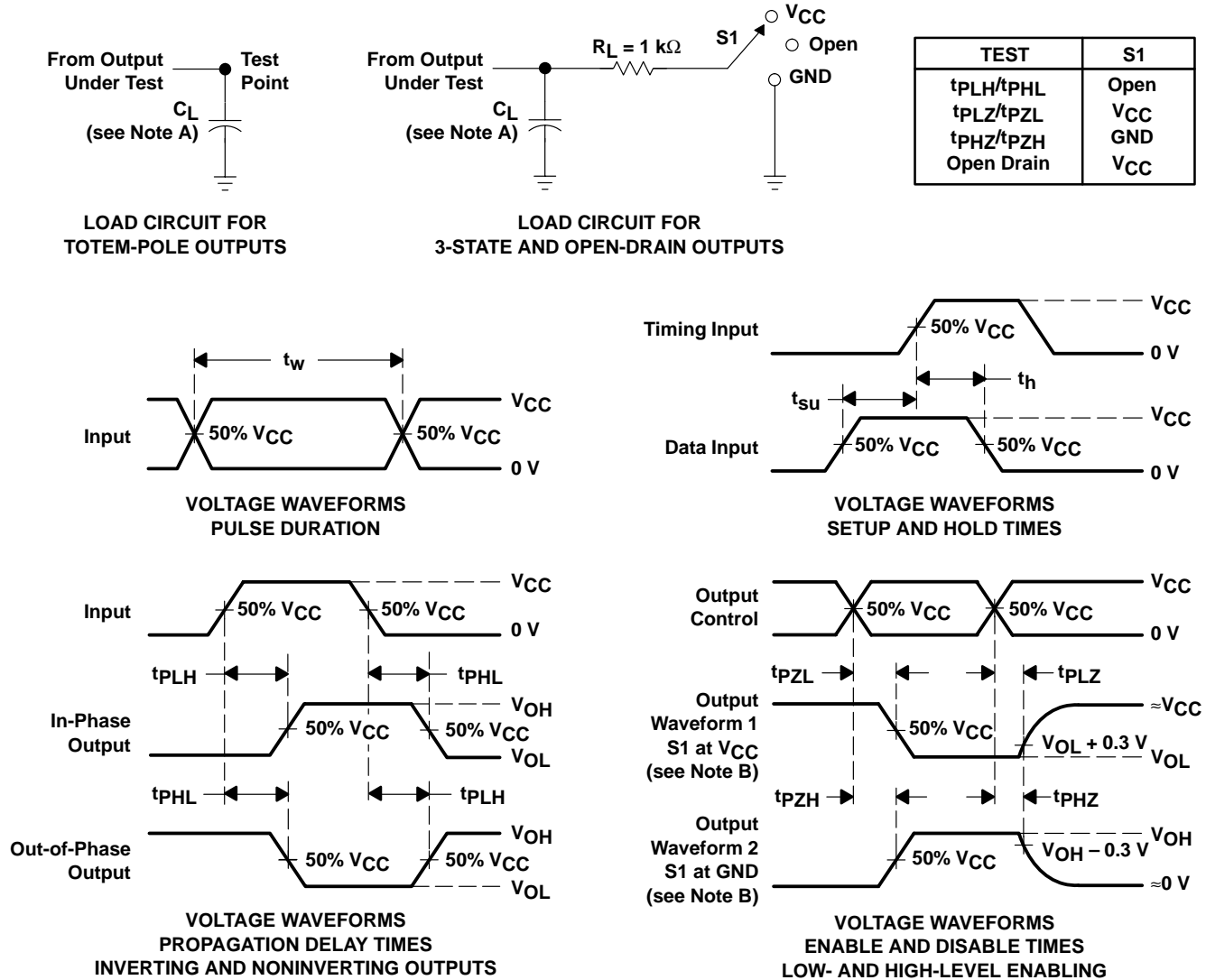


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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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