

SN54HCT74, SN74HCT74 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SCLS169B – DECEMBER 1982 – REVISED MAY 1997

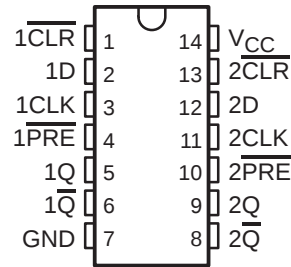
- Inputs Are TTL-Voltage Compatible
- Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

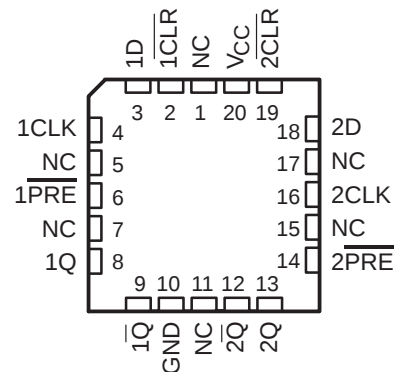
The 'HCT74 contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the data (D) input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN54HCT74 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HCT74 is characterized for operation from -40°C to 85°C .

SN54HCT74 . . . J OR W PACKAGE
SN74HCT74 . . . D, N, OR PW PACKAGE
(TOP VIEW)



SN54HCT74 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS				OUTPUT	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H [†]	H [†]
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	Q ₀

[†] This configuration is unstable; that is, it does not persist when $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.



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**TEXAS
INSTRUMENTS**

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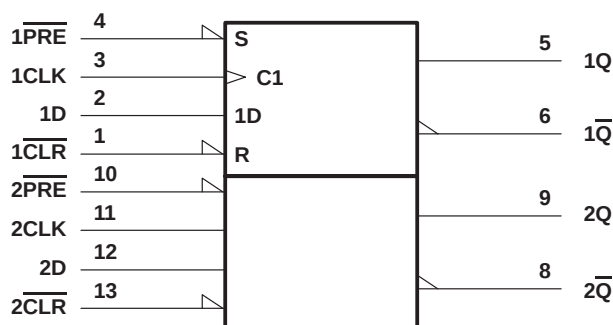
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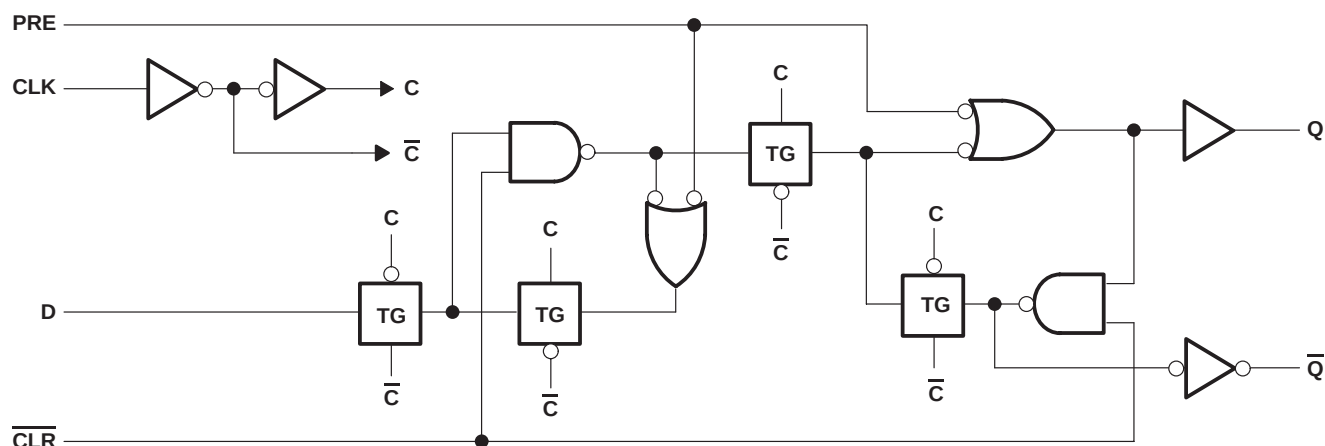
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, N, PW, and W packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	127°C/W
N package	78°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

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recommended operating conditions

			SN54HCT74			SN74HCT74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 4.5 V to 5.5 V	2			2			V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
t _t	Input transition (rise and fall) time		0		500	0		500	ns
T _A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HCT74		SN74HCT74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = –20 µA	4.5 V	4.4	4.499		4.4		4.4		V
		I _{OH} = –4 mA		3.98	4.3		3.7		3.84		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 µA	4.5 V		0.001	0.1		0.1		0.1	V
		I _{OL} = 4 mA			0.17	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		5.5 V			4		80		40	µA
ΔI _{CC} [†]	One input at 0.5 V or 2.4 V, Other inputs at 0 or V _{CC}		5.5 V		1.4	2.4		3		2.9	mA
C _i			4.5 V to 5.5 V		3	10		10		10	pF

[†] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V _{CC}	T _A = 25°C		SN54HCT74		SN74HCT74		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		4.5 V	0	27	0	18	0	22	MHz
			5.5 V	0	30	0	20	0	24	
t _w	Pulse duration	PRE or CLR low	4.5 V	16		24		20		ns
			5.5 V	14		21		18		
	CLK high or low		4.5 V	18		27		23		
			5.5 V	16		24		21		
t _{su}	Setup time before CLK↑	Data	4.5 V	12		18		15		ns
			5.5 V	11		16		14		
	PRE or CLR inactive		4.5 V	0		0		0		
			5.5 V	0		0		0		
t _h	Hold time, data after CLK↑		4.5 V	0		0		0		ns
			5.5 V	0		0		0		

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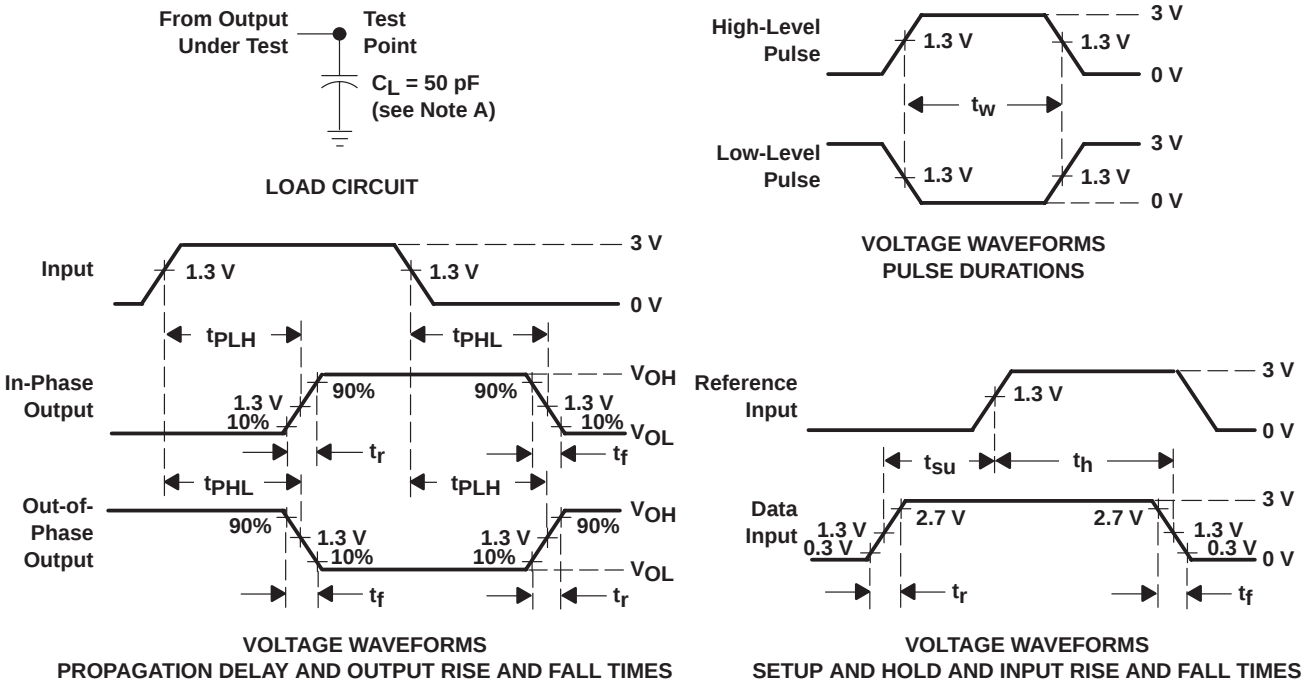
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT74		SN74HCT74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			4.5 V	27	40		18		22		MHz
			5.5 V	30	46		20		24		
t_{pd}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	4.5 V		21	35		53		44	ns
			5.5 V		17	31		48		40	
	CLK	Q or $\overline{Q}$	4.5 V		20	28		42		35	
			5.5 V		18	25		38		31	
t_t		Q or $\overline{Q}$	4.5 V		8	15		22		19	ns
			5.5 V		7	14		20		17	

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	35	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - C. For clock inputs, $f_{\max}$ is measured when the input duty cycle is 50%.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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