

SN54HC163, SN74HC163 4-BIT SYNCHRONOUS BINARY COUNTERS

SCLS298A – JANUARY 1996 – REVISED MAY 1997

- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

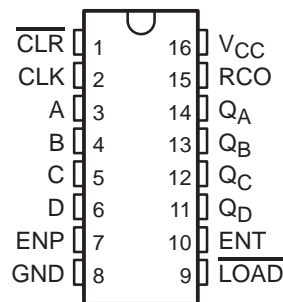
These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'HC163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

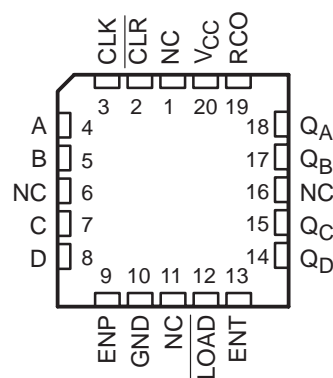
The clear function for the 'HC163 is synchronous. A low level at the clear ($\overline{\text{CLR}}$) input sets all four of the flip-flop outputs low after the next low-to-high transition of CLK, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the $\overline{\text{Q}}$ outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to $\overline{\text{CLR}}$ to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. ENP, ENT, and a ripple-carry output (RCO) are instrumental in accomplishing this function. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

SN54HC163 . . . J OR W PACKAGE
SN74HC163 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC163 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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**TEXAS
INSTRUMENTS**

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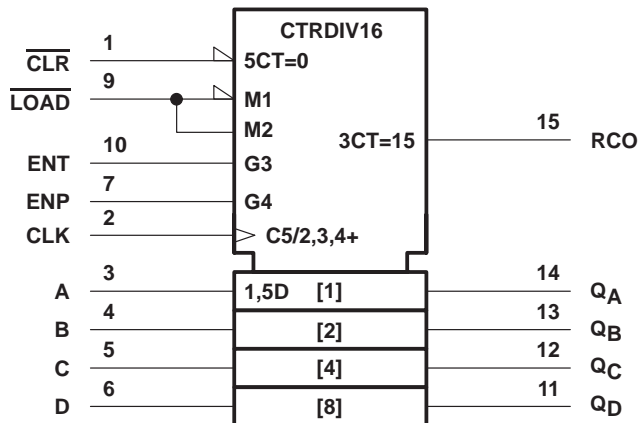
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description (continued)

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

The SN54HC163 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC163 is characterized for operation from -40°C to 85°C .

logic symbol†

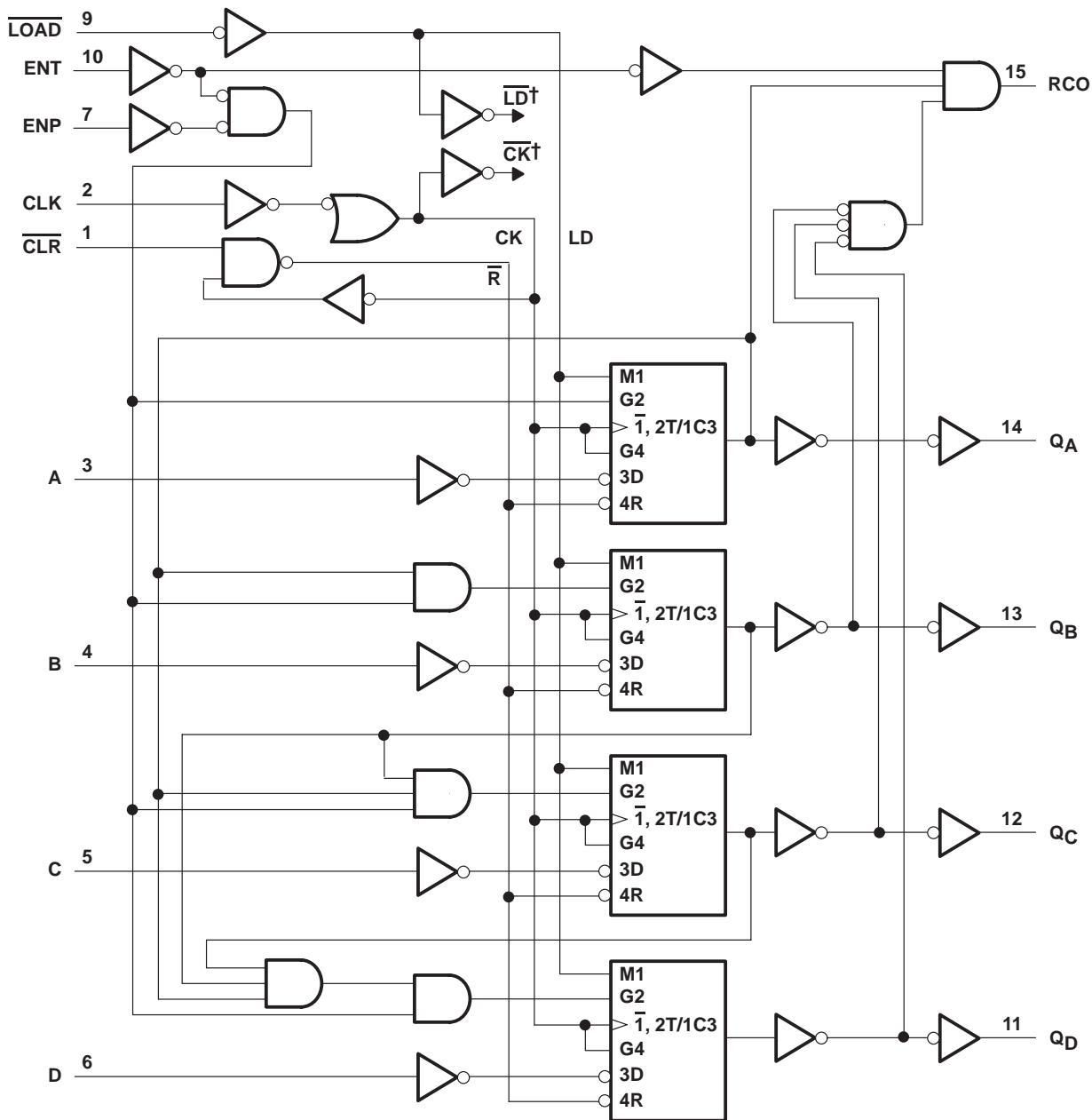


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, N, and W packages.

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logic diagram (positive logic)



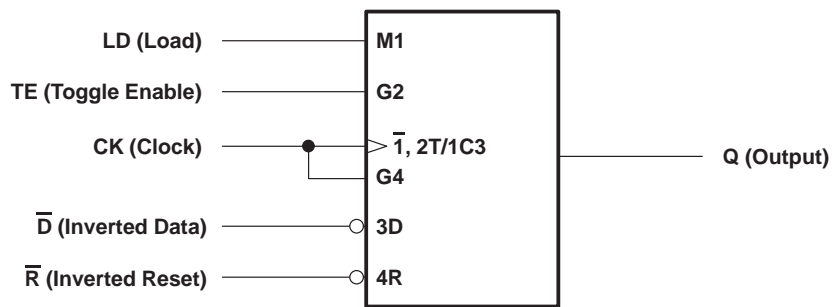
† For simplicity, routing of complementary signals $\overline{\text{LD}}$ and $\overline{\text{CK}}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

Pin numbers shown are for the D, J, N, and W packages.

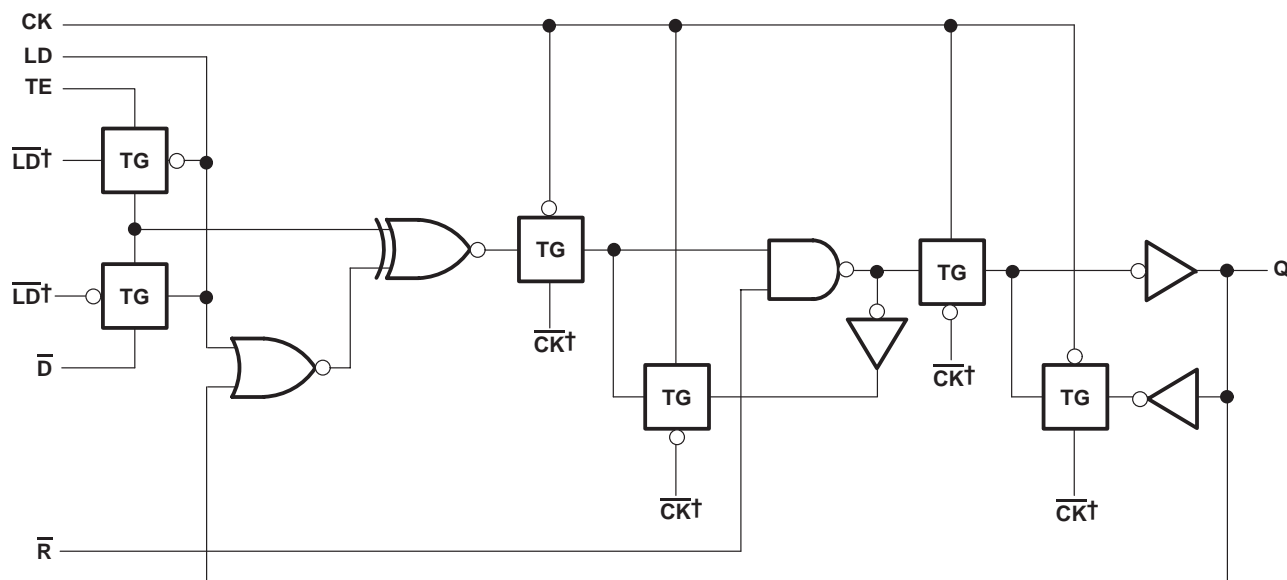
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logic symbol, each D/T flip-flop



logic diagram, each D/T flip-flop (positive logic)

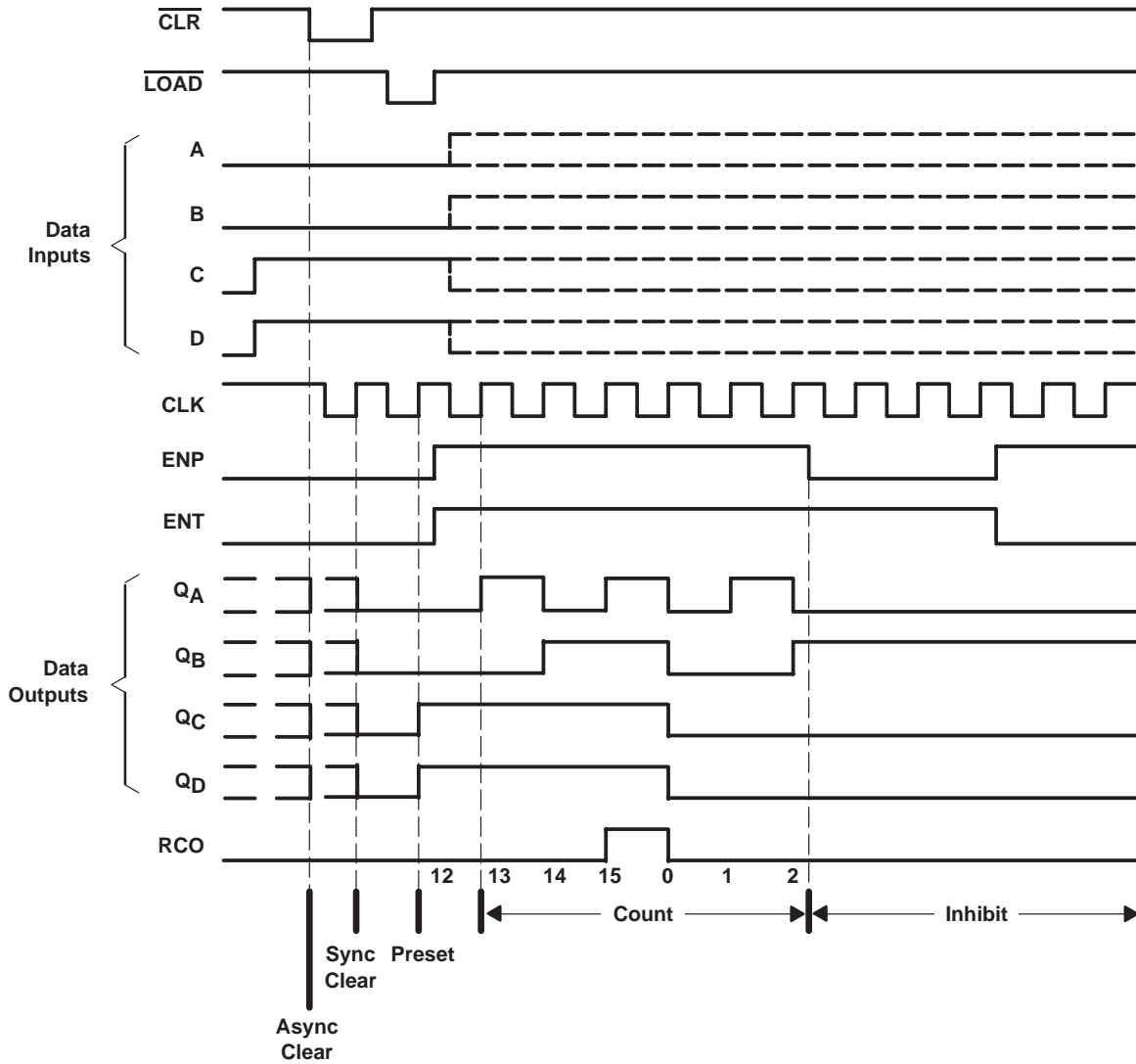


† The origins of \overline{LD} and \overline{CK} are shown in the logic diagram of the overall device.

typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (synchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



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absolute maximum ratings over operating free-air temperature†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	113°C/W
N package	78°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		SN54HC163			SN74HC163			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V		1.5	1.5		V	
		$V_{CC} = 4.5$ V		3.15	3.15			
		$V_{CC} = 6$ V		4.2	4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0	0.5	0	0.5	V
		$V_{CC} = 4.5$ V		0	1.35	0	1.35	
		$V_{CC} = 6$ V		0	1.8	0	1.8	
V_I	Input voltage	0	V_{CC}		0	V_{CC}		V
V_O	Output voltage	0	V_{CC}		0	V_{CC}		V
t_t^\ddagger	Input transition (rise and fall) time	$V_{CC} = 2$ V		0	1000	0	1000	ns
		$V_{CC} = 4.5$ V		0	500	0	500	
		$V_{CC} = 6$ V		0	400	0	400	
T_A	Operating free-air temperature	-55	125		-40	85		°C

‡ If this device is used in the threshold region (from $V_{ILmax} = 0.5$ V to $V_{IHmin} = 1.5$ V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_t = 1000$ ns and $V_{CC} = 2$ V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HC163		SN74HC163		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I _{OH} = -4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I _{OH} = -5.2 mA	6 V	5.48	5.8		5.2		5.34		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I _{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V			8		160		80	μA
C _i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25°C		SN54HC163		SN74HC163		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
f _{clock}	Clock frequency	2 V	0	6	0	4.2	0	5	MHz	
		4.5 V	0	31	0	21	0	25		
		6 V	0	36	0	25	0	29		
t _w	Pulse duration	CLK high or low	2 V	80		120		100	ns	
			4.5 V	16		24		20		
			6 V	14		20		17		
t _{su}	Setup time before CLK↑	A, B, C, or D	2 V	150		225		190	ns	
			4.5 V	30		45		38		
			6 V	26		38		32		
			LOAD low	2 V	135		205			170
				4.5 V	27		41			34
				6 V	23		35			29
		ENP, ENT	2 V	170		255		215		
			4.5 V	34		51		43		
			6 V	29		43		37		
		CLR low	2 V	160		240		200		
			4.5 V	32		48		40		
			6 V	27		41		34		
		CLR inactive	2 V	160		240		200		
			4.5 V	32		48		40		
			6 V	27		41		34		
t _h	Hold time, all synchronous inputs after CLK↑	2 V	0		0		0	ns		
		4.5 V	0		0		0			
		6 V	0		0		0			



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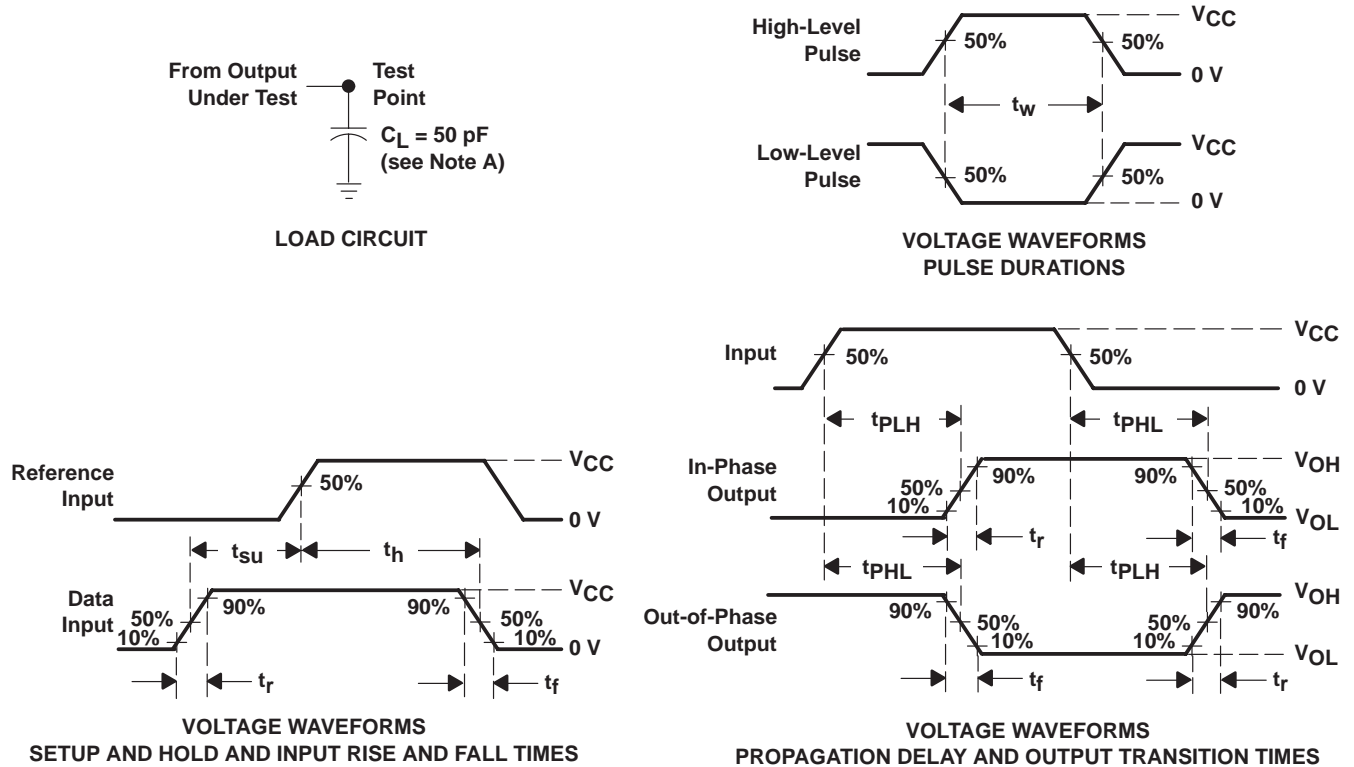
switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC163		SN74HC163		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	14		4.2		5	MHz	
			4.5 V	31	40		21		25		
			6 V	36	44		25		29		
t_{pd}	CLK	RCO	2 V		83	215		325		270	ns
			4.5 V		24	43		65		54	
			6 V		20	37		55		46	
		Any Q	2 V		80	205		310		255	
			4.5 V		25	41		62		51	
			6 V		21	35		53		43	
	ENT	RCO	2 V		62	195		295		245	
			4.5 V		17	39		59		49	
			6 V		14	33		50		42	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load	60	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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APPLICATION INFORMATION

n-bit synchronous counters

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 'HC163 count in binary. Virtually any count mode (modulo-N, N_1 -to- N_2 , N_1 -to-maximum) can be used with this fast look-ahead circuit.

The application circuit shown in Figure 2 is not valid for clock frequencies above 18 MHz (at 25°C and 4.5-V V_{CC}). The reason for this is that there is a glitch that is produced on the second stage's RCO and every succeeding stage's RCO. This glitch is common to all HC vendors that Texas Instruments has evaluated, in addition to the bipolar equivalents (LS, ALS, AS).



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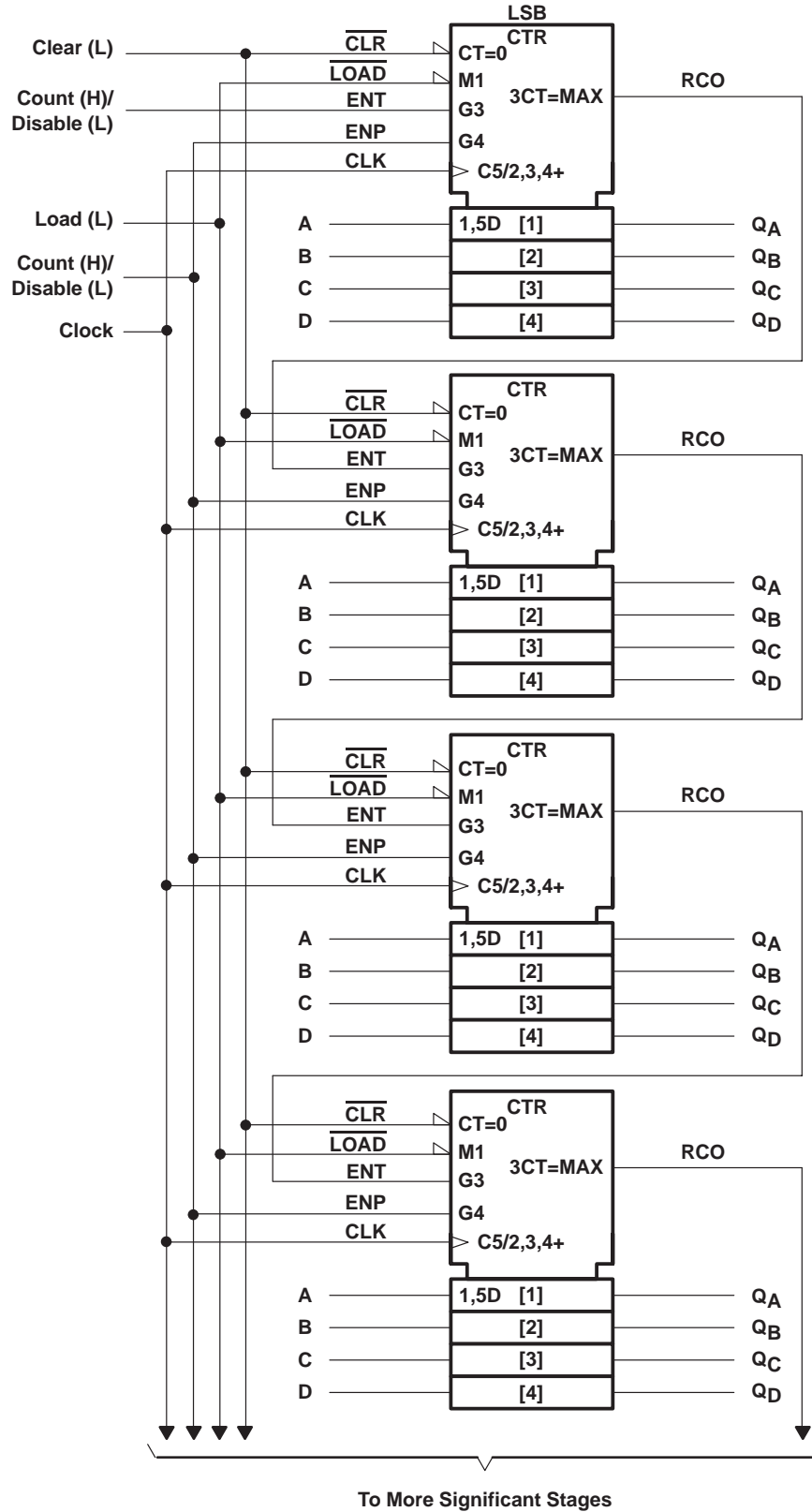


Figure 2

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The glitch on RCO is caused because the propagation delay of the rising edge of Q_A of the second stage is shorter than the propagation delay of the falling edge of ENT. RCO is the product of ENT, Q_A , Q_B , Q_C , and Q_D ($ENT \times Q_A \times Q_B \times Q_C \times Q_D$). The resulting glitch is about 7–12 ns in duration. Figure 3 shows the condition in which the glitch occurs. For simplicity, only two stages are being considered, but the results can be applied to other stages. Q_B , Q_C , and Q_D of the first and second stage are at logic one, and Q_A of both stages are at logic zero (1110 1110) after the first clock pulse. On the rising edge of the second clock pulse, Q_A and RCO of the first stage go high. On the rising edge of the third clock pulse, Q_A and RCO of the first stage return to a low level, and Q_A of the second stage goes to a high level. At this time, the glitch on RCO of the second stage appears because of the race condition inside the chip.

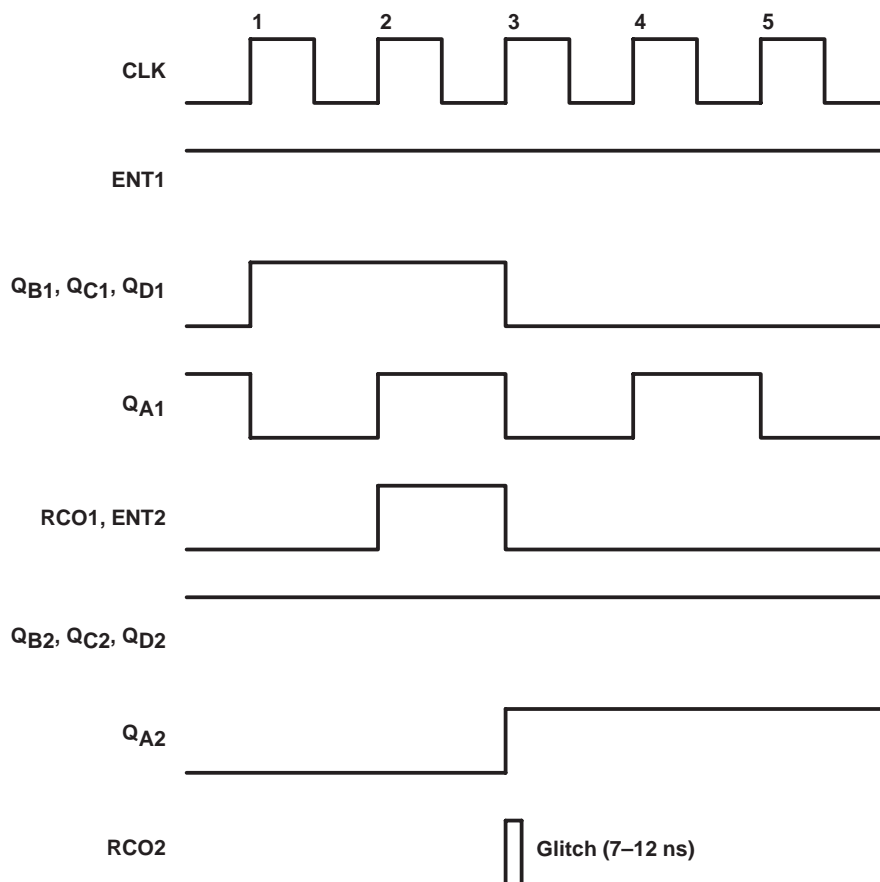


Figure 3

The glitch causes a problem in the next stage (stage three) if the glitch is still present when the next rising clock edge appears (clock pulse 4). To ensure that this does not happen, the clock frequency must be less than the inverse of the sum of the clock-to-RCO propagation delay and the glitch duration (t_g). In other words, $f_{max} = 1/(t_{pd \text{ CLK-to-RCO}} + t_g)$. For example, at 25°C at 4.5-V V_{CC} , the clock-to-RCO propagation delay is 43 ns and the maximum duration of the glitch is 12 ns. Therefore, the maximum clock frequency that the cascaded counters can use is 18 MHz. The following tables contain the f_{clock} , t_w , and f_{max} specifications for applications that use more than two 'HC163 devices cascaded together.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

	V _{CC}	T _A = 25°C		SN54HC163		SN74HC163		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock} Clock frequency	2 V	0	3.6	0	2.5	0	2.9	MHz
	4.5 V	0	18	0	12	0	14	
	6 V	0	21	0	14	0	17	
t _w Pulse duration, CLK high or low	2 V	140		200		170		ns
	4.5 V	28		40		36		
	6 V	24		36		30		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C		SN54HC163		SN74HC163		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			2 V	3.6		2.5		2.9		MHz
			4.5 V	18		12		14		
			6 V	21		14		17		

NOTE 3: These limits apply only to applications that use more than two 'HC163 devices cascaded together.

If the 'HC163 are used as a single unit, or only two cascaded together, then the maximum clock frequency that the device can use is not limited because of the glitch. In these situations, the device can be operated at the maximum specifications.

A glitch can appear on RCO of a single 'HC163 device, depending on the relationship of ENT to CLK. Any application that uses RCO to drive any input except an ENT of another cascaded 'HC163 must take this into consideration.

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