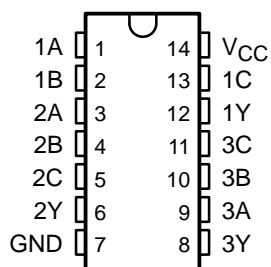


# SN54ALS11A, SN54AS11, SN74ALS11A, SN74AS11 TRIPLE 3-INPUT POSITIVE-AND GATES

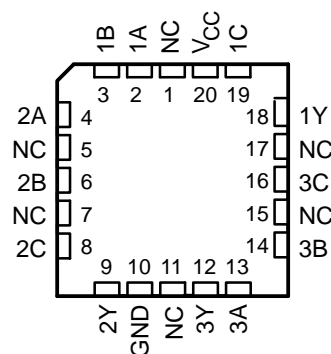
SDAS009D – MARCH 1984 – REVISED NOVEMBER 2002

- 4.5-V to 5.5-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 5.5 ns at 5 V

SN54ALS11A, . . . J OR W PACKAGE  
SN54AS11 . . . J PACKAGE  
SN74ALS11A, SN74AS11 . . . D, N, OR NS PACKAGE  
(TOP VIEW)



SN54ALS11A, SN54AS11 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

These devices contain three independent 3-input positive-AND gates. They perform the Boolean functions  $Y = A \cdot B \cdot C$  or  $Y = \overline{A} + \overline{B} + \overline{C}$  in positive logic.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
0°C to 70°C	PDIP – N	Tube	SN74ALS11AN	SN74ALS11AN	
			SN74AS11N	SN74AS11N	
	SOIC – D	Tube	SN74ALS11AD	ALS11A	
			Tape and reel		SN74ALS11ADR
			Tape and reel	SN74AS11D	AS11
				SN74AS11DR	
SOP – NS	Tape and reel	SN74ALS11ANSR	ALS11A		
		SN74AS11NSR	74AS11		
–55°C to 125°C	CDIP – J	Tube	SNJ54ALS11AJ	SNJ54ALS11AJ	
			SNJ54AS11J	SNJ54AS11J	
	CFP – W	Tube	SNJ54ALS11AW	SNJ54ALS11AW	
	LCCC – FK	Tube	SNJ54ALS11AFK	SNJ54ALS11AFK	
SNJ54AS11FK			SNJ54AS11FK		

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2002, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54ALS11A, SN54AS11, SN74ALS11A, SN74AS11

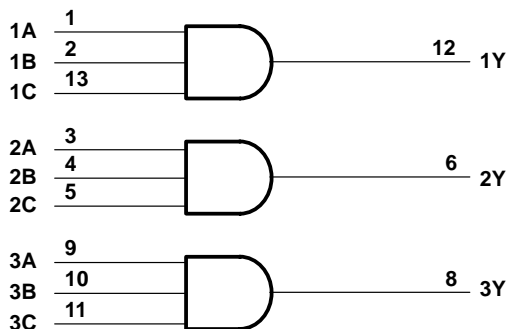
## TRIPLE 3-INPUT POSITIVE-AND GATES

SDAS009D – MARCH 1984 – REVISED NOVEMBER 2002

FUNCTION TABLE  
(each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

### logic diagram, each gate (positive logic)



Pin numbers shown are for the D, J, N, NS, and W packages.

### absolute maximum ratings over operating free-air temperature range (SN54ALS11A, SN74ALS11A) (unless otherwise noted)†

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Package thermal impedance, $\theta_{JA}$ (see Note 1): D package	86°C/W
N package	80°C/W
NS package	76°C/W
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 2)

	SN54ALS11A			SN74ALS11A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.8‡			0.8	V
			0.7§				
$I_{OH}$ High-level output current			-0.4			-0.4	mA
$I_{OL}$ Low-level output current			4			8	mA
$T_A$ Operating free-air temperature	-55		125	0		70	°C

‡ Applies over temperature range -55°C to 70°C

§ Applies over temperature range 70°C to 125°C

NOTE 2: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN54ALS11A, SN54AS11, SN74ALS11A, SN74AS11 TRIPLE 3-INPUT POSITIVE-AND GATES

SDAS009D – MARCH 1984 – REVISED NOVEMBER 2002

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54ALS11A		SN74ALS11A		UNIT		
		MIN	TYP†	MAX	MIN		TYP†	MAX
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.5		-1.5	V	
$V_{OH}$	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OH} = -0.4\text{ mA}$			$V_{CC} - 2$		$V_{CC} - 2$	V	
$V_{OL}$	$V_{CC} = 4.5\text{ V}$			0.25	0.4	0.25	0.4	V
						0.35	0.5	
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$				0.1		0.1	mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$				20		20	$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$				-0.1		-0.1	mA
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$	-20		-112		-30		mA
$I_{CCH}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 4.5\text{ V}$		1	1.8		1	1.8	mA
$I_{CCL}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 0$		1.6	3		1.6	3	mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V TO }5.5\text{ V}$ , $C_L = 50\text{ PF}$ , $R_L = 500\ \Omega$ , $T_A = \text{MIN TO MAX}\S$				UNIT
			SN54ALS11A		SN74ALS11A		
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A, B, or C	Y	2	14	2	13	ns
$t_{PHL}$			2	12.5	2	10	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**absolute maximum ratings over operating free-air temperature range (SN54AS11, SN74AS11) (unless otherwise noted)¶**

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Package thermal impedance, $\theta_{JA}$ (see Note 1): D package	86°C/W
N package	80°C/W
NS package	76°C/W
Storage temperature range	-65°C to 150°C

¶ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.



# SN54ALS11A, SN54AS11, SN74ALS11A, SN74AS11 TRIPLE 3-INPUT POSITIVE-AND GATES

SDAS009D – MARCH 1984 – REVISED NOVEMBER 2002

## recommended operating conditions (see Note 2)

		SN54AS11			SN74AS11			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V		
V <sub>IH</sub>	High-level input voltage	2			2			V		
V <sub>IL</sub>	Low-level input voltage	0.8			0.8			V		
I <sub>OH</sub>	High-level output current	-2			-2			mA		
I <sub>OL</sub>	Low-level output current	20			20			mA		
T <sub>A</sub>	Operating free-air temperature	-55			125			0	70	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS11			SN74AS11			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA	-1.2			-1.2			V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -2 mA	V <sub>CC</sub> -2			V <sub>CC</sub> -2			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 20 mA	0.35 0.5			0.35 0.5			V
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V	0.1			0.1			mA
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V	20			20			μA
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V	-0.5			-0.5			mA
I <sub>O</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V	-30 -112			-30 -112			mA
I <sub>CCH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 4.5 V	4.3 7			4.3 7			mA
I <sub>CCL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0	11.2 18			11.2 18			mA

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I<sub>OS</sub>.

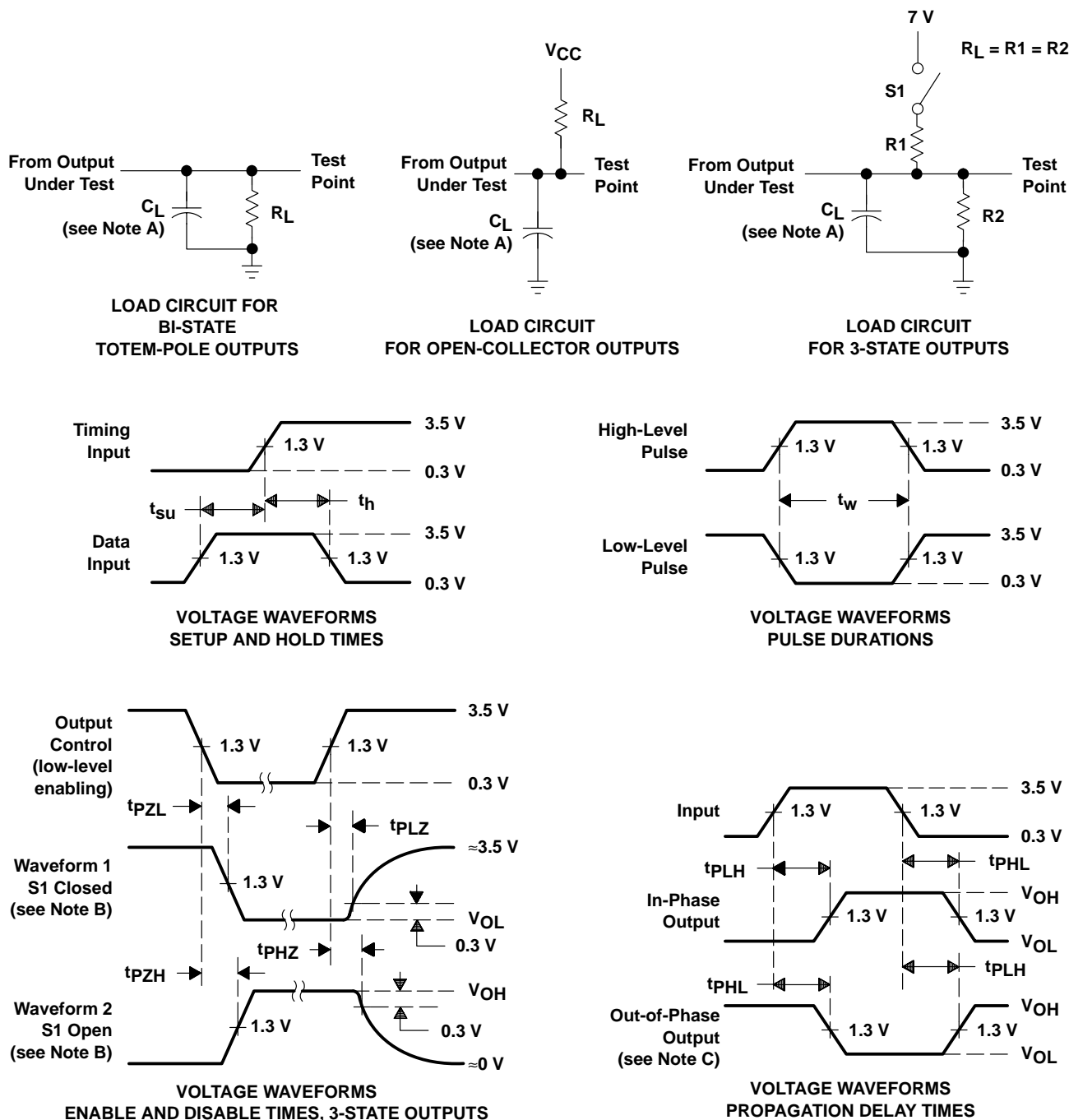
## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V TO 5.5 V, C <sub>L</sub> = 50 PF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN TO MAX§				UNIT
			SN54AS11		SN74AS11		
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A, B, or C	Y	1	6.5	1	6	ns
t <sub>PHL</sub>			1	6.5	1	5.5	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



PARAMETER MEASUREMENT INFORMATION  
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-86841012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8684101CA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8684101DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
5962-9756101Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9756101QCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/37402B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/37402BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN54ALS11AJ	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN54AS11J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN74ALS11AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS11ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS11ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS11ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS11AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS11ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS11ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS11ANSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS11D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS11DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS11DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS11DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS11N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS11NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS11NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS11NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ALS11AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54ALS11AJ	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54ALS11AW	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ54AS11FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54AS11J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type

---

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AB.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Low Power Wireless	<a href="http://www.ti.com/lpw">www.ti.com/lpw</a>	Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265