

# SN54ACT245, SN74ACT245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCAS452D – SEPTEMBER 1994 – REVISED JANUARY 2000

- Inputs Are TTL-Voltage Compatible
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- Package Options Include Plastic Small-Outline (DW) Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic (N) and Ceramic (J) DIPs

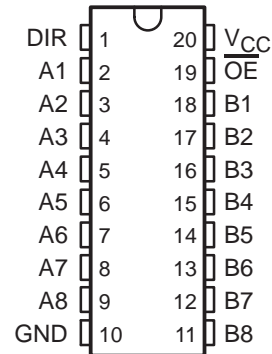
## description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

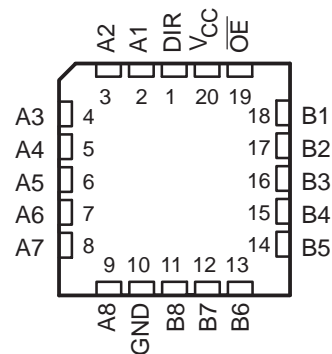
When the output-enable ( $\overline{OE}$ ) is low, the device passes noninverted data from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. A high on  $\overline{OE}$  disables the device so that the buses are effectively isolated.

The SN54ACT245 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ACT245 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54ACT245 . . . J OR W PACKAGE  
SN74ACT245 . . . DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



SN54ACT245 . . . FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each transceiver)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



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 **TEXAS  
INSTRUMENTS**

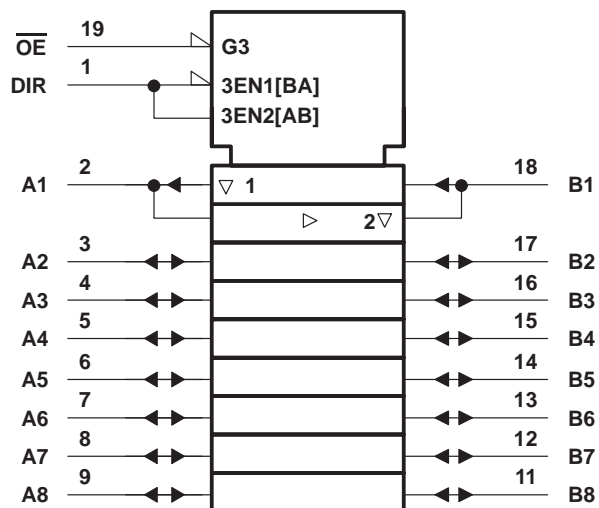
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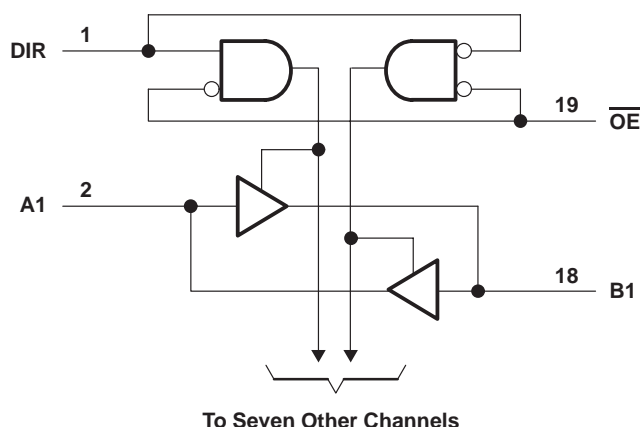
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 200$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
DB package .....	70°C/W
DW package .....	58°C/W
N package .....	69°C/W
PW package .....	83°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51.

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## recommended operating conditions (see Note 3)

		SN54ACT245		SN74ACT245		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-24		-24	mA
I <sub>OL</sub>	Low-level output current		24		24	mA
Δt/Δv	Input transition rise or fall rate	0	8	0	8	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54ACT245		SN74ACT245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.49	4.4		4.4		V	
		5.5 V	5.4	5.49	5.4		5.4			
	I <sub>OH</sub> = -24 mA	4.5 V	3.88		3.7		3.76			
		5.5 V	4.86		4.7		4.76			
	I <sub>OH</sub> = -50 mA†	5.5 V			3.85					
I <sub>OH</sub> = -75 mA†	5.5 V					3.85				
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V		0.001	0.1		0.1	0.1	V	
		5.5 V		0.001	0.1		0.1	0.1		
	I <sub>OL</sub> = 24 mA	4.5 V			0.36		0.5	0.44		
		5.5 V			0.36		0.5	0.44		
	I <sub>OL</sub> = 50 mA†	5.5 V				1.65				
I <sub>OL</sub> = 75 mA†	5.5 V					1.65				
I <sub>OZ</sub>	A or B ports‡	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.5		±10	±5	μA
I <sub>I</sub>	OE or DIR	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1	±1	μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		80	40	μA
ΔI <sub>CC</sub> §		One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V		0.6			1.6	1.5	mA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4.5					pF
C <sub>io</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		15					pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

‡ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

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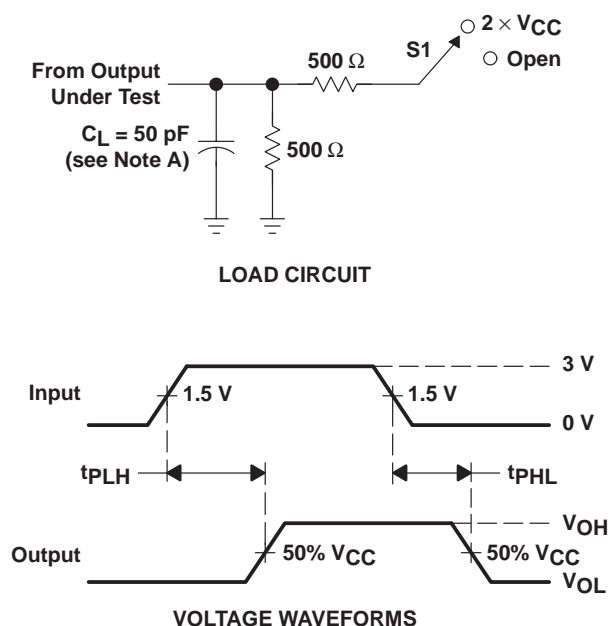
switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54ACT245		SN74ACT245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	1	4	7.5	1	9	1.5	8	ns
$t_{PHL}$			1	4	8	1	10	1	9	
$t_{PZH}$	$\overline{OE}$	A or B	1	5	10	1	12	1.5	11	ns
$t_{PZL}$			1	5.5	10	1	13	1.5	12	
$t_{PHZ}$	$\overline{OE}$	A or B	1	5.5	10	1	12	1	11	ns
$t_{PLZ}$			1	5	10	1	12	1.5	11	

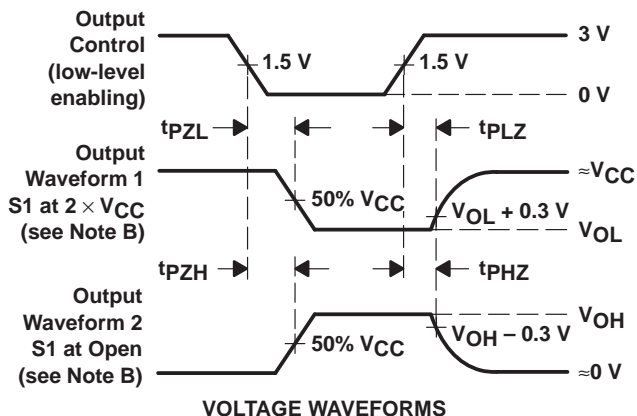
operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	45	pF

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	2 × V <sub>CC</sub>
$t_{PHZ}/t_{PZH}$	Open



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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