

SN54ABT245A, SN74ABT245B OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS0811 – JANUARY 1991 – REVISED AUGUST 2001

- Typical V_{OLP} (Output Ground Bounce) <1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

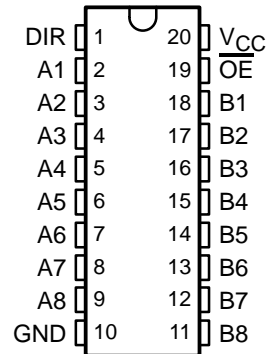
description

These octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

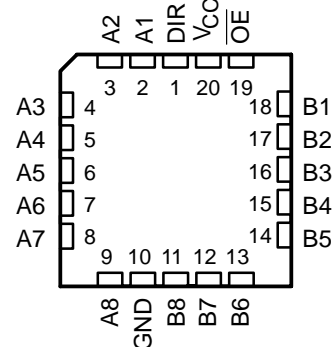
When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

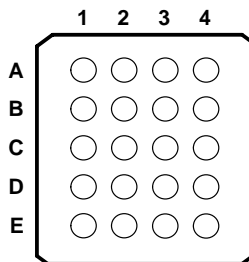
SN54ABT245A . . . J OR W PACKAGE
SN74ABT245B . . . DB, DGV, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ABT245B . . . FK PACKAGE
(TOP VIEW)



GQN PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4
A	A1	DIR	V_{CC}	\overline{OE}
B	A3	B2	A2	B1
C	A5	A4	B4	B3
D	A7	B6	A6	B5
E	GND	A8	B8	B7



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 **TEXAS
INSTRUMENTS**

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ORDERING INFORMATION

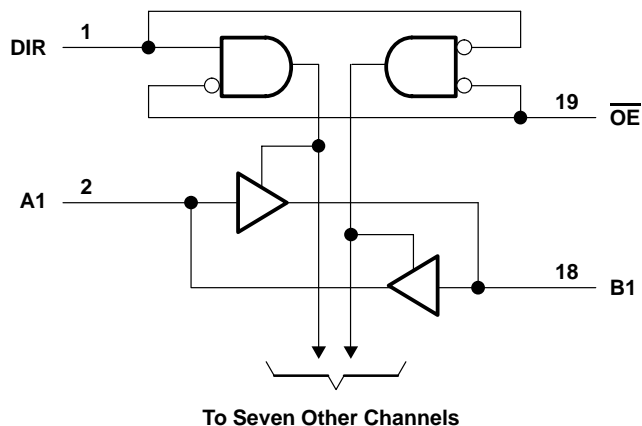
T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74ABT245BN	SN74ABT245BN
	SOIC – DW	Tube	SN74ABT245BDW	ABT245B
		Tape and reel	SN74ABT245BDWR	
	SSOP – DB	Tape and reel	SN74ABT245BDBR	AB245B
	TSSOP – PW	Tape and reel	SN74ABT245BPWR	AB245B
	TVSOP – DGV	Tape and reel	SN74ABT245BDGVR	AB245B
VFBGA – GQN	Tape and reel	SN74ABT245BGQNR	AB245B	
-55°C to 125°C	CDIP – J	Tube	SNJ54ABT245AJ	SNJ54ABT245AJ
	CFP - W	Tube	SNJ54ABT245AW	SNJ54ABT245AW
	LCCC - FK	Tube	SNJ54ABT245AFK	SNJ54ABT245AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, FK, J, N, PW, and W packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT245A	96 mA
SN74ABT245B	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	70°C/W
DGV package	92°C/W
DW package	58°C/W
GQN package	76°C/W
N package	69°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	SN54ABT245A		SN74ABT245B		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH} High-level output current		–24		–32	mA
I_{OL} Low-level output current		48		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		5		5	ns/V
$\Delta t/\Delta V_{CC}$ Power-up ramp rate				200	μ s/V
T_A Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT245A		SN74ABT245B		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V	
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA		2.5		2.5		2.5		V	
	V _{CC} = 5 V, I _{OH} = -3 mA		3		3		3			
	V _{CC} = 4.5 V, I _{OH} = -24 mA		2		2					
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 48 mA			0.55		0.55			V	
		I _{OL} = 64 mA		0.55*			0.55			
V _{hys}			100						mV	
I _I	Control inputs	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND		±1		±1		±1	μA	
	A or B ports	V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND		±20		±100		±20		
I _{OZPU}	V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	μA	
I _{OZPD}	V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	μA	
I _{OZH} ‡	V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, $\overline{OE} \geq 2$ V			10		10		10	μA	
I _{OZL} ‡	V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, $\overline{OE} \geq 2$ V			-10		-10		-10	μA	
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA	
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high		50		50		50	μA	
I _O §	V _{CC} = 5.5 V, V _O = 2.5 V	-50	-140	-180	-50	-180	-50	-180	mA	
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		5	250	250	250	μA	
			Outputs low		22	30	30	30	mA	
			Outputs disabled		1	250	250	250	μA	
ΔI _{CC} ¶	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Outputs enabled		1.5		1.5		1.5	mA
			Outputs disabled		50		50		50	μA
	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		1.5		1.5		1.5	mA	
C _i	Control inputs	V _I = 2.5 V or 0.5 V		4					pF	
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V		8					pF	

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



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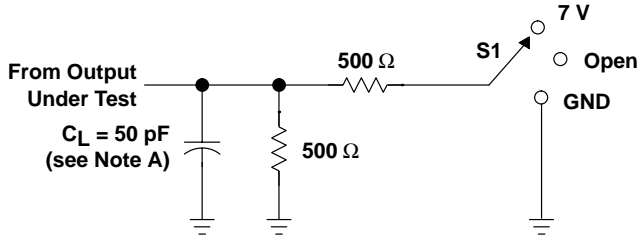
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54ABT245A		SN74ABT245B		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	2	3.2	0.8	3.8	1	3.6	ns
t_{PHL}			1	2.6	3.5	1	4.2	1	3.9	
t_{PZH}	\overline{OE}	A or B	2	3.5	4.5	1.2	6.2	2	5.6	ns
t_{PZL}			1.9	4	5.3	1.3	6.8	1.9	6.2	
t_{PHZ}	\overline{OE}	A or B	2.2	4.4	5.4	2.2	6.1	2.2	5.9	ns
t_{PLZ}			1.5	3	4	1.0	4.9	1.5	4.5	
$t_{sk(o)}$					0.5			0.5	ns	

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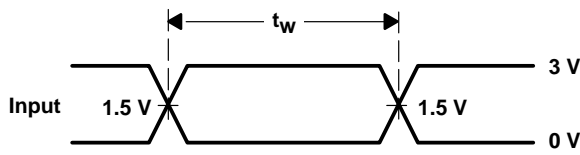
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PARAMETER MEASUREMENT INFORMATION

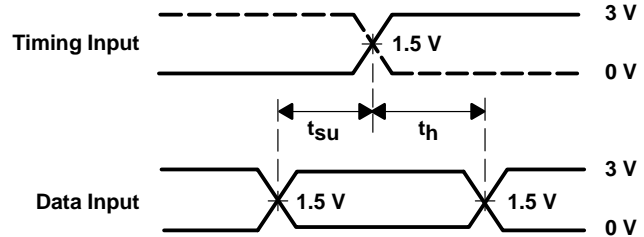


LOAD CIRCUIT

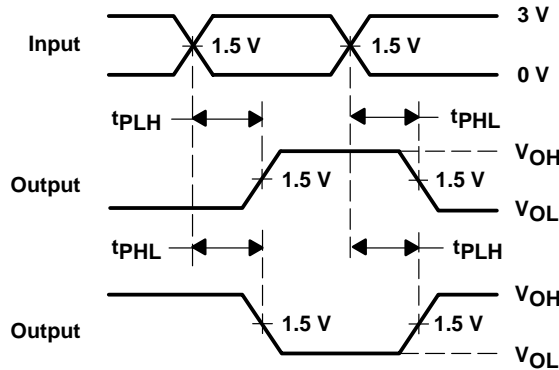
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



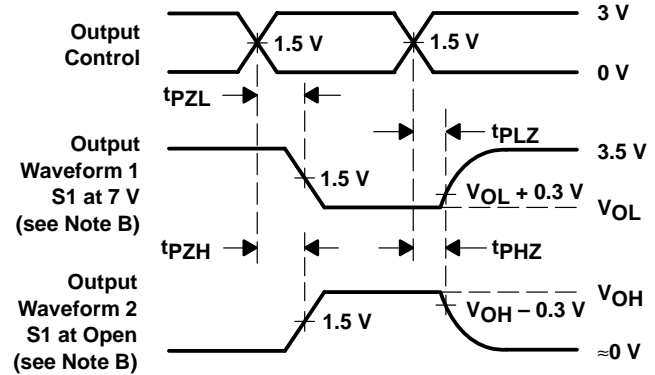
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265