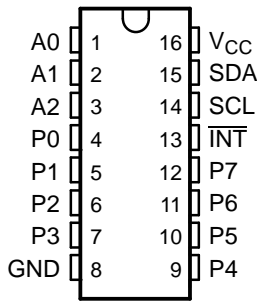


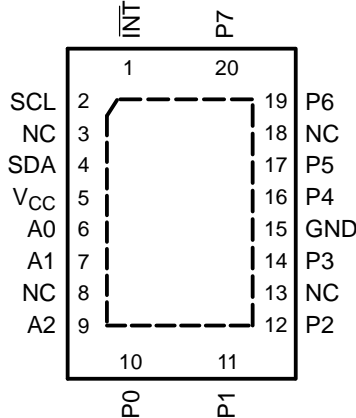
**FEATURES**

- Low Standby-Current Consumption of 10  $\mu$ A Maximum
- I<sup>2</sup>C to Parallel-Port Expander
- Open-Drain Interrupt Output
- Compatible With Most Microcontrollers
- Latched Outputs With High-Current Drive Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

**DW OR N PACKAGE (TOP VIEW)**

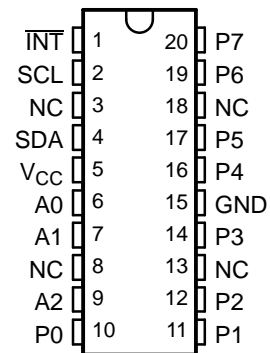


**RGY PACKAGE (TOP VIEW)**



NC – No internal connection

**DGV OR PW PACKAGE (TOP VIEW)**



NC – No internal connection

**DESCRIPTION/ORDERING INFORMATION**

This 8-bit input/output (I/O) expander for the two-line bidirectional bus (I<sup>2</sup>C) is designed for 2.5-V to 6-V V<sub>CC</sub> operation.

The PCF8574 provides general-purpose remote I/O expansion for most microcontroller families via the I<sup>2</sup>C interface [serial clock (SCL), serial data (SDA)].

The device features an 8-bit quasi-bidirectional I/O port (P0–P7), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are high. In this mode, only a current source to V<sub>CC</sub> is active. An additional strong pullup to V<sub>CC</sub> allows fast rising edges into heavily loaded outputs. This device turns on when an output is written high and is switched off by the negative edge of SCL. The I/Os should be high before being used as inputs.

**ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	PCF8574RGYR	PF574
	PDIP – N	Tube	PCF8574N	PCF8574N
	SOIC – DW	Tube	PCF8574DW	PCF8574
		Tape and reel	PCF8574DWR	
	TSSOP – PW	Tape and reel	PCF8574PWR	PF574
	TVSOP – DGV	Tape and reel	PCF8574DGV	PF574

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



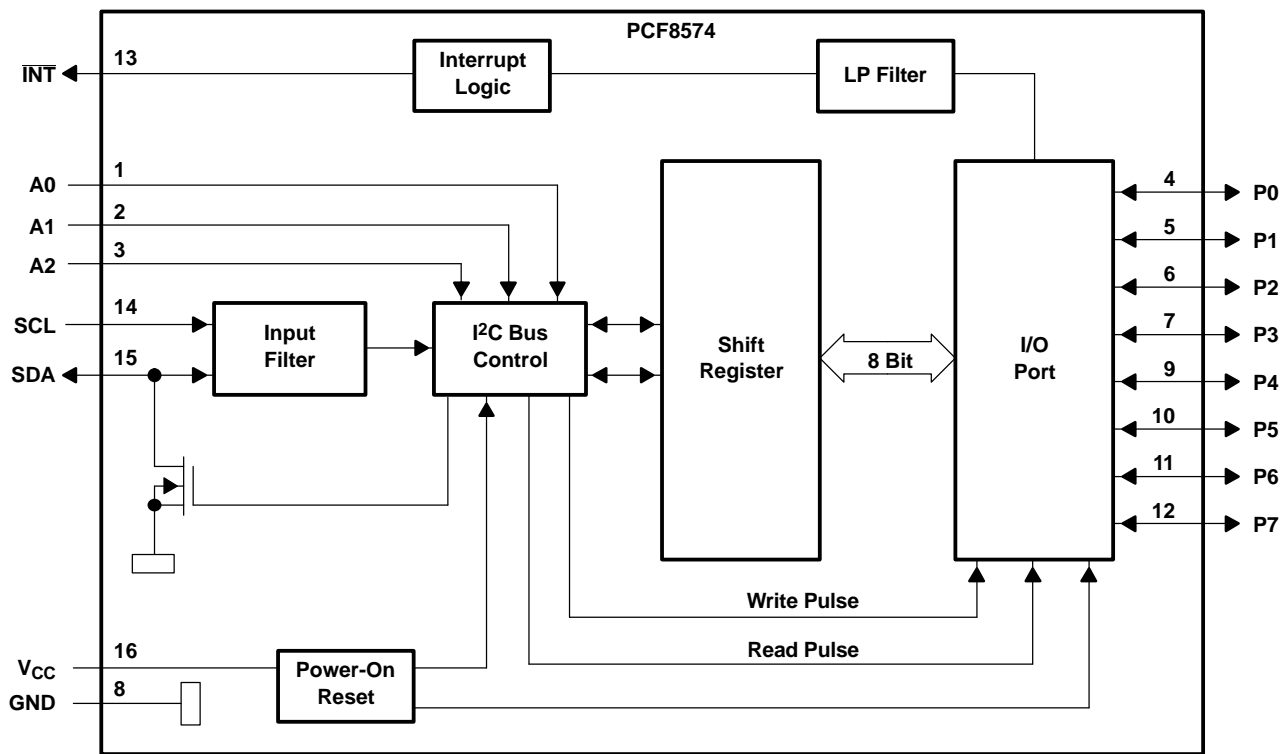
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

The PCF8574 provides an open-drain output ( $\overline{\text{INT}}$ ) that can be connected to the interrupt input of a microcontroller. An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time  $t_{iv}$ ,  $\overline{\text{INT}}$  is valid. Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from, or written to, the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge bit after the rising edge of the SCL signal or in the write mode at the acknowledge bit after the high-to-low transition of the rising edge of the SCL signal. Interrupts that occur during the acknowledge clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and, after the next rising clock edge, is transmitted as  $\overline{\text{INT}}$ . Reading from, or writing to, another device does not affect the interrupt circuit.

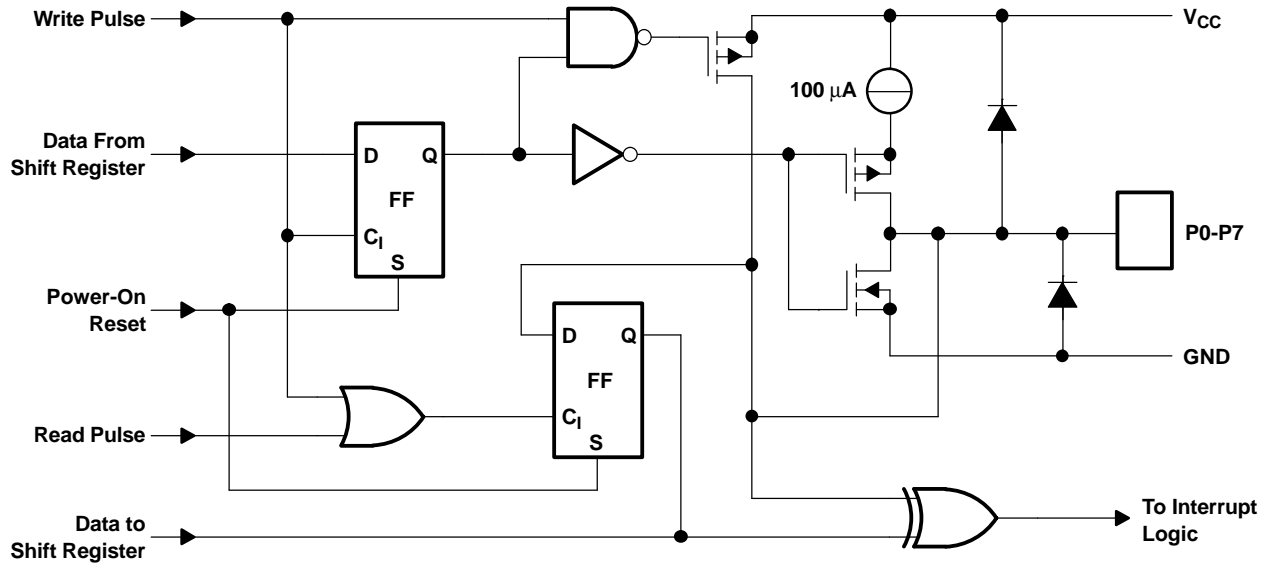
By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I<sup>2</sup>C bus. Therefore, the PCF8574 can remain a simple slave device.

**LOGIC DIAGRAM (POSITIVE LOGIC)**



Pin numbers shown are for the DW and N packages.

**SIMPLIFIED SCHEMATIC DIAGRAM OF EACH P-PORT INPUT/OUTPUT**



**I<sup>2</sup>C INTERFACE**

I<sup>2</sup>C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the SDA I/O while the SCL input is high. After the start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit ( $\overline{R/\overline{W}}$ ). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an acknowledge, a low on the SDA I/O during the high of the acknowledge-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the start and the stop conditions.

The data byte follows the address acknowledge. If the  $\overline{R/\overline{W}}$  bit is high, the data from this device are the values read from the P port. If the  $\overline{R/\overline{W}}$  bit is low, the data are from the master, to be output to the P port. The data byte is followed by an acknowledge sent from this device. If other data bytes are sent from the master, following the acknowledge, they are ignored by this device. Data are output only if complete bytes are received and acknowledged. The output data will be valid at time  $t_{pv}$  after the low-to-high transition of SCL and during the clock cycle for the acknowledge.

A stop condition, which is a low-to-high transition on the SDA I/O while the SCL input is high, is sent by the master.

**INTERFACE DEFINITION**

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I <sup>2</sup> C slave address	L	H	L	L	A2	A1	A0	$\overline{R/\overline{W}}$
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

ADDRESS REFERENCE

INPUTS			I <sup>2</sup> C-BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	32 (decimal), 20 (hexadecimal)
L	L	H	33 (decimal), 21 (hexadecimal)
L	H	L	34 (decimal), 22 (hexadecimal)
L	H	H	35 (decimal), 23 (hexadecimal)
H	L	L	36 (decimal), 24 (hexadecimal)
H	L	H	37 (decimal), 25 (hexadecimal)
H	H	L	38 (decimal), 26 (hexadecimal)
H	H	H	39 (decimal), 27 (hexadecimal)

**Absolute Maximum Ratings**<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-20 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-20 mA
I <sub>OK</sub>	Input/output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>		±400 μA
I <sub>OL</sub>	Continuous output low current	V <sub>O</sub> = 0 to V <sub>CC</sub>		50 mA
I <sub>OH</sub>	Continuous output high current	V <sub>O</sub> = 0 to V <sub>CC</sub>		-4 mA
	Continuous current through V <sub>CC</sub> or GND			±100 mA
θ <sub>JA</sub>	Package thermal impedance	DGV package <sup>(3)</sup>		92
		DW package <sup>(3)</sup>		57
		N package <sup>(3)</sup>		67
		PW package <sup>(3)</sup>		83
		RGY package <sup>(4)</sup>		37
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) The package thermal impedance is calculated in accordance with JESD 51-5.

**Recommended Operating Conditions**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.5	6	V
V <sub>IH</sub>	High-level input voltage	0.7 × V <sub>CC</sub>	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Low-level input voltage	-0.5	0.3 × V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current			-1 mA
I <sub>OL</sub>	Low-level output current			25 mA
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IK</sub>	Input diode clamp voltage	I <sub>I</sub> = -18 mA	2.5 V to 6 V	-1.2			V
V <sub>POR</sub>	Power-on reset voltage <sup>(2)</sup>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	6 V		1.3	2.4	V
I <sub>OH</sub>	P port	V <sub>O</sub> = GND	2.5 V to 6 V	30		300	μA
I <sub>OHT</sub>	P-port transient pullup current	High during acknowledge V <sub>OH</sub> = GND	2.5 V		-1		mA
I <sub>OL</sub>	SDA	V <sub>O</sub> = 0.4 V	2.5 V to 6 V	3			mA
	P port	V <sub>O</sub> = 1 V	5 V	10	25		
	INT	V <sub>O</sub> = 0.4 V	2.5 V to 6 V	1.6			
I <sub>I</sub>	SCL, SDA	V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V to 6 V			±5	μA
	INT					±5	
	A0, A1, A2					±5	
I <sub>IHL</sub>	P port	V <sub>I</sub> ≥ V <sub>CC</sub> or V <sub>I</sub> ≤ GND	2.5 V to 6 V			±400	μA
I <sub>CC</sub>	Operating mode	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, f <sub>SCL</sub> = 100 kHz	6 V		40	100	μA
	Standby mode	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0			2.5	10	
C <sub>i</sub>	SCL	V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V to 6 V		1.5	7	pF
C <sub>io</sub>	SDA	V <sub>IO</sub> = V <sub>CC</sub> or GND	2.5 V to 6 V		3	7	pF
	P port				4	10	

(1) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

(2) The power-on reset circuit resets the I<sup>2</sup>C-bus logic with V<sub>CC</sub> < V<sub>POR</sub> and sets all I/Os to logic high (with current source to V<sub>CC</sub>).

## I<sup>2</sup>C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		MIN	MAX	UNIT
f <sub>scl</sub>	I <sup>2</sup> C clock frequency		100	kHz
t <sub>sch</sub>	I <sup>2</sup> C clock high time	4		μs
t <sub>scl</sub>	I <sup>2</sup> C clock low time	4.7		μs
t <sub>sp</sub>	I <sup>2</sup> C spike time		100	ns
t <sub>sds</sub>	I <sup>2</sup> C serial data setup time	250		ns
t <sub>sdh</sub>	I <sup>2</sup> C serial data hold time	0	900	ns
t <sub>icr</sub>	I <sup>2</sup> C input rise time		1	μs
t <sub>icf</sub>	I <sup>2</sup> C input fall time		0.3	μs
t <sub>ocf</sub>	I <sup>2</sup> C output fall time (10-pF to 400-pF bus)		300	ns
t <sub>bud</sub>	I <sup>2</sup> C-bus free time between stop and start	4.7		μs
t <sub>sts</sub>	I <sup>2</sup> C start or repeated start condition setup	4.7		μs
t <sub>sth</sub>	I <sup>2</sup> C start or repeated start condition hold	4		μs
t <sub>sps</sub>	I <sup>2</sup> C stop-condition setup	4		μs
t <sub>vd</sub>	Valid data time	SCL low to SDA output valid		3.4 μs
C <sub>b</sub>	I <sup>2</sup> C bus capacitive load		400	pF

# PCF8574 REMOTE 8-BIT I/O EXPANDER FOR I2C BUS

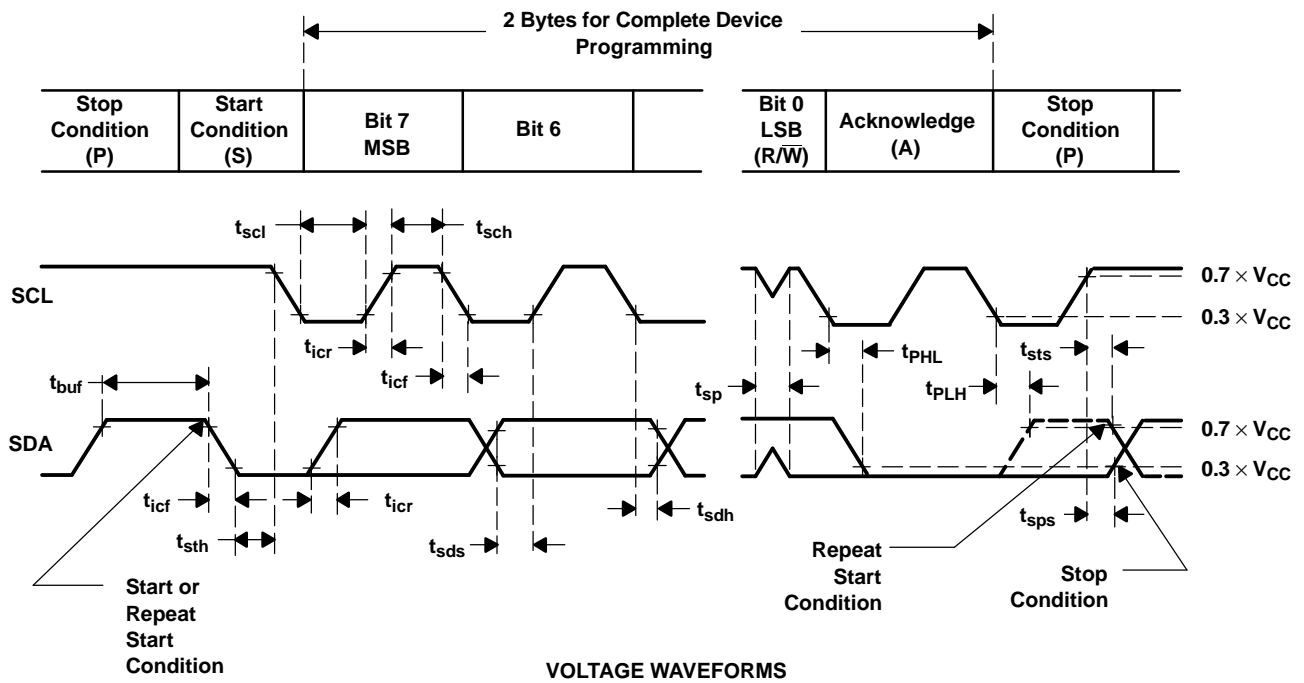
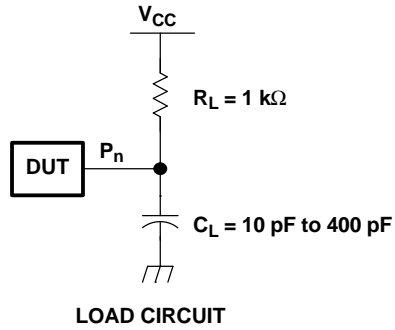
SCPS068D–JULY 2001–REVISED MARCH 2005

## Switching Characteristics

over recommended operating free-air temperature range,  $C_L \leq 100$  pF (unless otherwise noted) (see Figure 2)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{pv}$	Output data valid	SCL	P port		4	$\mu$ s
$t_{su}$	Input data setup time	P port	SCL	0		$\mu$ s
$t_h$	Input data hold time	P port	SCL	4		$\mu$ s
$t_{iv}$	Interrupt valid time	P port	$\overline{INT}$		4	$\mu$ s
$t_{ir}$	Interrupt reset delay time	SCL	$\overline{INT}$		4	$\mu$ s

PARAMETER MEASUREMENT INFORMATION



BYTE	DESCRIPTION
1	I <sup>2</sup> C address
2	P-port data

Figure 1. I<sup>2</sup>C Interface Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

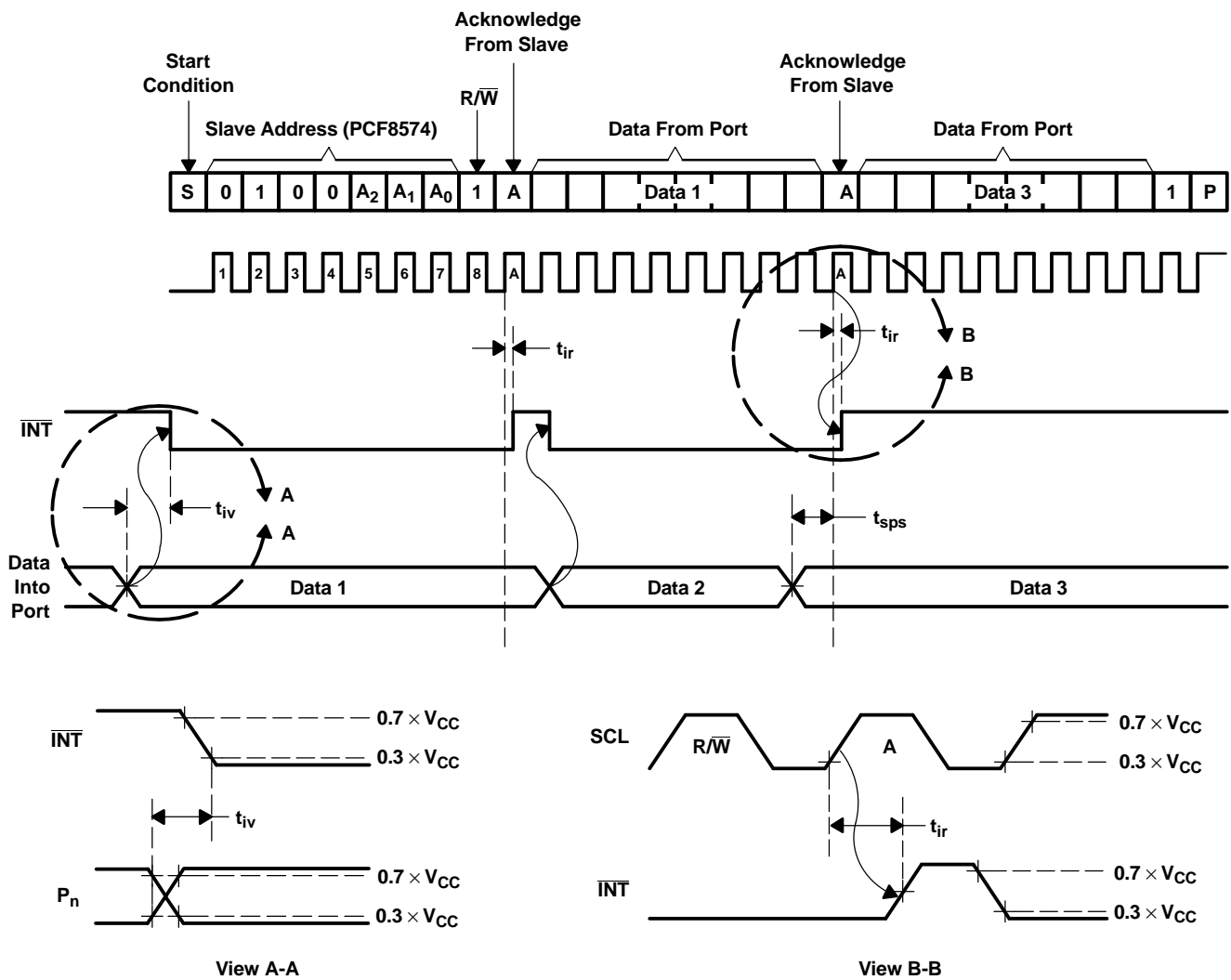


Figure 2. Interrupt-Timing Waveforms



PARAMETER MEASUREMENT INFORMATION

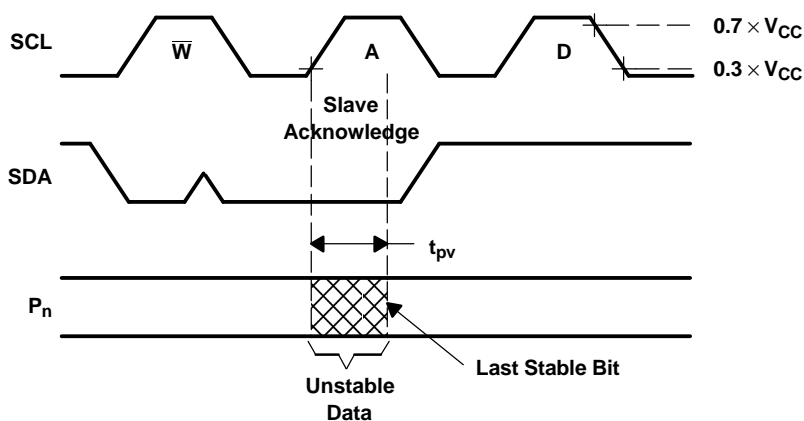


Figure 3. Write-Mode Timing

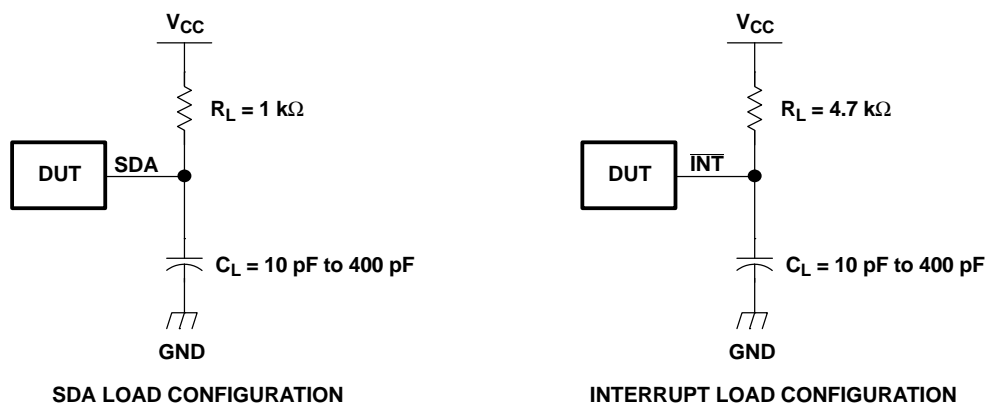


Figure 4. Load Circuits

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
PCF8574DGVR	ACTIVE	TVSOP	DGV	20		TBD	Call TI	Call TI
PCF8574DGVRE4	ACTIVE	TVSOP	DGV	20		TBD	Call TI	Call TI
PCF8574DW	ACTIVE	SOIC	DW	16		TBD	Call TI	Call TI
PCF8574DWE4	ACTIVE	SOIC	DW	16		TBD	Call TI	Call TI
PCF8574DWR	ACTIVE	SOIC	DW	16		TBD	Call TI	Call TI
PCF8574DWRE4	ACTIVE	SOIC	DW	16		TBD	Call TI	Call TI
PCF8574N	ACTIVE	PDIP	N	16		TBD	Call TI	Call TI
PCF8574NE4	ACTIVE	PDIP	N	16		TBD	Call TI	Call TI
PCF8574PW	ACTIVE	TSSOP	PW	20		TBD	Call TI	Call TI
PCF8574PWE4	ACTIVE	TSSOP	PW	20		TBD	Call TI	Call TI
PCF8574PWR	ACTIVE	TSSOP	PW	20		TBD	Call TI	Call TI
PCF8574PWRE4	ACTIVE	TSSOP	PW	20		TBD	Call TI	Call TI
PCF8574RGYR	ACTIVE	QFN	RGY	20		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

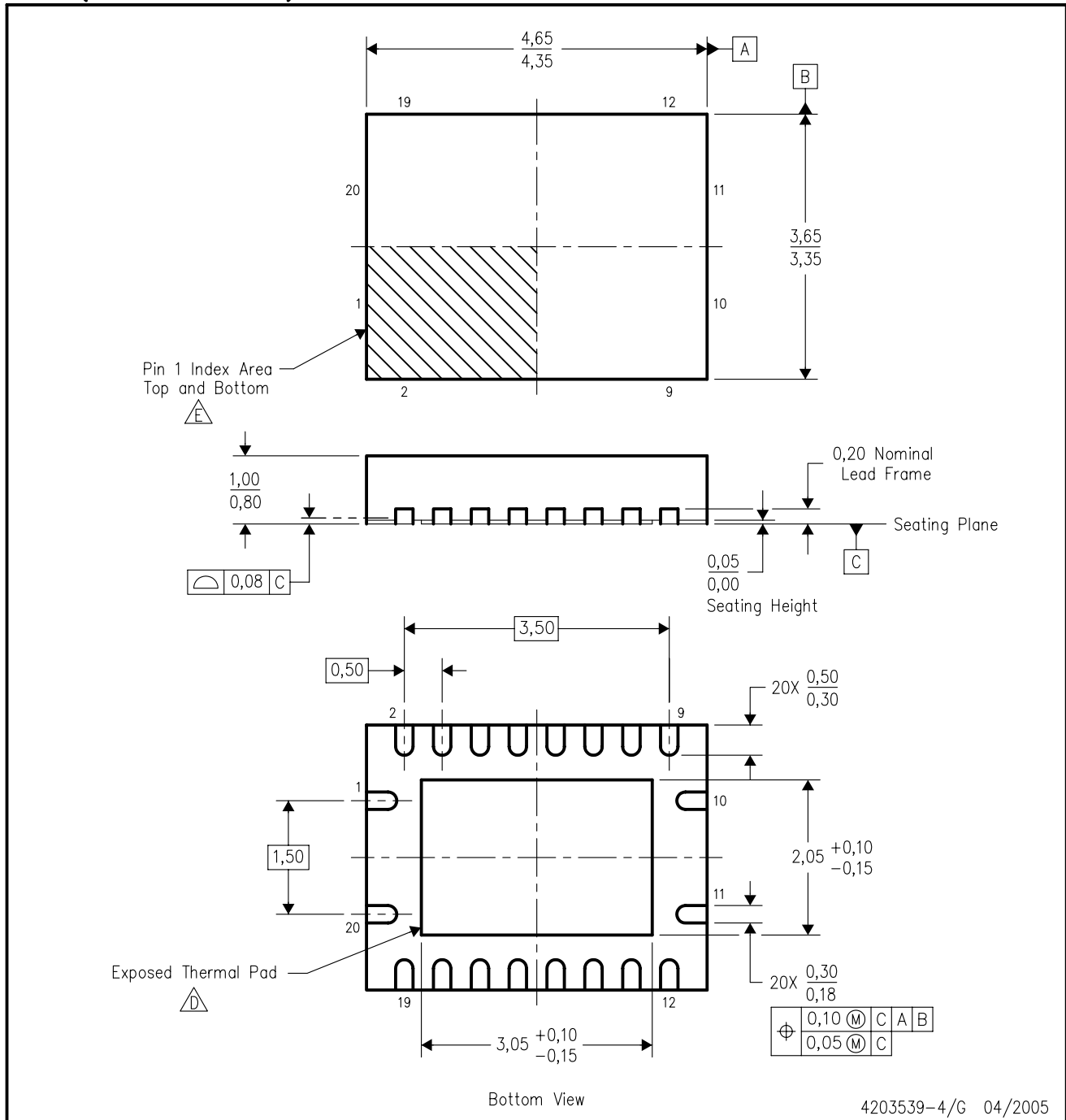
24 PINS SHOWN





- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

RGY (R-PQFP-N20)

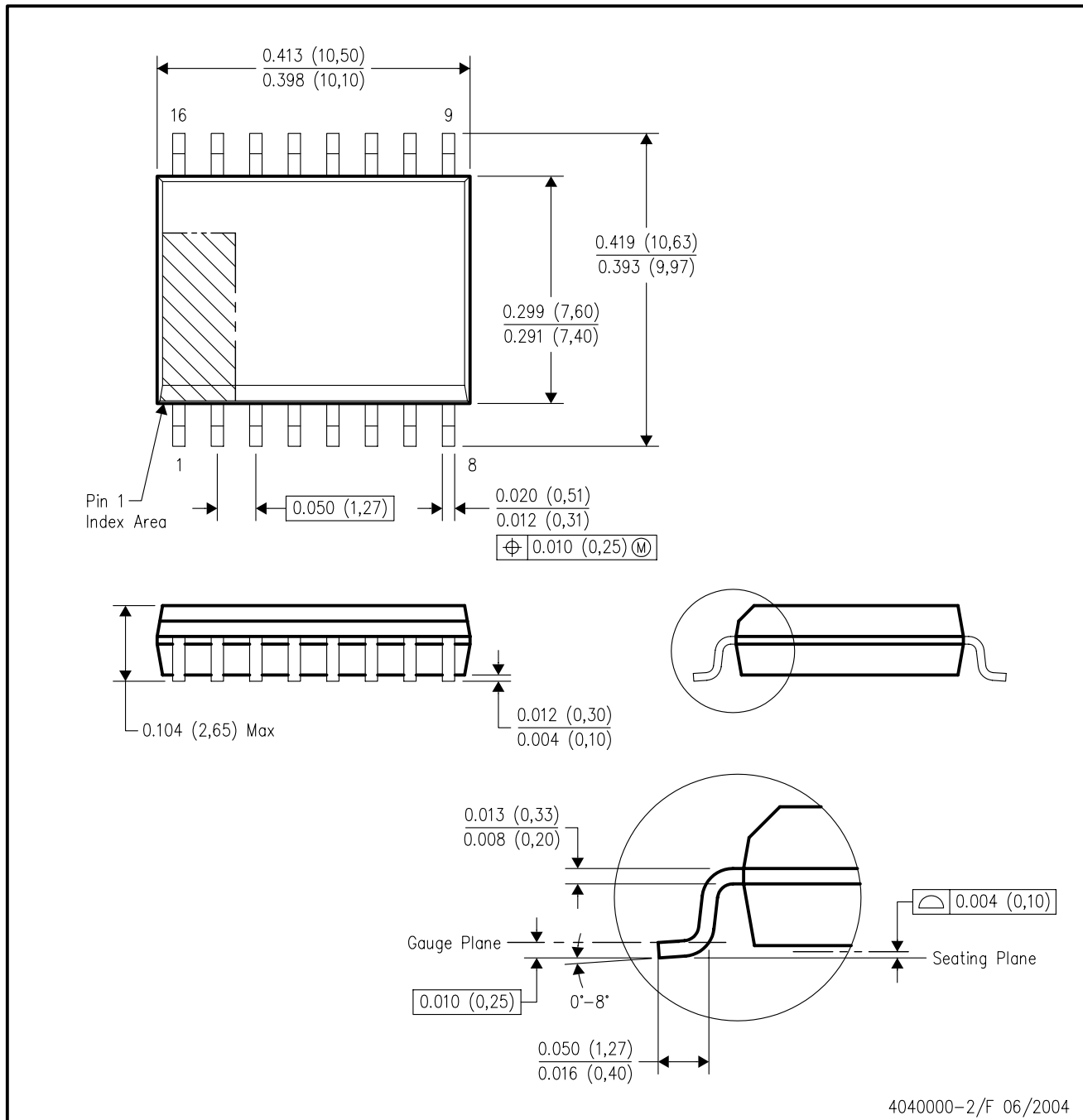
PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance.
  -  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - F. Package complies to JEDEC MO-241 variation BC.

DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AA.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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