- **Low Supply-Voltage Range, 1.8 V to 3.6 V**
- **Ultralow-Power Consumption:**
  - **Active Mode: 300 μA at 1 MHz, 2.2 V**
  - **Standby Mode: 1.1 μA**
  - **Off Mode (RAM Retention): 0.1 μA**
- **Five Power Saving Modes**
- **Wake-Up From Standby Mode in less than 6 μs**
- **16-Bit RISC Architecture, 125-ns Instruction Cycle Time**
- **Single-Channel Internal DMA**
- **12-Bit A/D Converter With Internal Reference, Sample-and-Hold and Autoscan Feature**
- **Three Configurable Operational Amplifiers**
- **Dual 12-Bit D/A Converters With Synchronization**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **16-Bit Timer_B With Three Capture/Compare-With-Shadow Registers**
- **On-Chip Comparator**
- **Serial Communication Interface (USART), Select Asynchronous UART or Synchronous SPI by Software**
- **Brownout Detector**
- **Supply Voltage Supervisor/Monitor With Programmable Level Detection**
- **Bootstrap Loader**
- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **Integrated LCD Driver for Up to 128 Segments**
- **Family Members Include:**
  - **MSP430FG437:**
    32KB+256B Flash Memory, 1KB RAM
  - **MSP430FG438:**
    48KB+256B Flash Memory, 2KB RAM
  - **MSP430FG439:**
    60KB+256B Flash Memory, 2KB RAM
- **For Complete Module Descriptions, See The *MSP430x4xx Family User's Guide*, Literature Number SLAU056**

description

The Texas Instruments MSP430 family of ultralow power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that attribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6μs.

The MSP430FG43x series are microcontroller configurations with two 16-bit timers, a high performance 12-bit A/D converter, dual 12-bit D/A converters, three configurable operational amplifiers, one universal synchronous/asynchronous communication interface (USART), DMA, 48 I/O pins, and a liquid crystal display (LCD) driver.

Typical applications for this device include analog and digital sensor systems, digital motor control, remote controls, thermostats, digital timers, hand-held meters, etc.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.

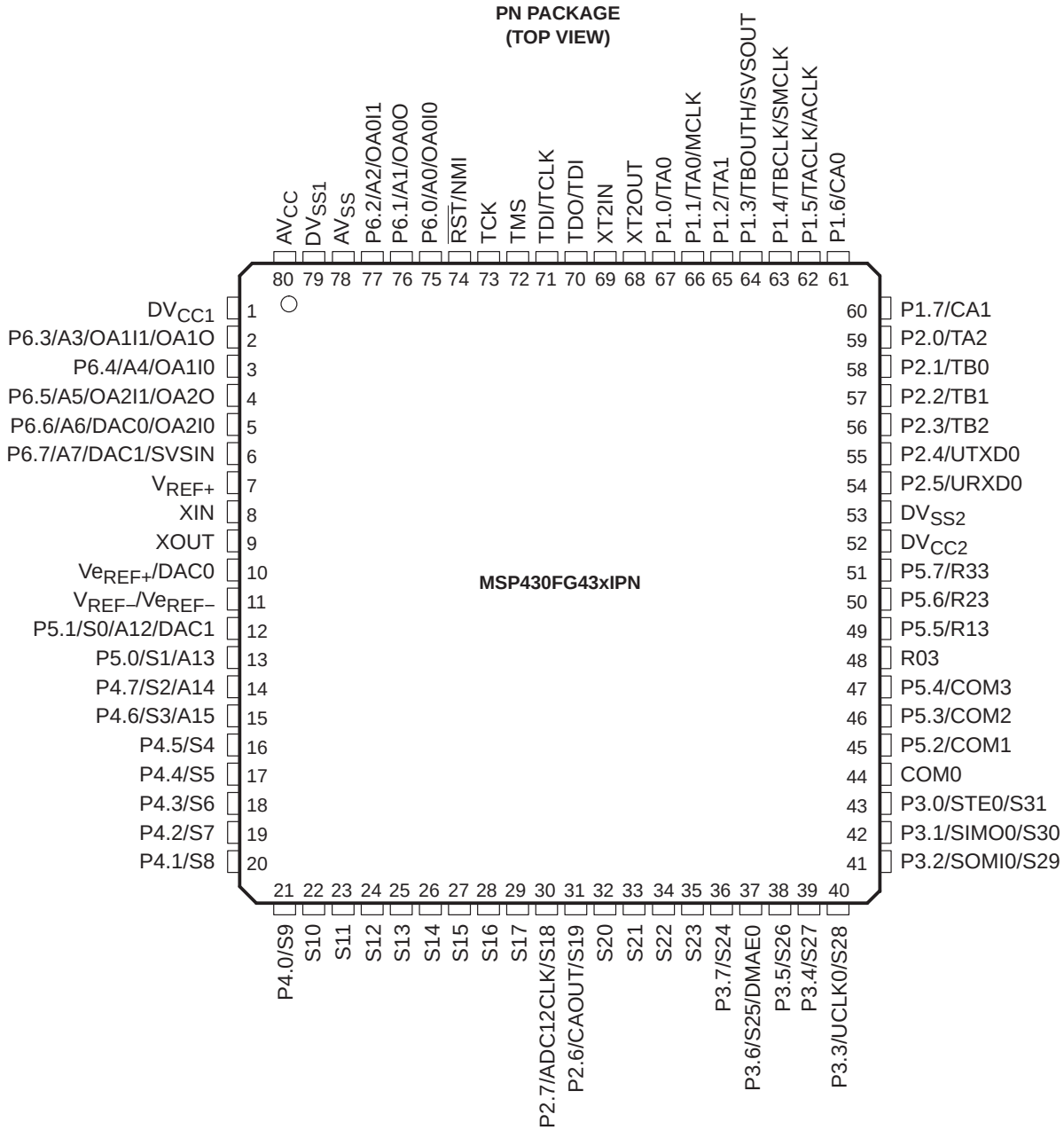
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

AVAILABLE OPTIONS

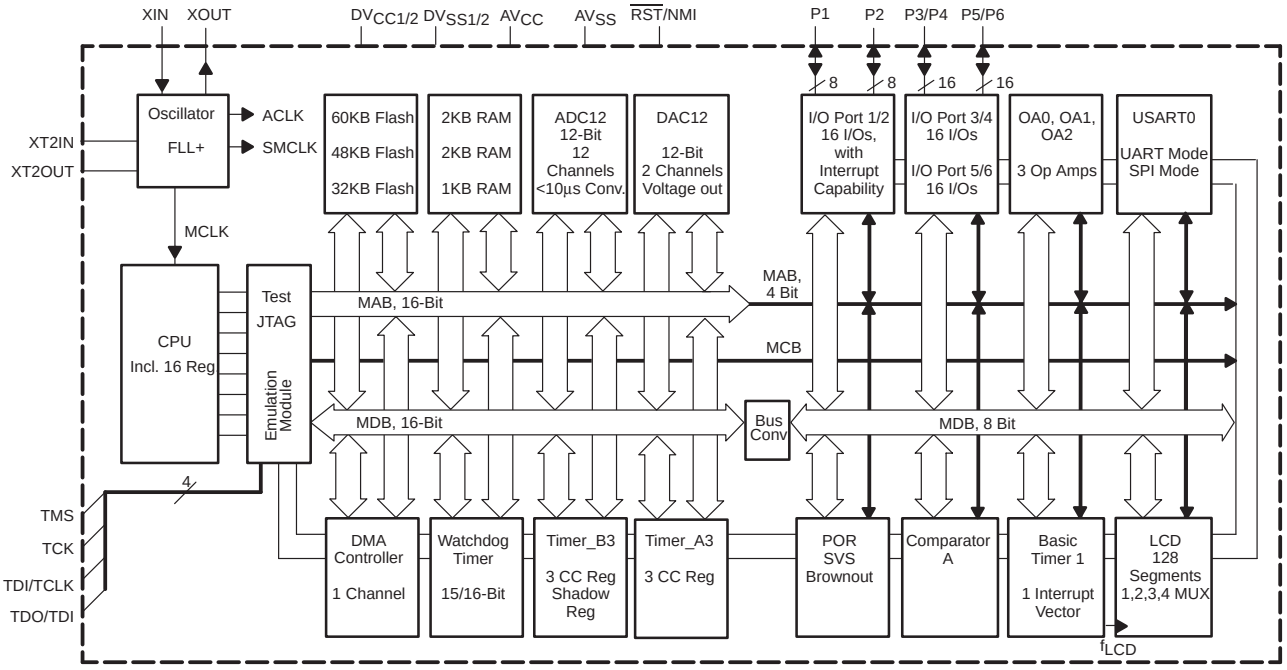
T_A	PACKAGED DEVICES
	PLASTIC 80-PIN QFP (PN)
−40°C to 85°C	MSP430FG437IPN MSP430FG438IPN MSP430FG439IPN

pin designation, MSP430FG437IPN, MSP430FG438IPN, MSP430FG439IPN

PN PACKAGE
(TOP VIEW)



MSP430FG43x functional block diagrams



MSP430FG43x Terminal Functions

TERMINAL		I/O	DESCRIPTION
PN NAME	NO.		
DV_{CC1}	1		Digital supply voltage, positive terminal.
P6.3/A3/OA1I1/OA1O	2	I/O	General-purpose digital I/O / analog input a3—12-bit ADC / OA1 output and/or input multiplexer on +terminal and −terminal
P6.4/A4/OA1I0	3	I/O	General-purpose digital I/O / analog input a4—12-bit ADC / OA1 input multiplexer on +terminal and −terminal
P6.5/A5/OA2I1/OA2O	4	I/O	General-purpose digital I/O / analog input a5—12-bit ADC / OA2 output and/or input multiplexer on +terminal and −terminal
P6.6/A6/DAC0/OA2I0	5	I/O	General-purpose digital I/O / analog input a6—12-bit ADC / DAC12.0 output / OA2 input multiplexer on +terminal and −terminal
P6.7/A7/DAC1/ SVSIN	6	I/O	General-purpose digital I/O / analog input a7—12-bit ADC / DAC12.1 output/analog input to supply voltage supervisor
V_{REF+}	7	O	Positive output terminal of the reference voltage in the ADC
XIN	8	I	Input terminal of crystal oscillator XT1
XOUT	9	O	Output terminal of crystal oscillator XT1
Ve_{REF+}/DAC0	10	I	Positive input terminal for an external reference voltage to the 12-bit ADC/DAC12.0 output
V_{REF-}/Ve_{REF-}	11	I	Negative terminal for the 12-bit ADC's reference voltage for both sources, the internal reference voltage or an external applied reference voltage to the 12-bit ADC.
P5.1/S0/A12/DAC1	12	I/O	General-purpose digital I/O / LCD segment output 0/ analog input a12—12-bit ADC/DAC12.1 output
P5.0/S1/A13	13	I/O	General-purpose digital I/O / LCD segment output 1/ analog input a13—12-bit ADC
P4.7/S2/A14	14	I/O	General-purpose digital I/O / LCD segment output 2/ analog input a14—12-bit ADC
P4.6/S3/A15	15	I/O	General-purpose digital I/O / LCD segment output 3/ analog input a15—12-bit ADC
P4.5/S4	16	I/O	General-purpose digital I/O / LCD segment output 4
P4.4/S5	17	I/O	General-purpose digital I/O / LCD segment output 5
P4.3/S6	18	I/O	General-purpose digital I/O / LCD segment output 6
P4.2/S7	19	I/O	General-purpose digital I/O / LCD segment output 7
P4.1/S8	20	I/O	General-purpose digital I/O / LCD segment output 8
P4.0/S9	21	I/O	General-purpose digital I/O / LCD segment output 9
S10	22	O	LCD segment output 10
S11	23	O	LCD segment output 11
S12	24	O	LCD segment output 12
S13	25	O	LCD segment output 13
S14	26	O	LCD segment output 14
S15	27	O	LCD segment output 15
S16	28	O	LCD segment output 16
S17	29	O	LCD segment output 17
P2.7/ADC12CLK/S18	30	I/O	General-purpose digital I/O / conversion clock—12-bit ADC / LCD segment output 18
P2.6/CAOUT/S19	31	I/O	General-purpose digital I/O / Comparator_A output / LCD segment output 19
S20	32	O	LCD segment output 20
S21	33	O	LCD segment output 21
S22	34	O	LCD segment output 22
S23	35	O	LCD segment output 23
P3.7/S24	36	I/O	General-purpose digital I/O / LCD segment output 24
P3.6/S25/DMAE0	37	I/O	General-purpose digital I/O / LCD segment output 25/DMA Channel 0 external trigger
P3.5/S26	38	I/O	General-purpose digital I/O / LCD segment output 26
P3.4/S27	39	I/O	General-purpose digital I/O / LCD segment output 27

MSP430FG43x Terminal Functions (Continued)

TERMINAL		I/O	DESCRIPTION
PN NAME	NO.		
P3.3/UCLK0/S28	40	I/O	General-purpose digital I/O / ext. clock i/p—USART0/UART or SPI mode, clock o/p—USART0/SPI mode / LCD segment output 28
P3.2/SOMI0/S29	41	I/O	General-purpose digital I/O / slave out/master in of USART0/SPI mode / LCD segment output 29
P3.1/SIMO0/S30	42	I/O	General-purpose digital I/O / slave out/master out of USART0/SPI mode / LCD segment output 30
P3.0/STE0/S31	43	I/O	General-purpose digital I/O / slave transmit enable-USART0/SPI mode / LCD segment output 31
COM0	44	O	Common output, COM0−3 are used for LCD backplanes.
P5.2/COM1	45	I/O	General-purpose digital I/O / common output, COM0−3 are used for LCD backplanes.
P5.3/COM2	46	I/O	General-purpose digital I/O / common output, COM0−3 are used for LCD backplanes.
P5.4/COM3	47	I/O	General-purpose digital I/O / common output, COM0−3 are used for LCD backplanes.
R03	48	I	Input port of fourth positive (lowest) analog LCD level (V5)
P5.5/R13	49	I/O	General-purpose digital I/O / input port of third most positive analog LCD level (V4 or V3)
P5.6/R23	50	I/O	General-purpose digital I/O / input port of second most positive analog LCD level (V2)
P5.7/R33	51	I/O	General-purpose digital I/O / output port of most positive analog LCD level (V1)
DV_{CC2}	52		Digital supply voltage, positive terminal.
DV_{SS2}	53		Digital supply voltage, negative terminal.
P2.5/URXD0	54	I/O	General-purpose digital I/O / receive data in—USART0/UART mode
P2.4/UTXD0	55	I/O	General-purpose digital I/O / transmit data out—USART0/UART mode
P2.3/TB2	56	I/O	General-purpose digital I/O / Timer_B3 CCR2. Capture: CCI2A/CCI2B input, compare: Out2 output
P2.2/TB1	57	I/O	General-purpose digital I/O / Timer_B3 CCR1. Capture: CCI1A/CCI1B input, compare: Out1 output
P2.1/TB0	58	I/O	General-purpose digital I/O / Timer_B3 CCR0. Capture: CCI0A/CCI0B input, compare: Out0 output
P2.0/TA2	59	I/O	General-purpose digital I/O / Timer_A Capture: CCI2A input, compare: Out2 output
P1.7/CA13	60	I/O	General-purpose digital I/O / Comparator_A input
P1.6/CA0	61	I/O	General-purpose digital I/O / Comparator_A input
P1.5/TACLK/ ACLK	62	I/O	General-purpose digital I/O / Timer_A, clock signal TACLK input / ACLK output (divided by 1, 2, 4, or 8)
P1.4/TBCLK/ SMCLK	63	I/O	General-purpose digital I/O / input clock TBCLK—Timer_B3 / submain system clock SMCLK output
P1.3/TBOUTH/ SVSOUT	64	I/O	General-purpose digital I/O / switch all PWM digital output ports to high impedance—Timer_B3 TB0 to TB2 / SVS: output of SVS comparator
P1.2/TA1	65	I/O	General-purpose digital I/O / Timer_A, Capture: CCI1A, compare: Out1 output
P1.1/TA0/MCLK	66	I/O	General-purpose digital I/O / Timer_A. Capture: CCI0B / MCLK output. Note: TA0 is only an input on this pin / BSL receive
P1.0/TA0	67	I/O	General-purpose digital I/O / Timer_A. Capture: CCI0A input, compare: Out0 output / BSL transmit
XT2OUT	68	O	Output terminal of crystal oscillator XT2
XT2IN	69	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
TDO/TDI	70	I/O	Test data output port. TDO/TDI data output or programming data input terminal
TDI/TCLK	71	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TMS	72	I	Test mode select. TMS is used as an input port for device programming and test.
TCK	73	I	Test clock. TCK is the clock input port for device programming and test.

MSP430FG43x Terminal Functions (Continued)

TERMINAL		I/O	DESCRIPTION
PN NAME	NO.		
$\overline{\text{RST}}$/NMI	74	I	Reset or nonmaskable interrupt input
P6.0/A0/OA0I0	75	I/O	General-purpose digital I/O / analog input a0 − 12-bit ADC / OA0 input multiplexer on +terminal and − terminal
P6.1/A1/OA0O	76	I/O	General-purpose digital I/O / analog input a1 − 12-bit ADC / OA0 output
P6.2/A2/OA0I1	77	I/O	General-purpose digital I/O / analog input a2 − 12-bit ADC / OA0 input multiplexer on + terminal and − terminal
AV_{SS}	78		Analog supply voltage, negative terminal. Supplies SVS, brownout, oscillator, FLL+, comparator_A, port 1, and LCD resistive divider circuitry.
DV_{SS1}	79		Digital supply voltage, negative terminal.
AV_{CC}	80		Analog supply voltage, positive terminal. Supplies SVS, brownout, oscillator, FLL+, comparator_A, port 1, and LCD resistive divider circuitry; must not power up prior to DV_{CC1}/DV_{CC2}.

short-form description

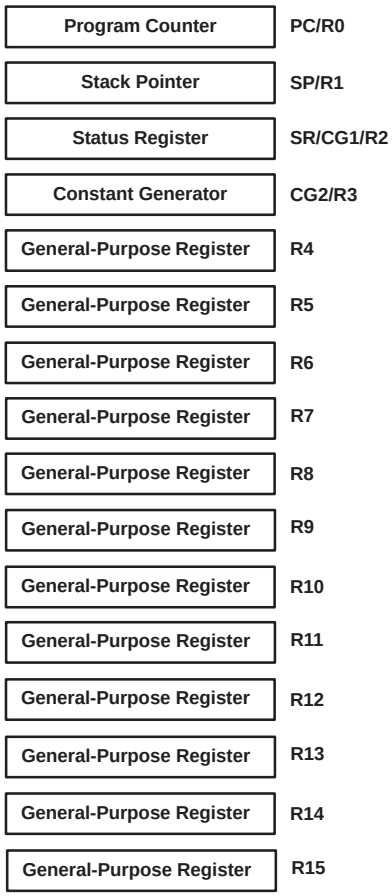
CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.



instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 −−−> R5
Single operands, destination only	e.g. CALL R8	PC −−>(TOS), R8−−> PC
Relative jump, un/conditional	e.g. JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 —> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)—> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) —> M(TONI)
Absolute	●	●	MOV &MEM, &TCDAT		M(MEM) —> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) —> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) —> R11 R10 + 2—> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 —> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode AM;
  - All clocks are active
- Low-power mode 0 (LPM0);
  - CPU is disabled
    ACLK and SMCLK remain active. MCLK is disabled
    FLL+ Loop control remains active
- Low-power mode 1 (LPM1);
  - CPU is disabled
    FLL+ Loop control is disabled
    ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 2 (LPM2);
  - CPU is disabled
    MCLK and FLL+ loop control and DCOCLK are disabled
    DCO's dc-generator remains enabled
    ACLK remains active
- Low-power mode 3 (LPM3);
  - CPU is disabled
    MCLK, FLL+ loop control, and DCOCLK are disabled
    DCO's dc-generator is disabled
    ACLK remains active
- Low-power mode 4 (LPM4);
  - CPU is disabled
    ACLK is disabled
    MCLK, FLL+ loop control, and DCOCLK are disabled
    DCO's dc-generator is disabled
    Crystal oscillator is stopped

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh − 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Flash Memory	WDTIFG KEYV (see Note 1)	Reset	0FFFEh	15, highest
NMI Oscillator Fault Flash Memory Access Violation	NMIIFG (see Notes 1 and 3) OFIFG (see Notes 1 and 3) ACCVIFG (see Notes 1 and 3)	(Non)maskable (Non)maskable (Non)maskable	0FFFCh	14
Timer_B3	TBCCR0 CCIFG0 (see Note 2)	Maskable	0FFFAh	13
Timer_B3	TBCCR1 CCIFG1, TBCCR2 CCIFG2, TBIFG (see Notes 1 and 2)	Maskable	0FFF8h	12
Comparator_A	CAIFG	Maskable	0FFF6h	11
Watchdog Timer	WDTIFG	Maskable	0FFF4h	10
USART0 Receive	URXIFG0	Maskable	0FFF2h	9
USART0 Transmit	UTXIFG0	Maskable	0FFF0h	8
ADC12	ADC12IFG (see Notes 1 and 2)	Maskable	0FFEEh	7
Timer_A3	TACCR0 CCIFG0 (see Note 2)	Maskable	0FFECh	6
Timer_A3	TACCR1 CCIFG1 and TACCR2 CCIFG2, TAIFG (see Notes 1 and 2)	Maskable	0FFEAh	5
I/O Port P1 (Eight Flags)	P1IFG.0 to P1IFG.7 (see Notes 1 and 2)	Maskable	0FFE8h	4
DAC12 DMA	DAC12.0IFG, DAC12.1IFG, DMA0IFG (see Notes 1 and 2)	Maskable	0FFE6h	3
			0FFE4h	2
I/O Port P2 (Eight Flags)	P2IFG.0 to P2IFG.7 (see Notes 1 and 2)	Maskable	0FFE2h	1
Basic Timer1	BTIFG	Maskable	0FFE0h	0, lowest

NOTES: 1. Multiple source flags
2. Interrupt flags are located in the module.
3. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.

special function registers

The MSP430 special function registers(SFR) are located in the lowest address space, and are organized as byte mode registers. SFRs should be accessed with byte instructions.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h	UTXIE0	URXIE0	ACCVIE	NMIIE			OFIE	WDTIE
	rw–0	rw–0	rw–0	rw–0			rw–0	rw–0

WDTIE: Watchdog-timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured as a general-purpose timer.

OFIE: Oscillator-fault-interrupt enable

NMIIE: Nonmaskable-interrupt enable

ACCVIE: Flash access violation interrupt enable

URXIE0: USART0: UART and SPI receive-interrupt enable

UTXIE0: USART0: UART and SPI transmit-interrupt enable

Address	7	6	5	4	3	2	1	0
01h	BTIE							
	rw–0							

BTIE: Basic timer interrupt enable

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h	UTXIFG0	URXIFG0		NMIIFG			OFIFG	WDTIFG
	rw–1	rw–0		rw–0			rw–1	rw–(0)

WDTIFG: Set on watchdog timer overflow (in watchdog mode) or security key violation
Reset on V_{CC} power-on or a reset condition at the $\overline{RST}$/NMI pin in reset mode

OFIFG: Flag set on oscillator fault

NMIIFG: Set via $\overline{RST}$/NMI pin

URXIFG0: USART0: UART and SPI receive flag

UTXIFG0: USART0: UART and SPI transmit flag

Address	7	6	5	4	3	2	1	0
03h	BTIFG							
	rw–0							

BTIFG: Basic timer flag

module enable registers 1 and 2

Address	7	6	5	4	3	2	1	0
04h	UTXE0	URXE0 USPIE0						
	rw–0	rw–0						

URXE0: USART0: UART mode receive enable

UTXE0: USART0: UART mode transmit enable

USPIE0: USART0: SPI mode transmit and receive enable

Address	7	6	5	4	3	2	1	0
05h								

Legend: rw: **Bit Can Be Read and Written**
rw–0,1: **Bit Can Be Read and Written. It Is Reset or Set by PUC.**
rw–(0,1): **Bit Can Be Read and Written. It Is Reset or Set by POR.**
SFR Bit Not Present in Device

memory organization

		MSP430FG437	MSP430FG438	MSP430FG439
Memory Main: interrupt vector Main: code memory	Size Flash Flash	32KB 0FFFFh − 0FFE0h 0FFFFh − 08000h	48KB 0FFFFh − 0FFE0h 0FFFFh − 04000h	60KB 0FFFFh − 0FFE0h 0FFFFh − 01100h
Information memory	Size Flash	256 Byte 010FFh − 01000h	256 Byte 010FFh − 01000h	256 Byte 010FFh − 01000h
Boot memory	Size ROM	1KB 0FFFh − 0C00h	1KB 0FFFh − 0C00h	1KB 0FFFh − 0C00h
RAM	Size	1KB 05FFh − 0200h	2KB 09FFh − 0200h	2KB 09FFh − 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh − 0100h 0FFh − 010h 0Fh − 00h	01FFh − 0100h 0FFh − 010h 0Fh − 00h	01FFh − 0100h 0FFh − 010h 0Fh − 00h

bootstrap loader (BSL)

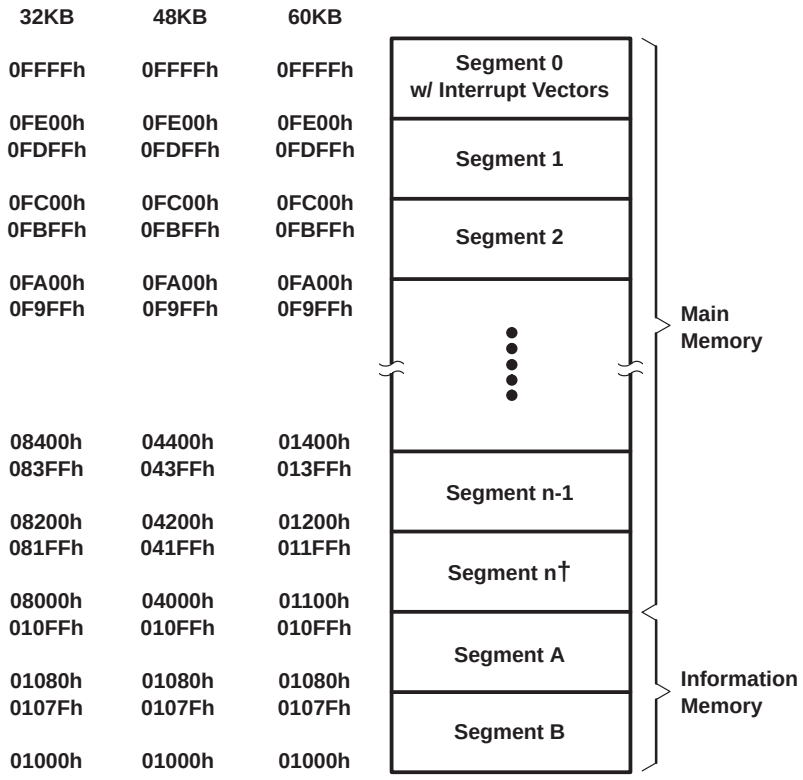
The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the Application report *Features of the MSP430 Bootstrap Loader*, Literature Number SLAA089.

BSL Function	PN Package Pins
Data Transmit	67 − P1.0
Data Receive	66 − P1.1

flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0−n.
  Segments A and B are also called *information memory.*
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.



† MSP430FG439 flash segment n = 256 bytes.

peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430x4xx Family User's Guide*, Literature Number SLAU056.

DMA controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12 conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode without having to awaken to move data to or from a peripheral.

oscillator and system clock

The clock system in the MSP430FG43x family of devices is supported by the FLL+ module that includes support for a 32768 Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high frequency crystal oscillator. The FLL+ clock module is designed to meet the requirements of both low system cost and low-power consumption. The FLL+ features digital frequency locked loop (FLL) hardware which in conjunction with a digital modulator stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 μs. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768 Hz watch crystal or a high frequency crystal.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8.

brownout, supply voltage supervisor

The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The supply voltage supervisor (SVS) circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must insure the default FLL+ settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

digital I/O

There are six 8-bit I/O ports implemented—ports P1 through P6:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.

Basic Timer1

The Basic Timer1 has two independent 8-bit timers which can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. The Basic Timer1 can be used to generate periodic interrupts and clock for the LCD module.

LCD drive

The LCD driver generates the segment and common signals required to drive an LCD display. The LCD controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral.

OA

The MSP430FG43x has three configurable low-current general-purpose operational amplifiers. Each OA input and output terminal is software-selectable and offers a flexible choice of connections for various applications. The OA op amps primarily support front-end analog signal conditioning prior to analog-to-digital conversion.

watchdog timer

The primary function of the watchdog timer (WDT) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

USART0

The MSP430FG43x has one hardware universal synchronous/asynchronous receive transmit (USART) peripheral module that is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels.

timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_A3 Signal Connections

Input Pin Number	Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number
PN					PN
62 - P1.5	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
62 - P1.5	$\overline{\text{TACLK}}$	INCLK			
67 - P1.0	TA0	CCI0A	CCR0	TA0	67 - P1.0
66 - P1.1	TA0	CCI0B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
65 - P1.2	TA1	CCI1A	CCR1	TA1	65 - P1.2
	CAOUT (internal)	CCI1B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
59 - P2.0	TA2	CCI2A	CCR2	TA2	59 - P2.0
	ACLK (internal)	CCI2B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

timer_B3

Timer_B3 is a 16-bit timer/counter with three capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_B3 Signal Connections					
Input Pin Number PN	Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number PN
63 - P1.4	TBCLK	TBCLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
63 - P1.4	$\overline{\text{TBCLK}}$	INCLK			
58 - P2.1	TB0	CCI0A	CCR0	TB0	58 - P2.1
58 - P2.1	TB0	CCI0B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
57 - P2.2	TB1	CCI1A	CCR1	TB1	57 - P2.2
57 - P2.2	TB1	CCI1B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
56 - P2.3	TB2	CCI2A	CCR2	TB2	56 - P2.3
56 - P2.3	TB2	CCI2B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

comparator_A

The primary function of the comparator_A module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

ADC12

The ADC12 module supports fast, 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator and a 16 word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

DAC12

The DAC12 module is a 12-bit, R-ladder, voltage output DAC. The DAC12 may be used in 8- or 12-bit mode, and may be used in conjunction with the DMA controller. When multiple DAC12 modules are present, they may be grouped together for synchronous operation.

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Watchdog	Watchdog timer control	WDTCTL	0120h
Timer_B3	Capture/compare register 2	TBCCR2	0196h
	Capture/compare register 1	TBCCR1	0194h
	Capture/compare register 0	TBCCR0	0192h
	Timer_B register	TBR	0190h
	Capture/compare control 2	TBCCTL2	0186h
	Capture/compare control 1	TBCCTL1	0184h
	Capture/compare control 0	TBCCTL0	0182h
	Timer_B control	TBCTL	0180h
	Timer_B interrupt vector	TBIV	011Eh
Timer_A3	Capture/compare register 2	TACCR2	0176h
	Capture/compare register 1	TACCR1	0174h
	Capture/compare register 0	TACCR0	0172h
	Timer_A register	TAR	0170h
	Capture/compare control 2	TACCTL2	0166h
	Capture/compare control 1	TACCTL1	0164h
	Capture/compare control 0	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Flash	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
DMA	DMA module control 0	DMACTL0	0122h
	DMA module control 1	DMACTL1	0124h
	DMA channel 0 control	DMA0CTL	01E0h
	DMA channel 0 source address	DMA0SA	01E2h
	DMA channel 0 destination address	DMA0DA	01E4h
	DMA channel 0 transfer size	DMA0SZ	01E6h

peripheral file map (continued)

PERIPHERALS WITH WORD ACCESS (CONTINUED)			
ADC12 See also *Peripherals with Byte Access*	Conversion memory 15	ADC12MEM15	015Eh
	Conversion memory 14	ADC12MEM14	015Ch
	Conversion memory 13	ADC12MEM13	015Ah
	Conversion memory 12	ADC12MEM12	0158h
	Conversion memory 11	ADC12MEM11	0156h
	Conversion memory 10	ADC12MEM10	0154h
	Conversion memory 9	ADC12MEM9	0152h
	Conversion memory 8	ADC12MEM8	0150h
	Conversion memory 7	ADC12MEM7	014Eh
	Conversion memory 6	ADC12MEM6	014Ch
	Conversion memory 5	ADC12MEM5	014Ah
	Conversion memory 4	ADC12MEM4	0148h
	Conversion memory 3	ADC12MEM3	0146h
	Conversion memory 2	ADC12MEM2	0144h
	Conversion memory 1	ADC12MEM1	0142h
	Conversion memory 0	ADC12MEM0	0140h
	Interrupt-vector-word register	ADC12IV	01A8h
	Inerrupt-enable register	ADC12IE	01A6h
	Inerrupt-flag register	ADC12IFG	01A4h
	Control register 1	ADC12CTL1	01A2h
	Control register 0	ADC12CTL0	01A0h
DAC12	DAC12_1 data	DAC12_1DAT	01CAh
	DAC12_1 control	DAC12_1CTL	01C2h
	DAC12_0 data	DAC12_0DAT	01C8h
	DAC12_0 control	DAC12_0CTL	01C0h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS			
OA2	Operational Amplifier 2 control register 1	OA2CTL1	0C5h
	Operational Amplifier 2 control register 0	OA2CTL0	0C4h
OA1	Operational Amplifier 1 control register 1	OA1CTL1	0C3h
	Operational Amplifier 1 control register 0	OA1CTL0	0C2h
OA0	Operational Amplifier 0 control register 1	OA0CTL1	0C1h
	Operational Amplifier 0 control register 0	OA0CTL0	0C0h
LCD	LCD memory 20	LCDM20	0A4h
	:	:	:
	LCD memory 16	LCDM16	0A0h
	LCD memory 15	LCDM15	09Fh
	:	:	:
	LCD memory 1	LCDM1	091h
	LCD control and mode	LCDCTL	090h
ADC12 (Memory control registers require byte access)	ADC memory-control register 15	ADC12MCTL15	08Fh
	ADC memory-control register 14	ADC12MCTL14	08Eh
	ADC memory-control register 13	ADC12MCTL13	08Dh
	ADC memory-control register 12	ADC12MCTL12	08Ch
	ADC memory-control register 11	ADC12MCTL11	08Bh
	ADC memory-control register 10	ADC12MCTL10	08Ah
	ADC memory-control register 9	ADC12MCTL9	089h
	ADC memory-control register 8	ADC12MCTL8	088h
	ADC memory-control register 7	ADC12MCTL7	087h
	ADC memory-control register 6	ADC12MCTL6	086h
	ADC memory-control register 5	ADC12MCTL5	085h
	ADC memory-control register 4	ADC12MCTL4	084h
	ADC memory-control register 3	ADC12MCTL3	083h
	ADC memory-control register 2	ADC12MCTL2	082h
	ADC memory-control register 1	ADC12MCTL1	081h
	ADC memory-control register 0	ADC12MCTL0	080h
USART0 (UART or SPI mode)	Transmit buffer	U0TXBUF	077h
	Receive buffer	U0RXBUF	076h
	Baud rate	U0BR1	075h
	Baud rate	U0BR0	074h
	Modulation control	U0MCTL	073h
	Receive control	U0RCTL	072h
	Transmit control	U0TCTL	071h
	USART control	U0CTL	070h
Comparator_A	Comparator_A port disable	CAPD	05Bh
	Comparator_A control 2	CACTL2	05Ah
	Comparator_A control 1	CACTL1	059h
BrownOUT, SVS	SVS control register (Reset by brownout signal)	SVSCTL	056h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
FLL+Clock	FLL+ Control 1	FLL_CTL1	054h
	FLL+ Control 0	FLL_CTL0	053h
	System clock frequency control	SCFQCTL	052h
	System clock frequency integrator	SCFI1	051h
	System clock frequency integrator	SCFI0	050h
Basic Timer1	BT counter 2	BTCNT2	047h
	BT counter 1	BTCNT1	046h
	BT control	BTCTL	040h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage applied at V_{CC} to V_{SS} . . . . . −0.3 V to 4.1 V
Voltage applied to any pin (see Note) . . . . . −0.3 V to V_{CC} + 0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature, T_{stg}: (unprogrammed device) . . . . . −55°C to 150°C
(programmed device) . . . . . −40°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

recommended operating conditions

			MIN	NOM	MAX	UNITS
Supply voltage during program execution, V_{CC} (AV_{CC} = $DV_{CC1/2}$ = V_{CC})			1.8		3.6	V
Supply voltage during flash memory programming, V_{CC} (AV_{CC} = $DV_{CC1/2}$ = V_{CC})			2.7		3.6	V
Supply voltage during program execution, SVS enabled (see Note 1), V_{CC} (AV_{CC} = $DV_{CC1/2}$ = V_{CC})			2		3.6	V
Supply voltage, V_{SS} (AV_{SS} = $DV_{SS1/2}$ = V_{SS})			0		0	V
Operating free-air temperature range, T_A			−40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Note 2)	LF selected, XTS_FLL=0	Watch crystal		32.768		kHz
	XT1 selected, XTS_FLL=1	Ceramic resonator	450		8000	kHz
	XT1 selected, XTS_FLL=1	Crystal	1000		8000	kHz
XT2 crystal frequency, $f_{(XT2)}$		Ceramic resonator	450		8000	kHz
		Crystal	1000		8000	
Processor frequency (signal MCLK), $f_{(System)}$		V_{CC} = 1.8 V	DC		4.15	MHz
		V_{CC} = 3.6 V	DC		8	

NOTES: 1. The minimum operating supply voltage is defined according to the trip point where POR is going active by decreasing the supply voltage. POR is going inactive when the supply voltage is raised above the minimum supply voltage plus the hysteresis of the SVS circuitry.
2. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.

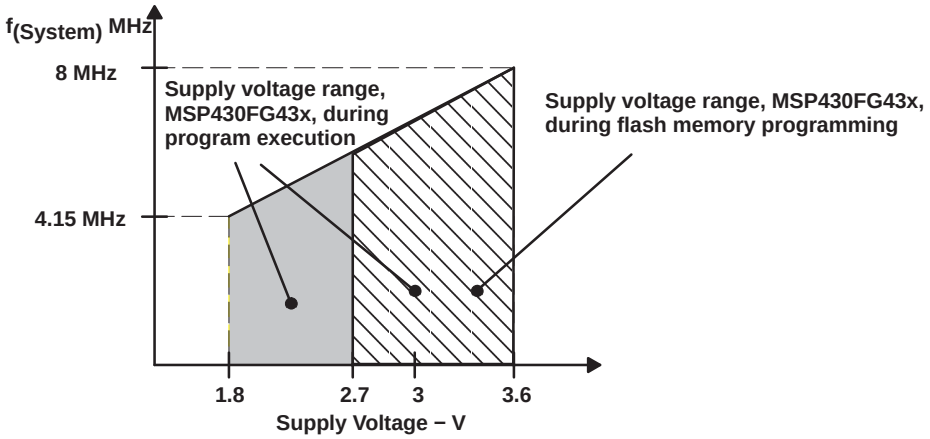


Figure 1. Frequency vs Supply Voltage, typical characteristic

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

supply current into AV_{CC} + $DV_{CC1/2}$ excluding external current

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active mode, (see Note 1) $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz XTS_FLL=0, SELM=(0,1)	T_A = −40°C to 85°C	V_{CC} = 2.2 V		300	370	µA
			V_{CC} = 3 V		470	570	
$I_{(LPM0)}$	Low-power mode, (LPM0) (see Note 1)	T_A = −40°C to 85°C	V_{CC} = 2.2 V		55	70	µA
			V_{CC} = 3 V		95	110	
$I_{(LPM2)}$	Low-power mode, (LPM2), f(MCLK) = f (SMCLK) = 0 MHz, f(ACLK) = 32,768 Hz, SCG0 = 0 (see Note 2)	T_A = −40°C to 85°C	V_{CC} = 2.2 V		11	14	µA
			V_{CC} = 3 V		17	22	
$I_{(LPM3)}$	Low-power mode, (LPM3) $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1 (see Note 2 and Note 3)	T_A = −40°C	V_{CC} = 2.2 V		1	2.0	µA
		T_A = 25°C			1.1	2.0	
		T_A = 60°C			2	3	
		T_A = 85°C			3.5	6	
		T_A = −40°C	V_{CC} = 3 V		1.8	2.8	
		T_A = 25°C			1.6	2.7	
		T_A = 60°C			2.5	3.5	
		T_A = 85°C			4.2	7.5	
$I_{(LPM4)}$	Low-power mode, (LPM4) $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1 (see Note 2)	T_A = −40°C	V_{CC} = 2.2 V		0.1	0.5	µA
		T_A = 25°C			0.1	0.5	
		T_A = 60°C			0.7	1.1	
		T_A = 85°C			1.7	3	
		T_A = −40°C	V_{CC} = 3 V		0.1	0.8	
		T_A = 25°C			0.1	0.8	
		T_A = 60°C			0.8	1.2	
		T_A = 85°C			1.9	3.5	

NOTES: 1. Timer_B is clocked by $f_{(DCOCLK)}$ = 1 MHz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
2. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
3. The current consumption in LPM3 is measured with active Basic Timer1 and LCD (ACLK selected). The current consumption of the Comparator_A and the SVS module are specified in the respective sections. The LPM3 currents are characterized with a KDS Daishinku DT−38 (6 pF) crystal and OSCCAPx=01h.

Current consumption of active mode versus system frequency, F-version:

$$I_{(AM)} = I_{(AM)}\,[1\text{ MHz}] \times f_{(System)}\,[\text{MHz}]$$

Current consumption of active mode versus supply voltage, F-version:

$$I_{(AM)} = I_{(AM)\,[3\text{ V}]} + 175\ \mu\text{A/V} \times (V_{CC} - 3\text{ V})$$

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SCHMITT-trigger inputs − Ports P1, P2, P3, P4, P5, and P6; $\overline{\text{RST}}$/NMI; JTAG: TCK, TMS, TDI/TCLK, TDO/TDI

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1		1.55	V
		V_{CC} = 3 V	1.5		1.98	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4		0.9	V
		V_{CC} = 3 V	0.9		1.3	
V_{hys}	Input voltage hysteresis (V_{IT+} − V_{IT-})	V_{CC} = 2.2 V	0.3		1.1	V
		V_{CC} = 3 V	0.5		1	

inputs Px.x, TAx, TBx

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag, (see Note 1)	2.2 V	62			ns
			3 V	50			
$t_{(cap)}$	Timer_A, Timer_B capture timing	TA0, TA1, TA2 TB0, TB1, TB2	2.2 V	62			ns
			3 V	50			
$f_{(TAext)}$	Timer_A, Timer_B clock frequency externally applied to pin	TACLK, TBCLK, INCLK: $t_{(H)} = t_{(L)}$	2.2 V			8	MHz
$f_{(TBext)}$			3 V			10	
$f_{(TAint)}$	Timer_A, Timer_B clock frequency	SMCLK or ACLK signal selected	2.2 V			8	MHz
$f_{(TBint)}$			3 V			10	

NOTES: 1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$.

leakage current − Ports P1, P2, P3, P4, P5, and P6 (see Note 1)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{lkg(Px.y)}$	Leakage current	Port Px	$V_{(Px.y)}$ (see Note 2)	V_{CC} = 2.2 V/3 V			±50	nA

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs − Ports P1, P2, P3, P4, P5, and P6

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = −1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{CC}−0.25		V_{CC}	V
		$I_{OH(max)}$ = −6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{CC}−0.6		V_{CC}	
		$I_{OH(max)}$ = −1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{CC}−0.25		V_{CC}	
		$I_{OH(max)}$ = −6 mA,	V_{CC} = 3 V,	See Note 2	V_{CC}−0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{SS}		V_{SS}+0.25	V
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{SS}		V_{SS}+0.6	
		$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{SS}		V_{SS}+0.25	
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 3 V,	See Note 2	V_{SS}		V_{SS}+0.6	

NOTES: 1. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
2. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

output frequency

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(Px.y)}$	(1 ≤ x ≤ 6, 0 ≤ y ≤ 7)	C_L = 20 pF, I_L = ±1.5 mA	V_{CC} = 2.2 V / 3 V	DC		f_{System}	MHz
$f_{(MCLK)}$ $f_{(SMCLK)}$ $f_{(ACLK)}$	P1.1/TA0/MCLK, P1.4/TBCLK/SMCLK, P1.5/TACLK/ACLK	C_L = 20 pF				f_{System}	MHz
$t_{(Xdc)}$	Duty cycle of output frequency	P1.5/TACLK/ACLK, C_L = 20 pF V_{CC} = 2.2 V / 3 V	$f_{(ACLK)} = f_{(LFXT1)} = f_{(XT1)}$	40%		60%	
			$f_{(ACLK)} = f_{(LFXT1)} = f_{(LF)}$	30%		70%	
			$f_{(ACLK)} = f_{(LFXT1)}$		50%		
		P1.1/TA0/MCLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{(MCLK)} = f_{(XT1)}$	40%		60%	
			$f_{(MCLK)} = f_{(DCOCLK)}$	50%− 15 ns	50%	50%+ 15 ns	
		P1.4/TBCLK/SMCLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{(SMCLK)} = f_{(XT2)}$	40%		60%	
			$f_{(SMCLK)} = f_{(DCOCLK)}$	50%− 15 ns	50%	50%+ 15 ns	

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs − Ports P1, P2, P3, P4, P5, and P6 (continued)

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

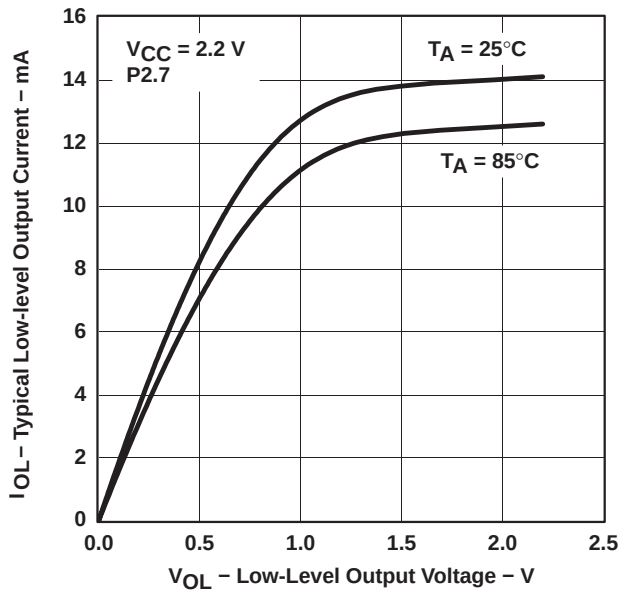


Figure 2

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

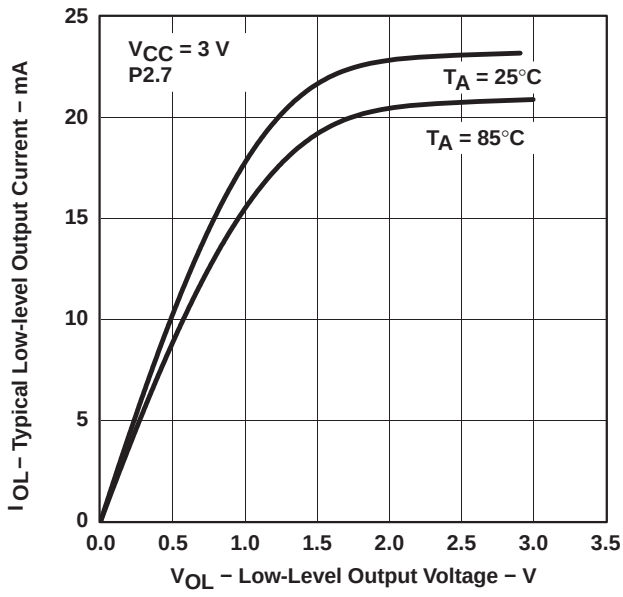


Figure 3

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

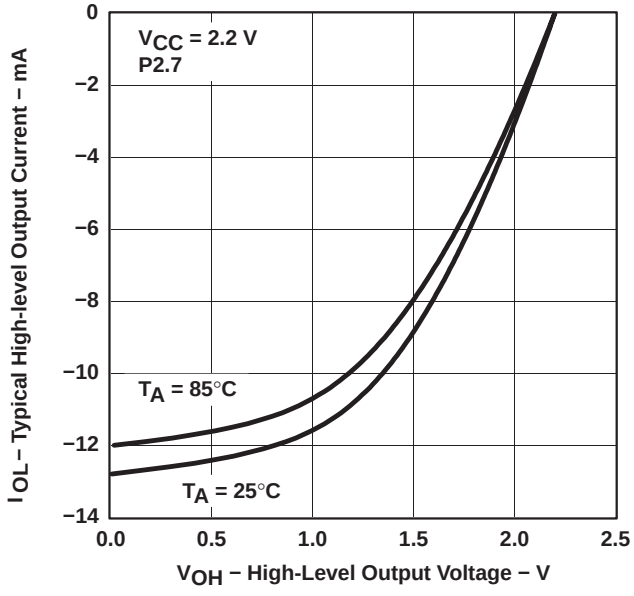


Figure 4

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

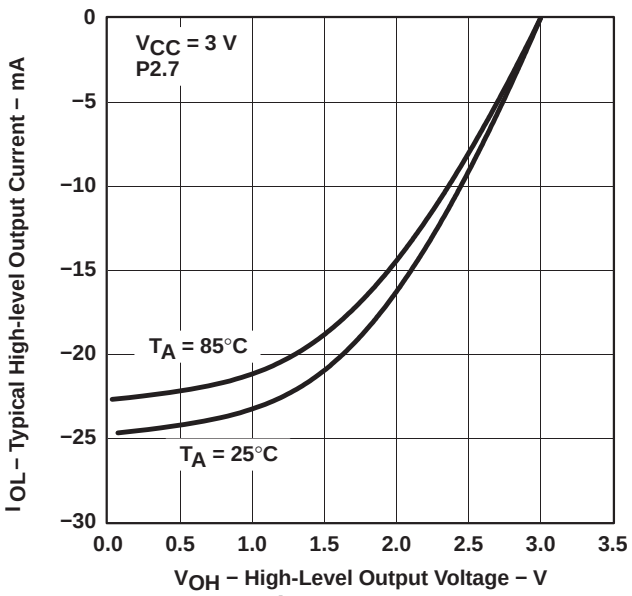


Figure 5

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

wake-up LPM3

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(LPM3)}$	Delay time	f = 1 MHz	V_{CC} = 2.2 V/3 V			6	µs
		f = 2 MHz				6	
		f = 3 MHz				6	

RAM

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VRAMh	CPU halted (see Note 1)	1.6			V

NOTE 1: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

LCD

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(33)}$	Analog voltage	Voltage at P5.7/R33	V_{CC} = 3 V	2.5		V_{CC} + 0.2	V
$V_{(23)}$		Voltage at P5.6/R23			$[V_{(33)}-V_{(03)}] \times 2/3 + V_{(03)}$		
$V_{(13)}$		Voltage at P5.5/R13			$[V_{(33)}-V_{(03)}] \times 1/3 + V_{(03)}$		
$V_{(33)} - V_{(03)}$		Voltage at R33 to R03		2.5		V_{CC} + 0.2	
$I_{(R03)}$	Input leakage	R03 = V_{SS}	No load at all segment and common lines, V_{CC} = 3 V			±20	nA
$I_{(R13)}$		P5.5/R13 = $V_{CC}/3$				±20	
$I_{(R23)}$		P5.6/R23 = $2 \times V_{CC}/3$				±20	
$V_{(Sxx0)}$	Segment line voltage	$I_{(Sxx)}$ = −3 µA,	V_{CC} = 3 V	$V_{(03)}$		$V_{(03)}$ − 0.1	V
$V_{(Sxx1)}$				$V_{(13)}$		$V_{(13)}$ − 0.1	
$V_{(Sxx2)}$				$V_{(23)}$		$V_{(23)}$ − 0.1	
$V_{(Sxx3)}$				$V_{(33)}$		$V_{(33)}$ + 0.1	

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Comparator_A (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(CC)}$		CAON=1, CARSEL=0, CAREF=0	V_{CC} = 2.2 V		25	40	µA
			V_{CC} = 3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON=1, CARSEL=0, CAREF=1/2/3, No load at P1.6/CA0 and P1.7/CA1	V_{CC} = 2.2 V		30	50	µA
			V_{CC} = 3 V		45	71	
$V_{(Ref025)}$	$\frac{\text{Voltage @ 0.25 } V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=1, No load at P1.6/CA0 and P1.7/CA1	V_{CC} = 2.2 V / 3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	$\frac{\text{Voltage @ 0.5 } V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=2, No load at P1.6/CA0 and P1.7/CA1	V_{CC} = 2.2V / 3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	see Figure 6 and Figure 7	PCA0=1, CARSEL=1, CAREF=3, No load at P1.6/CA0 and P1.7/CA1; T_A = 85°C	V_{CC} = 2.2 V	390	480	540	mV
			V_{CC} = 3 V	400	490	550	
V_{IC}	Common-mode input voltage range	CAON=1	V_{CC} = 2.2 V / 3 V	0		V_{CC}−1	V
V_p−V_S	Offset voltage	See Note 2	VCC = 2.2 V / 3 V	−30		30	mV
V_{hys}	Input hysteresis	CAON = 1	V_{CC} = 2.2 V / 3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$		T_A = 25°C, Overdrive 10 mV, without filter: CAF = 0	V_{CC} = 2.2 V	160	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C Overdrive 10 mV, with filter: CAF = 1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3 V	0.9	1.5	2.6	
$t_{(response\ HL)}$		T_A = 25°C Overdrive 10 mV, without filter: CAF = 0	V_{CC} = 2.2 V	130	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, with filter: CAF = 1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3 V	0.9	1.5	2.6	

NOTES: 1. The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.

typical characteristics

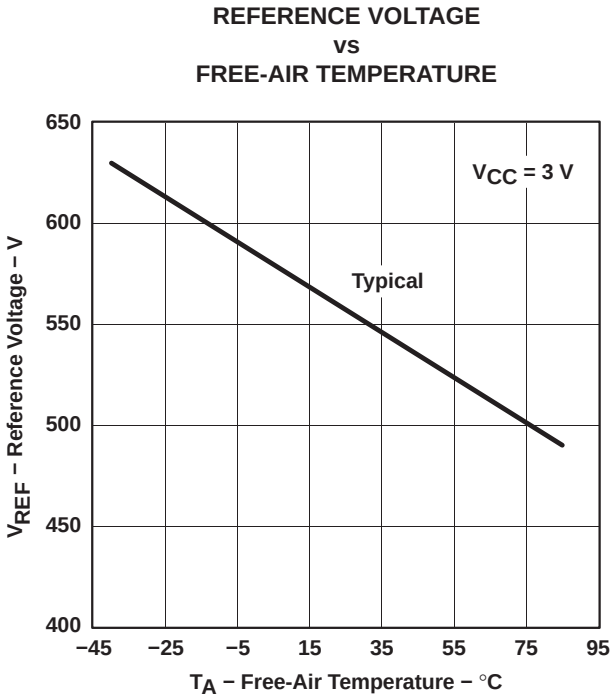


Figure 6. $V_{(RefVT)}$ vs Temperature

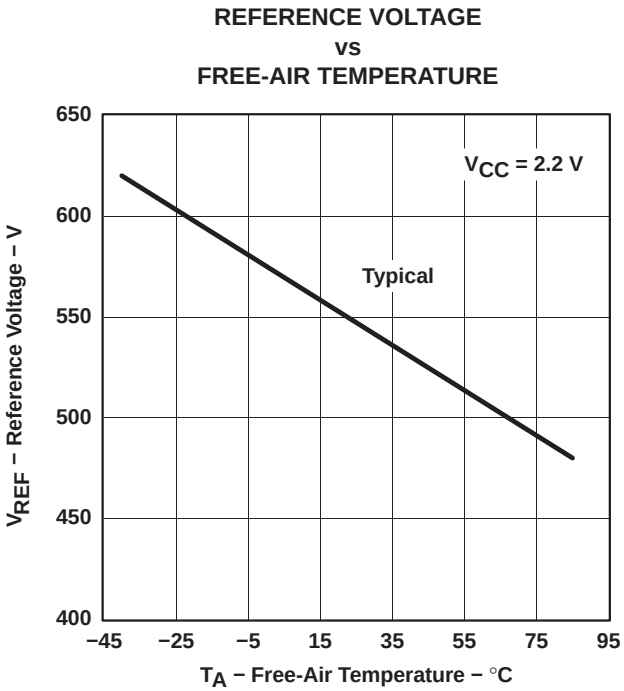


Figure 7. $V_{(RefVT)}$ vs Temperature

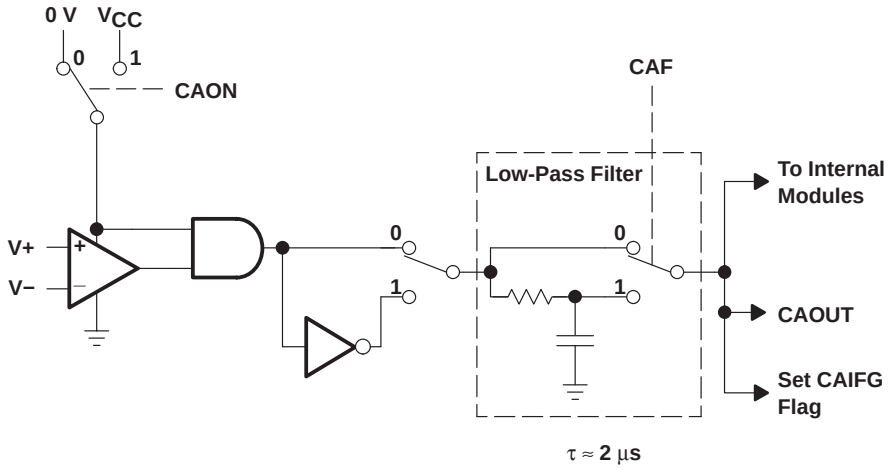


Figure 8. Block Diagram of Comparator_A Module

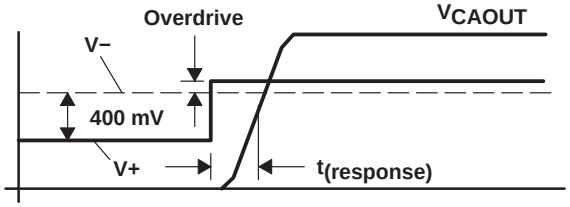


Figure 9. Overdrive Definition

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

POR/brownout reset (BOR) (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(BOR)}$	Brownout (see Note 2)				2000	µs
$V_{CC(start)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 10)		$0.7 \times V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 10 through Figure 12)			1.71	V
$V_{hys(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 10)	70	130	180	mV
$t_{(reset)}$		Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally, V_{CC} = 2.2 V/3 V	2			µs

NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8V.

2. During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default FLL+ settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency. See the *MSP430x4xx Family User's Guide* (SLAU056) for more information on the brownout/SVS circuit.

typical characteristics

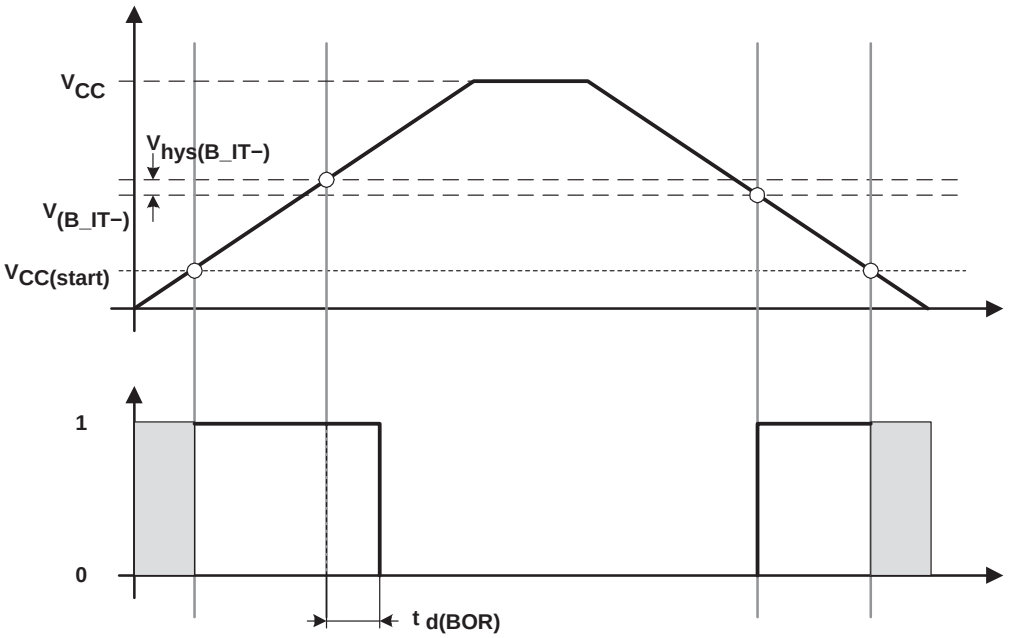


Figure 10. POR/Brownout Reset (BOR) vs Supply Voltage

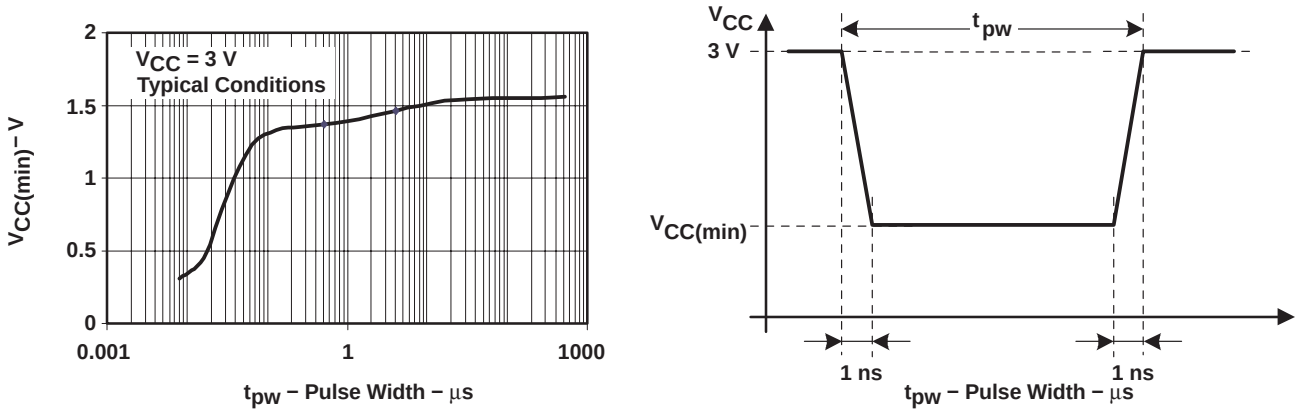


Figure 11. $V_{(CC)min}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

typical characteristics

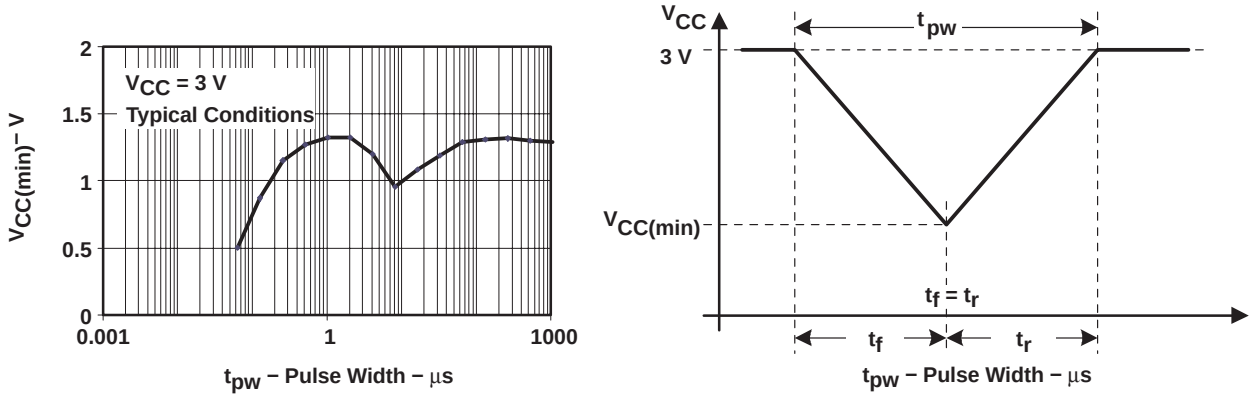


Figure 12. $V_{CC(min)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

SVS (supply voltage supervisor/monitor)

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT
$t_{(SVSR)}$	dV_{CC}/dt > 30 V/ms (see Figure 13)		5		150	µs
	$dV_{CC}/dt \le 30$ V/ms				2000	µs
$t_{d(SVSon)}$	SVSon, switch from VLD=0 to VLD ≠ 0, V_{CC} = 3 V		20		150	µs
t_{settle}	VLD ≠ 0‡				12	µs
$V_{(SVSstart)}$	VLD ≠ 0, $V_{CC}/dt \le 3$ V/s (see Figure 13)			1.55	1.7	V
$V_{hys(SVS\_IT-)}$	$V_{CC}/dt \le 3$ V/s (see Figure 13)	VLD = 1	70	120	155	mV
		VLD = 2 .. 14	$V_{(SVS\_IT-)}$ x 0.001		$V_{(SVS\_IT-)}$ x 0.016	
	$V_{CC}/dt \le 3$ V/s (see Figure 13), external voltage applied on A7	VLD = 15	4.4		20	mV
$V_{(SVS\_IT-)}$	$V_{CC}/dt \le 3$ V/s (see Figure 13)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.23	
		VLD = 3	2.05	2.2	2.35	
		VLD = 4	2.14	2.3	2.46	
		VLD = 5	2.24	2.4	2.58	
		VLD = 6	2.33	2.5	2.69	
		VLD = 7	2.46	2.65	2.84	
		VLD = 8	2.58	2.8	2.97	
		VLD = 9	2.69	2.9	3.10	
		VLD = 10	2.83	3.05	3.26	
		VLD = 11	2.94	3.2	3.39	
		VLD = 12	3.11	3.35	3.58†	
		VLD = 13	3.24	3.5	3.73†	
		VLD = 14	3.43	3.7†	3.96†	
	$V_{CC}/dt \le 3$ V/s (see Figure 13), external voltage applied on A7	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$ (see Note 1)	VLD ≠ 0, V_{CC} = 2.2 V/3 V			10	15	µA

† The recommended operating voltage range is limited to 3.6 V.

‡ t_{settle} is the settling time that the comparator o/p needs to have a stable level after VLD is switched VLD ≠ 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be > 50 mV.

NOTE 1: The current consumption of the SVS module is not included in the I_{CC} current consumption data.

typical characteristics

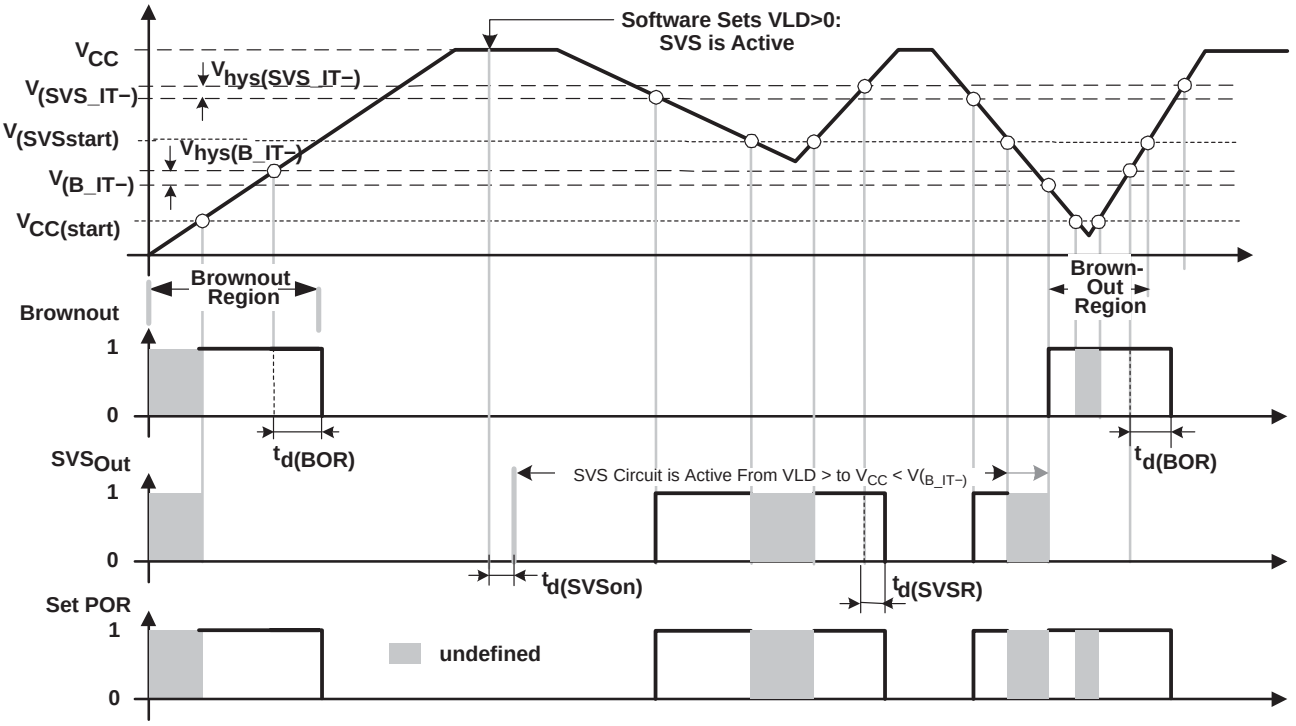


Figure 13. SVS Reset (SVSR) vs Supply Voltage

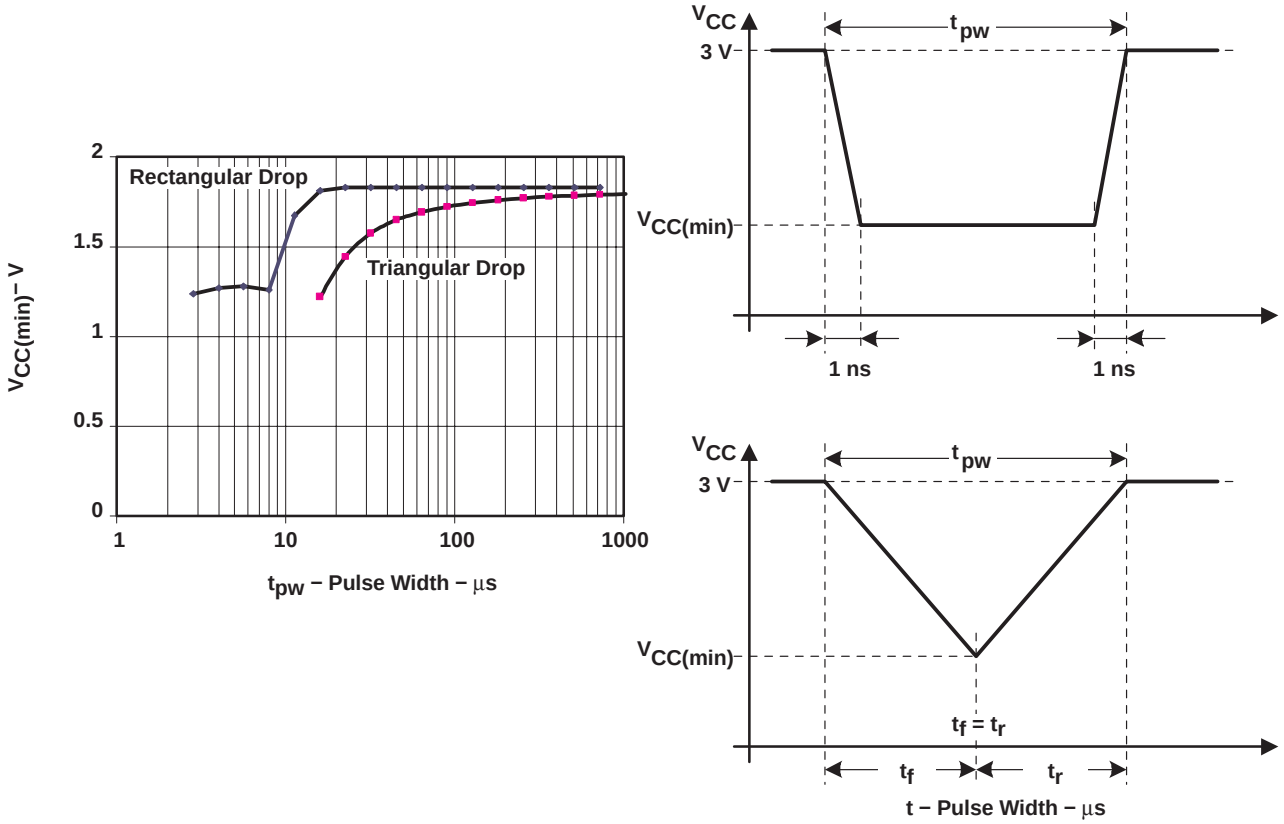


Figure 14. $V_{CC(min)}$ With a Square Voltage Drop and a Triangle Voltage Drop to Generate an SVS Signal

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

DCO

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{(DCOCLK)}$	$N_{(DCO)}$=01E0h, FN_8=FN_4=FN_3=FN_2=0, D = 2; DCOPLUS= 0	2.2 V/3 V		1		MHz
$f_{(DCO2)}$	FN_8=FN_4=FN_3=FN_2=0 ; DCOPLUS = 1	2.2 V	0.3	0.65	1.25	MHz
		3 V	0.3	0.7	1.3	
$f_{(DCO27)}$	FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1, (see Note 1)	2.2 V	2.5	5.6	10.5	MHz
		3 V	2.7	6.1	11.3	
$f_{(DCO2)}$	FN_8=FN_4=FN_3=0, FN_2=1; DCOPLUS = 1	2.2 V	0.7	1.3	2.3	MHz
		3 V	0.8	1.5	2.5	
$f_{(DCO27)}$	FN_8=FN_4=FN_3=0, FN_2=1; DCOPLUS = 1, (see Note 1)	2.2 V	5.7	10.8	18	MHz
		3 V	6.5	12.1	20	
$f_{(DCO2)}$	FN_8=FN_4=0, FN_3= 1, FN_2=x; DCOPLUS = 1	2.2 V	1.2	2	3	MHz
		3 V	1.3	2.2	3.5	
$f_{(DCO27)}$	FN_8=FN_4=0, FN_3= 1, FN_2=x; DCOPLUS = 1, (see Note 1)	2.2 V	9	15.5	25	MHz
		3 V	10.3	17.9	28.5	
$f_{(DCO2)}$	FN_8=0, FN_4= 1, FN_3= FN_2=x; DCOPLUS = 1	2.2 V	1.8	2.8	4.2	MHz
		3 V	2.1	3.4	5.2	
$f_{(DCO27)}$	FN_8=0, FN_4=1, FN_3= FN_2=x; DCOPLUS = 1, (see Note 1)	2.2 V	13.5	21.5	33	MHz
		3 V	16	26.6	41	
$f_{(DCO2)}$	FN_8=1, FN_4=FN_3=FN_2=x; DCOPLUS = 1	2.2 V	2.8	4.2	6.2	MHz
		3 V	4.2	6.3	9.2	
$f_{(DCO27)}$	FN_8=1,FN_4=FN_3=FN_2=x; DCOPLUS = 1, (see Note 1)	2.2 V	21	32	46	MHz
		3 V	30	46	70	
S_n	Step size between adjacent DCO taps: $S_n = f_{DCO(Tap\ n+1)} / f_{DCO(Tap\ n)}$, (see Figure 16 for taps 21 to 27)	1 < TAP ≤ 20	1.06		1.11	
		TAP = 27	1.07		1.17	
D_t	Temperature drift, $N_{(DCO)}$ = 01E0h, FN_8=FN_4=FN_3=FN_2=0 D = 2; DCOPLUS = 0, (see Note 2)	2.2 V	–0.2	–0.3	–0.4	%/°C
		3 V	–0.2	–0.3	–0.4	
D_V	Drift with V_{CC} variation, $N_{(DCO)}$ = 01E0h, FN_8=FN_4=FN_3=FN_2=0 D = 2; DCOPLUS = 0 (see Note 2)	2.2 V/ 3 V	0	5	15	%/V

NOTES: 1. Do not exceed the maximum system frequency.
2. This parameter is not production tested.

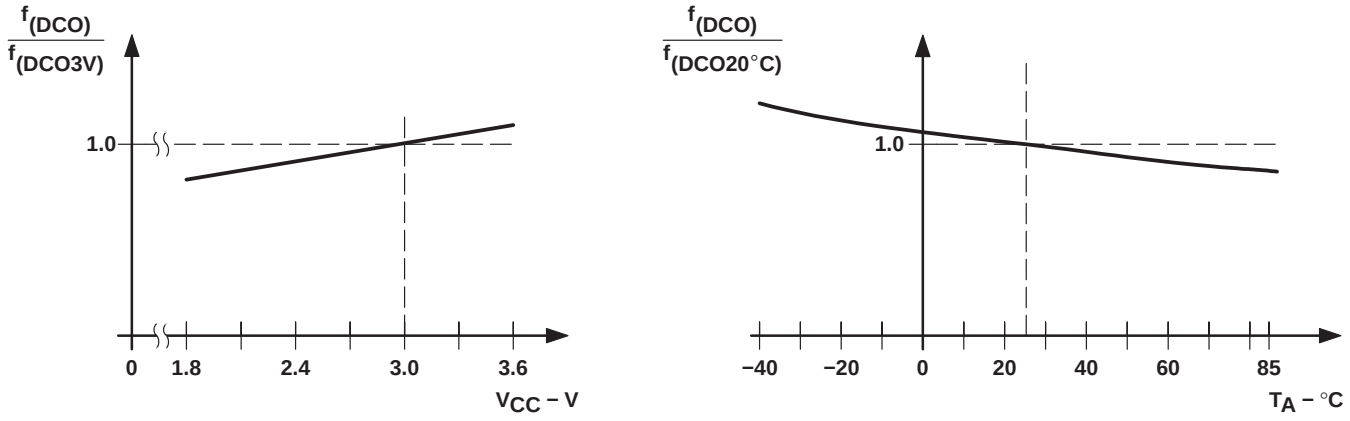


Figure 15. DCO Frequency vs Supply Voltage V_{CC} and vs Ambient Temperature

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

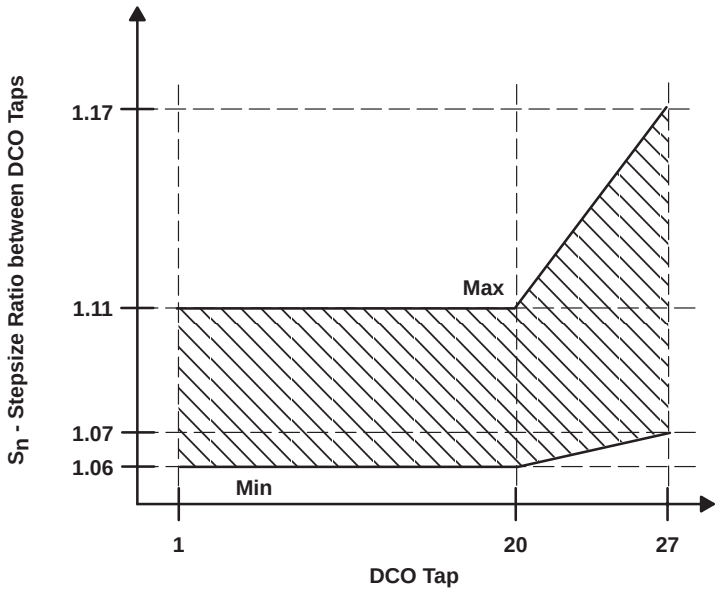


Figure 16. DCO Tap Step Size

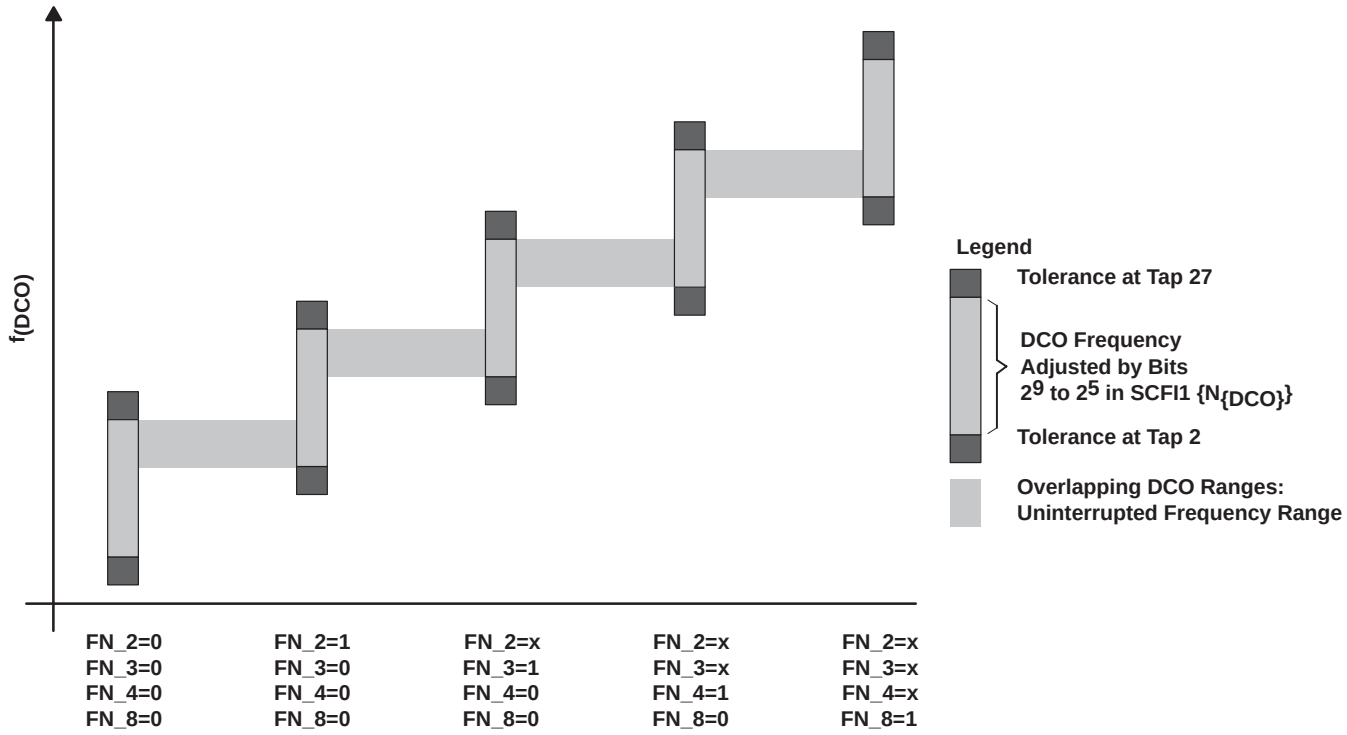


Figure 17. Five Overlapping DCO Ranges Controlled by FN_x Bits

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

crystal oscillator, LFXT1 oscillator (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{XIN}	Integrated input capacitance (see Note 4)	OSCCAPx = 0h, V_{CC} = 2.2 V / 3 V		0		pF
		OSCCAPx = 1h, V_{CC} = 2.2 V / 3 V		10		
		OSCCAPx = 2h, V_{CC} = 2.2 V / 3 V		14		
		OSCCAPx = 3h, V_{CC} = 2.2 V / 3 V		18		
C_{XOUT}	Integrated output capacitance (see Note 4)	OSCCAPx = 0h, V_{CC} = 2.2 V / 3 V		0		pF
		OSCCAPx = 1h, V_{CC} = 2.2 V / 3 V		10		
		OSCCAPx = 2h, V_{CC} = 2.2 V / 3 V		14		
		OSCCAPx = 3h, V_{CC} = 2.2 V / 3 V		18		
V_{IL}	Input levels at XIN	V_{CC} = 2.2 V/3 V (see Note 3)	V_{SS}		$0.2 \times V_{CC}$	V
V_{IH}			$0.8 \times V_{CC}$		V_{CC}	

NOTES: 1. The parasitic capacitance from the package and board may be estimated to be 2 pF. The effective load capacitor for the crystal is $(C_{XIN} \times C_{XOUT}) / (C_{XIN} + C_{XOUT})$. This is independent of XTS_FLL.
2. To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines should be observed.
   - Keep as short of a trace as possible between the ’FG43x and the crystal.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
3. Applies only when using an external logic-level clock source. XTS_FLL must be set. Not applicable when using a crystal or resonator.
4. External capacitance is recommended for precision real-time clock applications; OSCCAPx = 0h.

crystal oscillator, XT2 oscillator (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
C_{XT2IN}	Integrated input capacitance	V_{CC} = 2.2 V/3 V		2		pF
C_{XT2OUT}	Integrated output capacitance	V_{CC} = 2.2 V/3 V		2		pF
V_{IL}	Input levels at XT2IN	V_{CC} = 2.2 V/3 V (see Note 2)	V_{SS}		$0.2 \times V_{CC}$	V
V_{IH}			$0.8 \times V_{CC}$		V_{CC}	V

NOTES: 1. The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.
2. Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

USART0 (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{(\tau)}$	USART0: deglitch time	V_{CC} = 2.2 V	200	430	800	ns
		V_{CC} = 3 V	150	280	500	

NOTES: 1. The signal applied to the USART0 receive signal/terminal (URXD0) should meet the timing requirements of $t_{(\tau)}$ to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of $t_{(\tau)}$. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD0 line.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, power supply and input range conditions (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together AV_{SS} and DV_{SS} are connected together $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{(P6.x/Ax)}$	Analog input voltage range (see Note 2)	All external Ax terminals. Analog inputs selected in ADC12MCTLx register and P6Sel.x=1 $V_{(AVSS)} \le V_{Ax} \le V_{(AVCC)}$		0		V_{AVCC}	V
I_{ADC12}	Operating supply current into AV_{CC} terminal (see Note 3)	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 1, REFON = 0 SHT0=0, SHT1=0, ADC12DIV=0	V_{CC} = 2.2 V		0.65	1.3	mA
			V_{CC} = 3 V		0.8	1.6	
I_{REF+}	Operating supply current into AV_{CC} terminal (see Note 4)	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 0, REFON = 1, REF2_5V = 1	V_{CC} = 3 V		0.5	0.8	mA
		$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 0, REFON = 1, REF2_5V = 0	V_{CC} = 2.2 V		0.5	0.8	mA
			V_{CC} = 3 V		0.5	0.8	
C_I †	Input capacitance	Only one terminal can be selected at one time, Ax	V_{CC} = 2.2 V			40	pF
R_I†	Input MUX ON resistance	$0V \le V_{Ax} \le V_{AVCC}$	V_{CC} = 3 V			2000	Ω

† Not production tested, limits verified by design

NOTES: 1. The leakage current is defined in the leakage current table with Ax parameter.
2. The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
3. The internal reference supply current is not included in current consumption parameter I_{ADC12}.
4. The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

12-bit ADC, external reference (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 2)		1.4		V_{AVCC}	V
V_{REF-}/V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 3)		0		1.2	V
$(V_{eREF+} - V_{REF-}/V_{eREF-})$	Differential external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 4)		1.4		V_{AVCC}	V
I_{VeREF+}	Static input current	$0V \le V_{eREF+} \le V_{AVCC}$	V_{CC} = 2.2 V/3 V			±1	µA
$I_{VREF-/VeREF-}$	Static input current	$0V \le V_{eREF-} \le V_{AVCC}$	V_{CC} = 2.2 V/3 V			±1	µA

NOTES: 1. The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
2. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
3. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
4. The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, built-in reference

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REF2_5V = 1 for 2.5 V $I_{VREF+}max \le I_{VREF+} \le I_{VREF+}min$	V_{CC} = 3 V	2.4	2.5	2.6	V
		REF2_5V = 0 for 1.5 V $I_{VREF+}max \le I_{VREF+} \le I_{VREF+}min$	V_{CC} = 2.2 V/3 V	1.44	1.5	1.56	
$AV_{CC(min)}$	AV_{CC} minimum voltage, Positive built-in reference active	REF2_5V = 0, $I_{VREF+}max \le I_{VREF+} \le I_{VREF+}min$		2.2			V
		REF2_5V = 1, $I_{VREF+}min \ge I_{VREF+} \ge -0.5mA$		2.8			
		REF2_5V = 1, $I_{VREF+}min \ge I_{VREF+} \ge -1mA$		2.9			
I_{VREF+}	Load current out of V_{REF+} terminal		V_{CC} = 2.2 V	0.01		−0.5	mA
			V_{CC} = 3 V	0.01		−1	
$I_{L(VREF)+}$ †	Load-current regulation V_{REF+} terminal	I_{VREF+} = 500 µA +/− 100 µA Analog input voltage ~0.75 V; REF2_5V = 0	V_{CC} = 2.2 V			±2	LSB
			V_{CC} = 3 V			±2	
		I_{VREF+} = 500 µA ± 100 µA Analog input voltage ~1.25 V; REF2_5V = 1	V_{CC} = 3 V			±2	LSB
$I_{DL(VREF)+}$ ‡	Load current regulation V_{REF+} terminal	I_{VREF+} =100 µA → 900 µA, C_{VREF+}=5 µF, ax ~0.5 x V_{REF+} Error of conversion result ≤ 1 LSB	V_{CC} = 3 V			20	ns
C_{VREF+}	Capacitance at pin V_{REF+} (see Note 1)	REFON =1, 0 mA ≤ I_{VREF+} ≤ I_{VREF+}max	V_{CC} = 2.2 V/3 V	5	10		µF
T_{REF+}†	Temperature coefficient of built-in reference	I_{VREF+} is a constant in the range of 0 mA ≤ I_{VREF+} ≤ 1 mA	V_{CC} = 2.2 V/3 V			±100	ppm/°C
t_{REFON}†	Settle time of internal reference voltage (see Figure 18 and Note 2)	I_{VREF+} = 0.5 mA, C_{VREF+} = 10 µF, V_{REF+} = 1.5 V, V_{AVCC} = 2.2 V				17	ms

† Not production tested, limits characterized
‡ Not production tested, limits verified by design

NOTES: 1. The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests uses two capacitors between pins V_{REF+} and AV_{SS} and V_{REF-}/V_{eREF-} and AV_{SS}: 10 µF tantalum and 100 nF ceramic.
2. The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load.

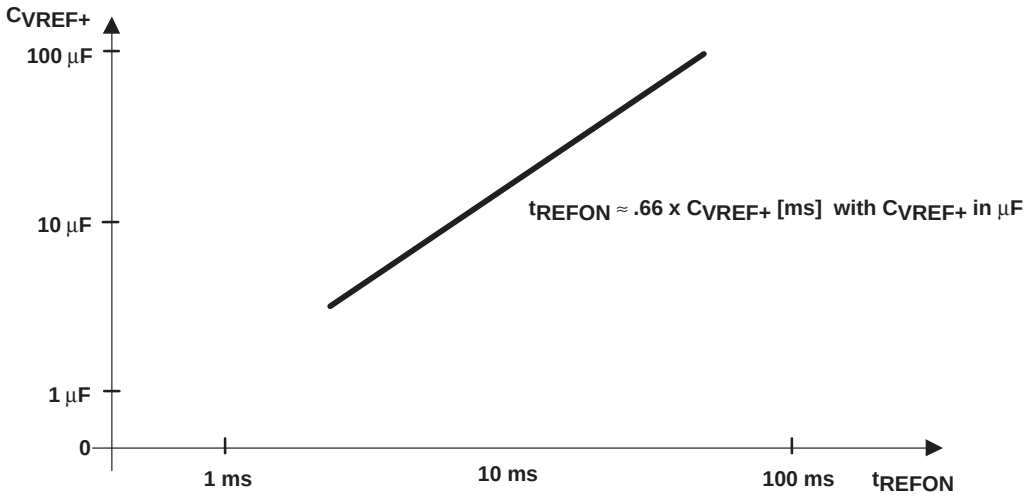


Figure 18. Typical Settling Time of Internal Reference t_{REFON} vs External Capacitor on V_{REF+}

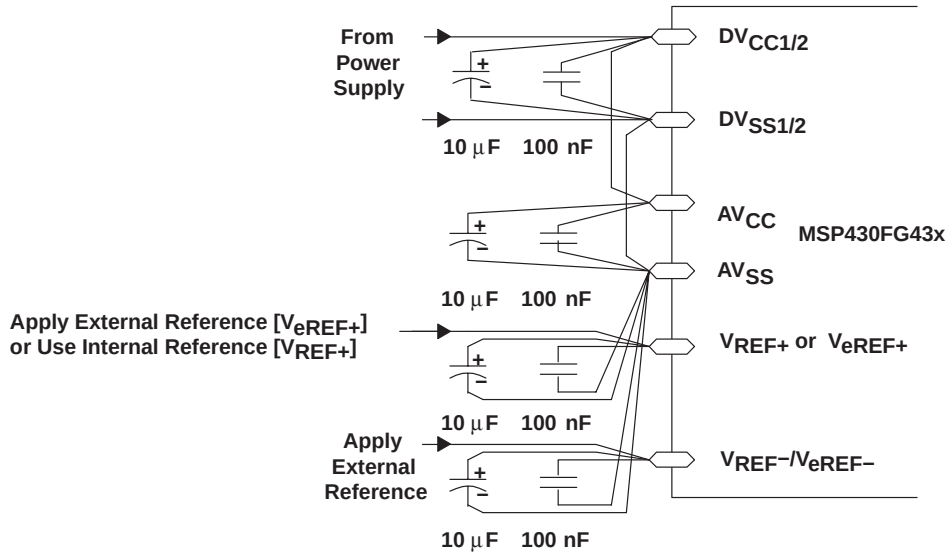


Figure 19. Supply Voltage and Reference Voltage Design V_{REF-}/V_{eREF-} External Supply

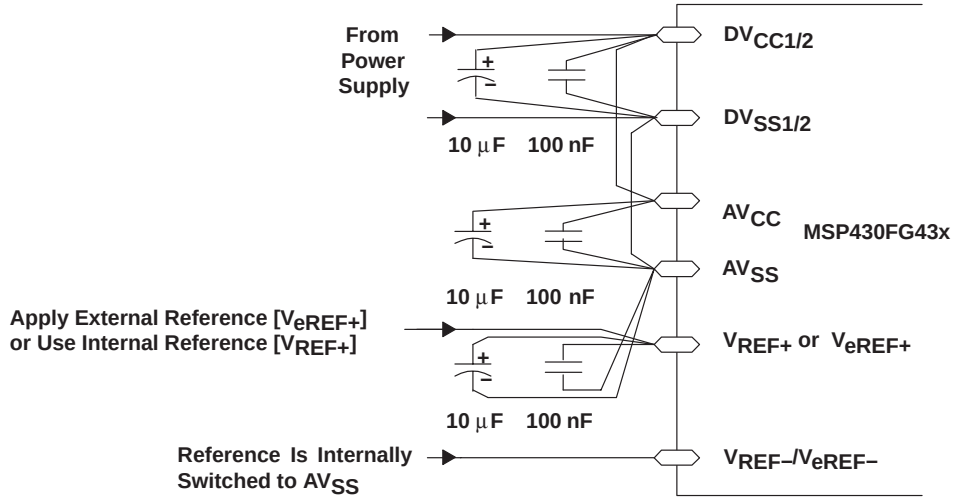


Figure 20. Supply Voltage and Reference Voltage Design V_{REF-}/V_{eREF-} = AV_{SS}, Internally Connected

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, timing parameters

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$f_{ADC12CLK}$		For specified performance of ADC12 linearity parameters	V_{CC} = 2.2V/3 V	0.45	5	6.3	MHz
$f_{ADC12OSC}$	Internal ADC12 oscillator	ADC12DIV=0, $f_{ADC12CLK}=f_{ADC12OSC}$	V_{CC} = 2.2 V/ 3 V	3.7	5	6.3	MHz
$t_{CONVERT}$	Conversion time	$C_{VREF+} \geq 5$ µF, Internal oscillator, $f_{ADC12OSC}$ = 3.7 MHz to 6.3 MHz	V_{CC} = 2.2 V/ 3 V	2.06		3.51	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK or SMCLK: ADC12SSEL ≠ 0		13×ADC12DIV× $1/f_{ADC12CLK}$			µs
$t_{ADC12ON}$‡	Turn on settling time of the ADC	(see Note 1)				100	ns
t_{Sample}‡	Sampling time	R_S = 400 Ω, R_I = 1000 Ω, C_I = 30 pF, τ = [R_S + R_I] x C_I (see Note 2)	V_{CC} = 3 V	1220			ns
			V_{CC} = 2.2 V	1400			

† Not production tested, limits characterized
‡ Not production tested, limits verified by design

NOTES: 1. The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
2. Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns where n = ADC resolution = 12, R_S = external source resistance.

12-bit ADC, linearity parameters

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
E_I	Integral linearity error	1.4 V ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}) min ≤ 1.6 V	V_{CC} = 2.2 V/3 V			±2	LSB
		1.6 V < (V_{eREF+} − V_{REF-}/V_{eREF-}) min ≤ [V_{AVCC}]				±1.7	
E_D	Differential linearity error	(V_{eREF+} − V_{REF-}/V_{eREF-})$_{min}$ ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	V_{CC} = 2.2 V/3 V			±1	LSB
E_O	Offset error	(V_{eREF+} − V_{REF-}/V_{eREF-})$_{min}$ ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}), Internal impedance of source R_S < 100 Ω, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	V_{CC} = 2.2 V/3 V		±2	±4	LSB
E_G	Gain error	(V_{eREF+} − V_{REF-}/V_{eREF-})$_{min}$ ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	V_{CC} = 2.2 V/3 V		±1.1	±2	LSB
E_T	Total unadjusted error	(V_{eREF+} − V_{REF-}/V_{eREF-})$_{min}$ ≤ (V_{eREF+} − V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	V_{CC} = 2.2 V/3 V		±2	±5	LSB

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, temperature sensor and built-in V_{MID}

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
I_{SENSOR}	Operating supply current into AV_{CC} terminal (see Note 1)	REFON = 0, INCH = 0Ah, ADC12ON=NA, T_A = 25°C	2.2 V		40	120	µA
			3 V		60	160	
V_{SENSOR}†	(see Note 2)	ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V/ 3 V		986		mV
TC_{SENSOR}†		ADC12ON = 1, INCH = 0Ah	2.2 V/ 3 V		3.55±3%		mV/°C
$t_{SENSOR(sample)}$†	Sample time required if channel 10 is selected (see Note 3)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30			µs
			3 V	30			
I_{VMID}	Current into divider at channel 11 (see Note 4)	ADC12ON = 1, INCH = 0Bh,	2.2 V			NA	µA
			3 V			NA	
V_{MID}	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, V_{MID} is ~0.5 x V_{AVCC}	2.2 V		1.1	1.1±0.04	V
			3 V		1.5	1.50±0.04	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (see Note 5)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1400			ns
			3 V	1220			

† Not production tested, limits characterized

NOTES:
1. The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and REFON=1), or (ADC12ON=1 AND INCH=0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is already included in I_{REF+}.
2. The temperature sensor offset can be as much as ±20°C. A single-point calibration is recommended in order to minimize the offset error of the built-in temperature sensor.
3. The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$
4. No additional current is needed. The V_{MID} is used during sampling.
5. The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

12-bit DAC, supply specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} = DV_{CC}, AV_{SS} = DV_{SS} =0 V		2.20		3.60	V
I_{DD}	Supply Current: Single DAC Channel (see Notes 1 and 2)	DAC12AMPx=2, DAC12IR=0, DAC12_xDAT=0800h	2.2V/3V		50	110	µA
		DAC12AMPx=2, DAC12IR=1, DAC12_xDAT=0800h , V_{eREF+}=V_{REF+}= AV_{CC}	2.2V/3V		50	110	
		DAC12AMPx=5, DAC12IR=1, DAC12_xDAT=0800h, V_{eREF+}=V_{REF+}= AV_{CC}	2.2V/3V		200	440	
		DAC12AMPx=7, DAC12IR=1, DAC12_xDAT=0800h, V_{eREF+}=V_{REF+}= AV_{CC}	2.2V/3V		700	1500	
PSRR	Power supply rejection ratio (see Notes 3 and 4)	DAC12_xDAT = 800h, V_{REF} = 1.5 V ΔAV_{CC} = 100mV	2.2V		70		dB
		DAC12_xDAT = 800h, V_{REF} = 1.5 V or 2.5 V ΔAV_{CC} = 100mV	3V				

NOTES:
1. No load at the output pin, DAC12_0 or DAC12_1, assuming that the control bits for the shared pins are set properly.
2. Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications.
3. PSRR = 20*log{$\Delta AV_{CC}/\Delta V_{DAC12\_xOUT}$}.
4. V_{REF} is applied externally. The internal reference is not used.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, linearity specifications (see Figure 21)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Resolution		(12-bit Monotonic)		12			bits
INL	Integral nonlinearity (see Note 1)	V_{ref} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2V		±2.0	±8.0	LSB
		V_{ref} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3V				
DNL	Differential nonlinearity (see Note 1)	V_{ref} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2V		±0.4	±1.0	LSB
		V_{ref} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3V				
E_O	Offset voltage w/o calibration (see Notes 1, 2)	V_{ref} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2V			±21	mV
		V_{ref} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3V				
	Offset voltage with calibration (see Notes 1, 2)	V_{ref} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2V			±2.5	
		V_{ref} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3V				
$d_{E(O)}/d_T$	Offset error temperature coefficient (see Note 1)		2.2V/3V		±30		µV/C
E_G	Gain error (see Note 1)	V_{REF} = 1.5 V	2.2V			±3.50	% FSR
		V_{REF} = 2.5 V	3V				
$d_{E(G)}/d_T$	Gain temperature coefficient (see Note 1)		2.2V/3V		10		ppm of FSR/°C
t_{Offset_Cal}	Time for offset calibration (see Note 3)	DAC12AMPx=2	2.2V/3V			100	ms
		DAC12AMPx=3,5	2.2V/3V			32	
		DAC12AMPx=4,6,7	2.2V/3V			6	

NOTES: 1. Parameters calculated from the best-fit curve from 0x0A to 0xFFF. The best-fit curve method is used to deliver coefficients “a” and “b” of the first order equation: y = a + b*x. $V_{DAC12\_xOUT} = E_O + (1 + E_G) * (V_{eREF+}/4095) * DAC12\_xDAT$, DAC12IR = 1.
2. The offset calibration works on the output operational amplifier. Offset Calibration is triggered setting bit DAC12CALON
3. The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx ={0, 1}. It is recommended that the DAC12 module be configured prior to initiating calibration. Port activity during calibration may effect accuracy and is not recommended.

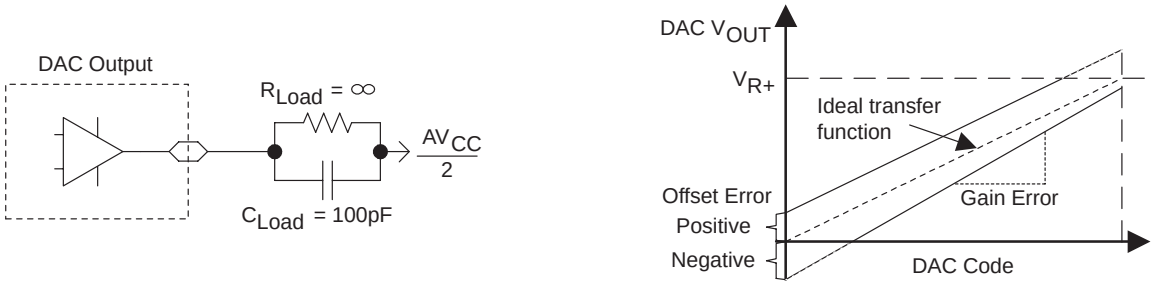
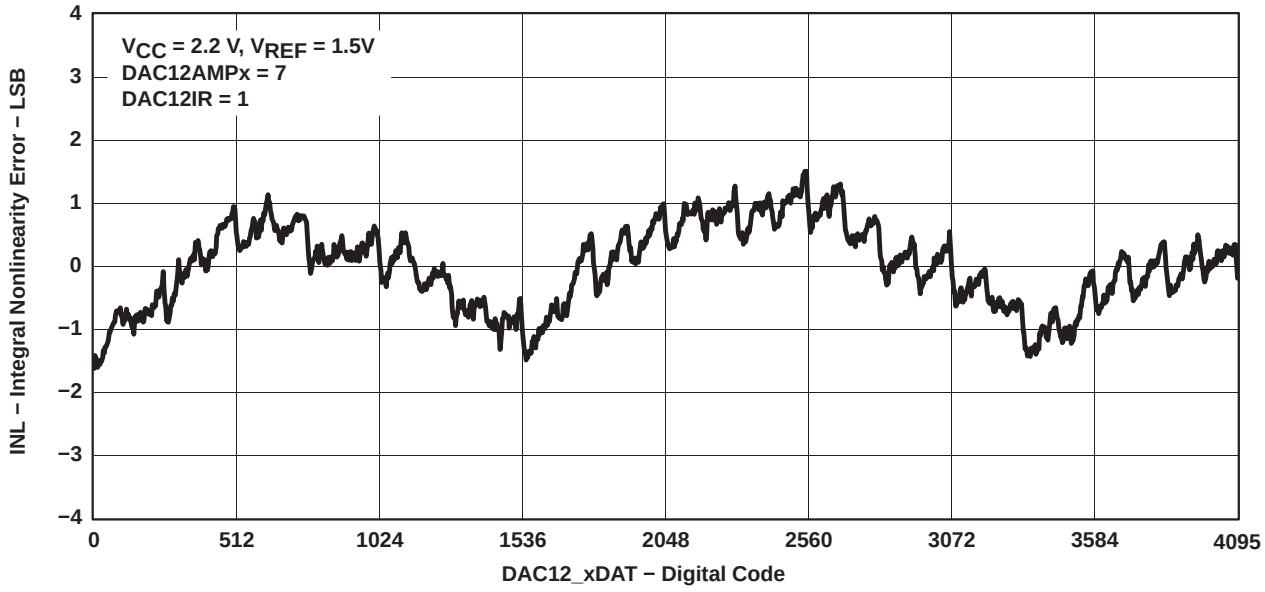


Figure 21. Linearity Test Load Conditions and Gain/Offset Definition

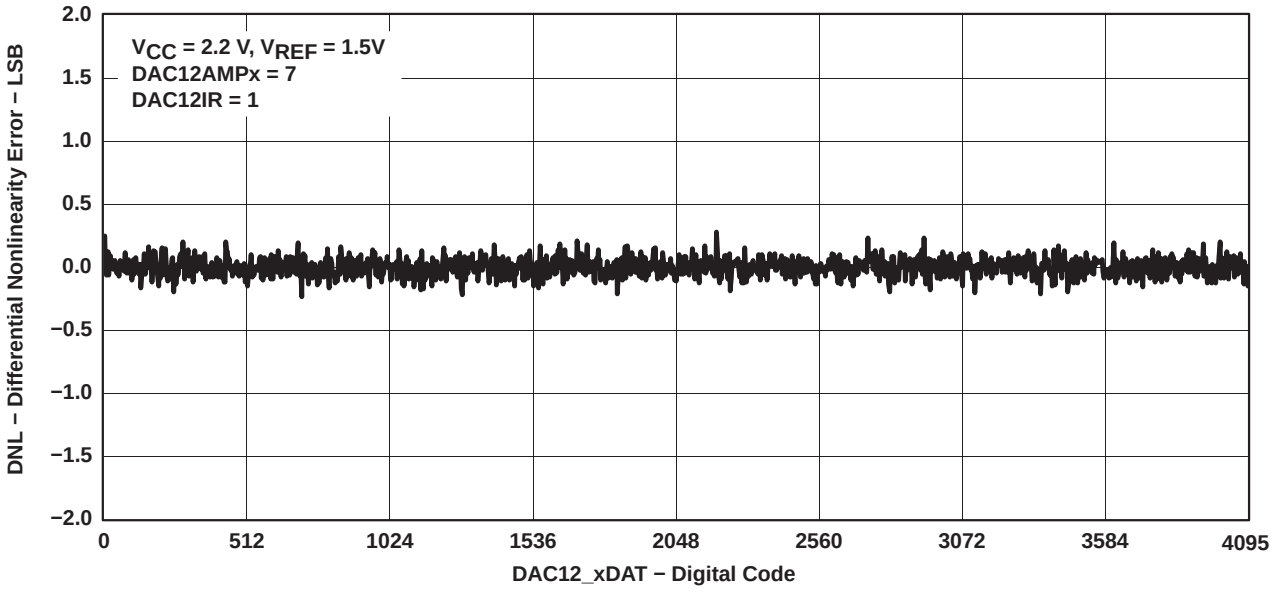
electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, linearity specifications (continued)

TYPICAL INL ERROR
vs
DIGITAL INPUT DATA



TYPICAL DNL ERROR
vs
DIGITAL INPUT DATA



electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, output specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_O	Output voltage range (see Note 1, Figure 24)	No Load, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2V/3V	0		0.005	V
		No Load, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7	2.2V/3V	AV_{CC}−0.05		AV_{CC}	
		R_{Load}= 3 kΩ, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2V/3V	0		0.1	
		R_{Load}= 3 kΩ, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7	2.2V/3V	AV_{CC}−0.13		AV_{CC}	
$C_{L(DAC12)}$	Max DAC12 load capacitance		2.2V/3V			100	pF
$I_{L(DAC12)}$	Max DAC12 load current		2.2V	−0.5		+0.5	mA
			3V	−1.0		+1.0	
$R_{O/P(DAC12)}$	Output Resistance (see Figure 24)	R_{Load}= 3 kΩ, $V_{O/P(DAC12)}$ < 0.3 V, DAC12AMPx = 7, DAC12_xDAT = 0h	2.2V/3V		150	250	Ω
		R_{Load}= 3 kΩ, $V_{O/P(DAC12)} > AV_{CC}$−0.3 V DAC12AMPx = 7, DAC12_xDAT = 0FFFh	2.2V/3V		150	250	
		R_{Load}= 3 kΩ, 0.3V ≤ $V_{O/P(DAC12)}$ ≤ AV_{CC} − 0.3V DAC12AMPx = 7	2.2V/3V		1	4	

NOTES: 1. Data is valid after the offset calibration of the output amplifier.

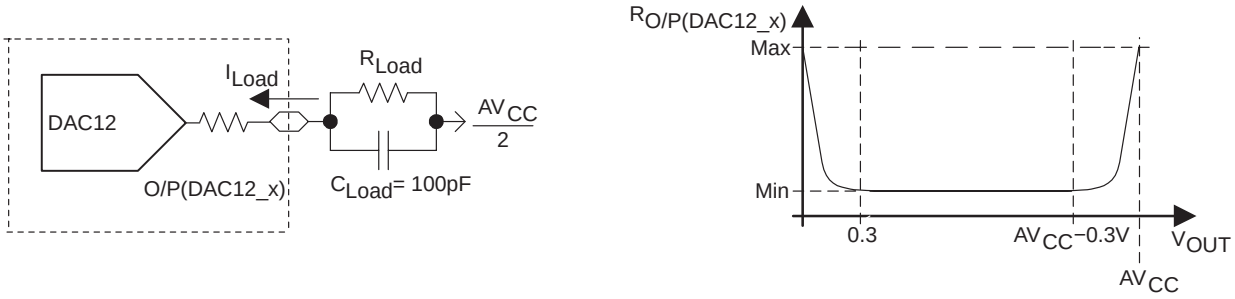


Figure 24. DAC12_x Output Resistance Tests

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

12-bit DAC, reference input specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Ve_{REF+}	Reference input voltage range	DAC12IR=0, (see Notes 1 and 2)	2.2V/3V		$AV_{CC}/3$	AV_{CC}+0.2	V
		DAC12IR=1, (see Notes 3 and 4)	2.2V/3V		AVcc	AVcc+0.2	
$Ri_{(VREF+)}$, $Ri_{(VeREF+)}$	Reference input resistance	DAC12_0 IR=DAC12_1 IR =0	2.2V/3V	20			MΩ
		DAC12_0 IR=1, DAC12_1 IR = 0	2.2V/3V	40	48	56	kΩ
		DAC12_0 IR=0, DAC12_1 IR = 1	2.2V/3V				
		DAC12_0 IR=DAC12_1 IR =1 DAC12_0 SREFx = DAC12_1 SREFx (see Note 5)	2.2V/3V	20	24	28	kΩ

NOTES: 1. For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AV_{CC}).
2. The maximum voltage applied at reference input voltage terminal $Ve_{REF+} = [AV_{CC} - V_{E(O)}] / [3*(1 + E_G)]$.
3. For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AV_{CC}).
4. The maximum voltage applied at reference input voltage terminal $Ve_{REF+} = [AV_{CC} - V_{E(O)}] / (1 + E_G)$.
5. When DAC12IR = 1 and DAC12SREFx = 0 or 1 for both channels, the reference input resistive dividers for each DAC are in parallel reducing the reference input resistance.

12-bit DAC, dynamic specifications; $V_{ref} = V_{CC}$, DAC12IR = 1 (see Figure 25 and Figure 26)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
t_{ON}	DAC12 on-time	DAC12_xDAT = 800h, $Error_{V(O)}$ < ±0.5 LSB (see Note 1,Figure 25)	DAC12AMPx=0 → {2, 3, 4}	2.2V/3V		60	120	µs
			DAC12AMPx=0 → {5, 6}	2.2V/3V		15	30	
			DAC12AMPx=0 → 7	2.2V/3V		6	12	
$t_{S(FS)}$	Settling time,full-scale	DAC12_xDAT = 80h→ F7Fh→ 80h	DAC12AMPx=2	2.2V/3V		100	200	µs
			DAC12AMPx=3,5	2.2V/3V		40	80	
			DAC12AMPx=4,6,7	2.2V/3V		15	30	
$t_{S(C-C)}$	Settling time, code to code	DAC12_xDAT = 3F8h→ 408h→ 3F8h BF8h→ C08h→ BF8h	DAC12AMPx=2	2.2V/3V		5		µs
			DAC12AMPx=3,5	2.2V/3V		2		
			DAC12AMPx=4,6,7	2.2V/3V		1		
SR	Slew Rate	DAC12_xDAT = 80h→ F7Fh→ 80h	DAC12AMPx=2	2.2V/3V	0.05	0.12		V/µs
			DAC12AMPx=3,5	2.2V/3V	0.35	0.7		
			DAC12AMPx=4,6,7	2.2V/3V	1.5	2.7		
Glitch energy: full-scale		DAC12_xDAT = 80h→ F7Fh→ 80h	DAC12AMPx=2	2.2V/3V		10		nV-s
			DAC12AMPx=3,5	2.2V/3V		10		
			DAC12AMPx=4,6,7	2.2V/3V		10		

NOTES: 1. R_{Load} and C_{Load} connected to AV_{SS} (not $AV_{CC}/2$) in Figure 25.
2. Slew rate applies to output voltage steps >= 200mV.

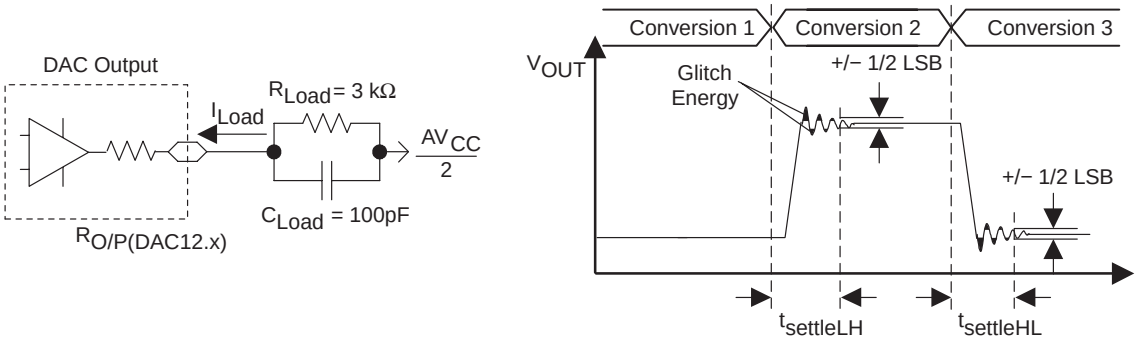


Figure 25. Settling Time and Glitch Energy Testing

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

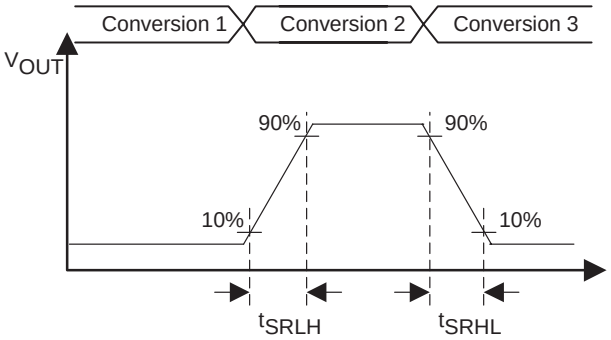


Figure 26. Slew Rate Testing

12-bit DAC, dynamic specifications continued (T_A = 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
BW_{-3dB}	3-dB bandwidth, V_{DC}=1.5V, V_{AC}=0.1V_{PP} (see Figure 27)	DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2V/3V	40			kHz
		DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2V/3V	180			
		DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2V/3V	550			
Channel-to-channel crosstalk (see Note 1 and Figure 28)		DAC12_0DAT = 800h, No Load, DAC12_1DAT = 80h<−>F7Fh, R_{Load} = 3kΩ f_{DAC12_1OUT} = 10kHz @ 50/50 duty cycle	2.2V/3V		−80		dB
		DAC12_0DAT = 80h<−>F7Fh, R_{Load} = 3kΩ, DAC12_1DAT = 800h, No Load f_{DAC12_0OUT} = 10kHz @ 50/50 duty cycle	2.2V/3V		−80		

NOTES: 1. R_{LOAD} = 3 kΩ, C_{LOAD} = 100 pF

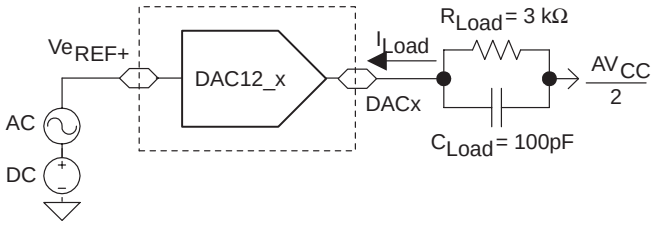


Figure 27. Test Conditions for 3-dB Bandwidth Specification

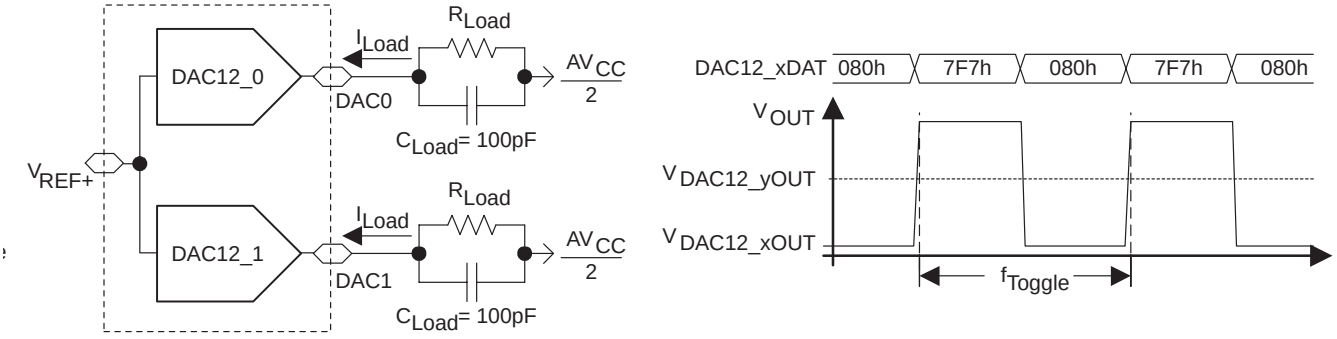


Figure 28. Crosstalk Test Conditions

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

operational amplifier OA, supply specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		—	2.2		3.6	V
I_{CC}	Supply current (see Note 1)	Fast Mode, RRIP OFF	2.2 V/3 V		180	290	µA
		Medium Mode, RRIP OFF	2.2 V/3 V		110	190	
		Slow Mode, RRIP OFF	2.2 V/3 V		50	80	
		Fast Mode, RRIP ON	2.2 V/3 V		300	490	
		Medium Mode, RRIP ON	2.2 V/3 V		190	350	
		Slow Mode, RRIP ON	2.2 V/3 V		90	190	
PSRR	Power supply rejection ratio	Non-inverting	2.2 V/3 V		70		dB

NOTES: 1. P6SEL.x = 1 for each corresponding pin when used in OA input or OA output mode.

operational amplifier OA, input/output specifications

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$V_{I/P}$	Voltage supply, I/P	RRIP OFF		—	−0.1		V_{CC}−1.2	V
		RRIP ON		—	−0.1		V_{CC}+0.1	V
I_{Ikg}	Input leakage current, I/P (see Notes 1 and 2)	T_A = −40 to +55°C		—	−5	±0.5	5	nA
		T_A = +55 to +85°C		—	−20	±5	20	nA
V_n	Voltage noise density, I/P	Fast Mode	$f_{V(I/P)}$ = 1 kHz	—		50		nV/√Hz
		Medium Mode		—		80		
		Slow Mode		—		140		
		Fast Mode	$f_{V(I/P)}$ = 10 kHz	—		30		
		Medium Mode		—		50		
		Slow Mode		—		65		
V_{IO}	Offset voltage, I/P			2.2 V/3 V			±10	mV
	Offset temperature drift, I/P	see Note 3		2.2 V/3 V		±10		µV/°C
	Offset voltage drift with supply, I/P	0.3V ≤ V_{IN} ≤ V_{CC}−0.3V ΔV_{CC}≤ ± 10%, T_A = 25°C		2.2 V/3 V			±1.5	mV/V
V_{OH}	High-level output voltage, O/P	Fast Mode, I_{SOURCE} ≤ −500µA		2.2 V	V_{CC}−0.2		V_{CC}	V
		Slow Mode,I_{SOURCE} ≤ −150µA		3 V	V_{CC}−0.1		V_{CC}	
V_{OL}	Low-level output voltage, O/P	Fast Mode, I_{SOURCE} ≤ +500µA		2.2 V	V_{SS}		0.2	V
		Slow Mode,I_{SOURCE} ≤ +150µA		3 V	V_{SS}		0.1	
$R_{O/P}$ (OAx)	Output Resistance (see Figure 29 and Note 4)	R_{Load}= 3 kΩ, C_{Load} = 50pF, RRIP ON, $V_{O/P(OAx)}$ < 0.2 V		2.2 V/3 V		150	250	Ω
		R_{Load}= 3 kΩ, C_{Load} = 50pF, RRIP ON, $V_{O/P(OAx)}$ > AV_{CC} − 0.2 V		2.2 V/3 V		150	250	
		R_{Load}= 3 kΩ, C_{Load} = 50pF, RRIP ON, 0.2 V ≤ $V_{O/P(OAx)}$ ≤ AV_{CC} − 0.2 V		2.2 V/3 V		0.1	4	
CMRR	Common-mode rejection ratio	Non-inverting		2.2 V/3 V		70		dB

NOTES: 1. ESD damage can degrade input current leakage.
2. The input bias current is overridden by the input leakage current.
3. Characterized and calculated using the box method, not production tested.
4. Specification valid for voltage-follower OAx configuration.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

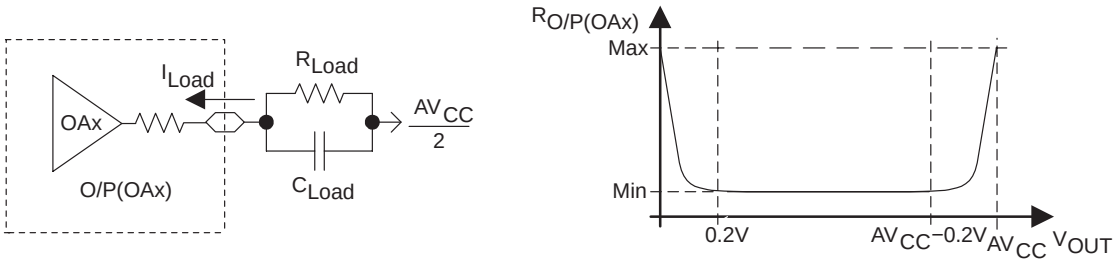


Figure 29. OAx Output Resistance Tests

operational amplifier OA, dynamic specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
SR	Slew rate	Fast Mode	—		1.2		V/µs
		Medium Mode	—		0.8		
		Slow Mode	—		0.3		
	Open-loop voltage gain		—		100		dB
ϕ_m	Phase margin	C_L = 50 pF	—		60		deg
	Gain margin	C_L = 50 pF	—		20		dB
GBW	Gain-Bandwidth Product (see Figure 30 and Figure 31)	Non−inverting, Fast Mode, R_L = 47kΩ, C_L = 50pF	2.2 V/3 V		2.2		MHz
		Non−inverting, Medium Mode, R_L =300kΩ, C_L = 50pF	2.2 V/3 V		1.4		
		Non−inverting, Slow Mode, R_L =300kΩ, C_L = 50pF	2.2 V/3 V		0.5		
$t_{en(on)}$	Enable time on	t_{on}, non-inverting, Gain = 1	2.2 V/3 V		10	20	µs
$t_{en(off)}$	Enable time off		2.2 V/3 V			1	µs

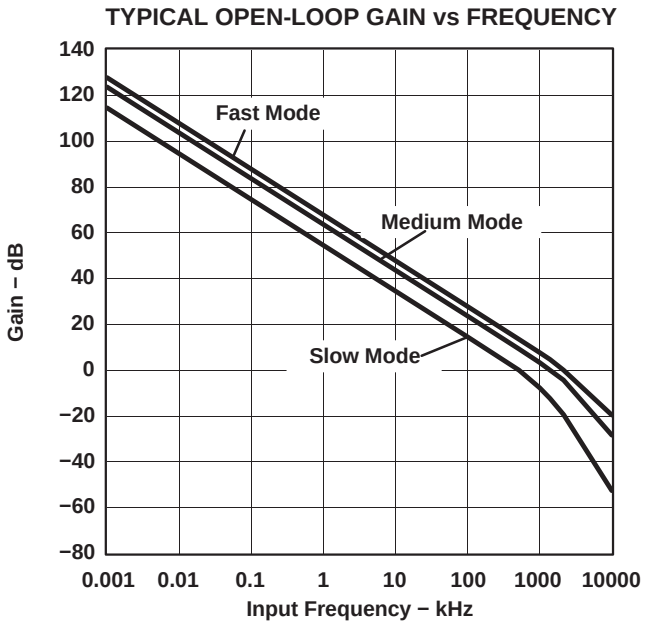


Figure 30

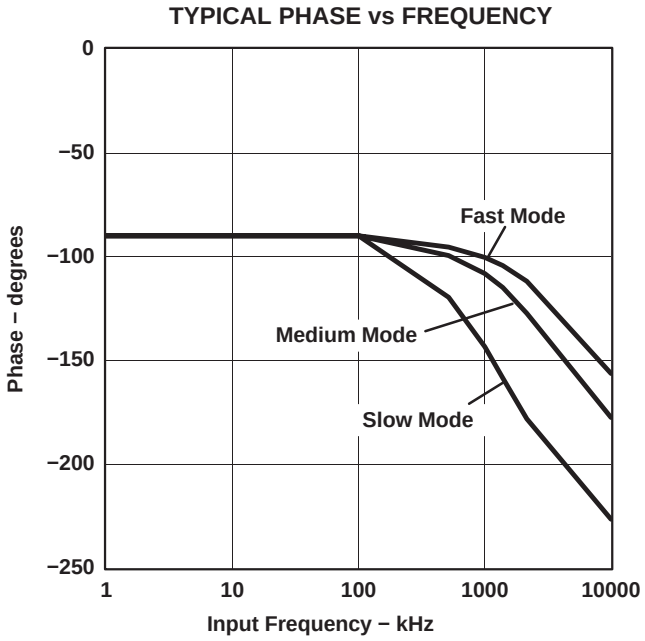


Figure 31

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

Flash Memory

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and Erase supply voltage			2.7		3.6	V
f_{FTG}	Flash Timing Generator frequency			257		476	kHz
I_{PGM}	Supply current from DV_{CC} during program		2.7 V/ 3.6 V		3	5	mA
I_{ERASE}	Supply current from DV_{CC} during erase		2.7 V/ 3.6 V		3	7	mA
t_{CPT}	Cumulative program time	see Note 1	2.7 V/ 3.6 V			4	ms
$t_{CMErase}$	Cumulative mass erase time	see Note 2	2.7 V/ 3.6 V	200			ms
	Program/Erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	see Note 3			35		t_{FTG}
$t_{Block, 0}$	Block program time for 1st byte or word				30		
$t_{Block, 1-63}$	Block program time for each additional byte or word				21		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time				5297		
$t_{Seg Erase}$	Segment erase time				4819		

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. The mass erase duration generated by the flash timing generator is at least 11.1ms (= 5297x1/f_{FTG},max = 5297x1/476kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
3. These values are hardwired into the Flash Controller's state machine (t_{FTG} = 1/f_{FTG}).

JTAG Interface

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
f_{TCK}	TCK input frequency	see Note 1	2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pull-up resistance on TMS, TCK, TDI/TCLK	see Note 2	2.2 V/ 3 V	25	60	90	kΩ

NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.
2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

JTAG Fuse (see Note 1)

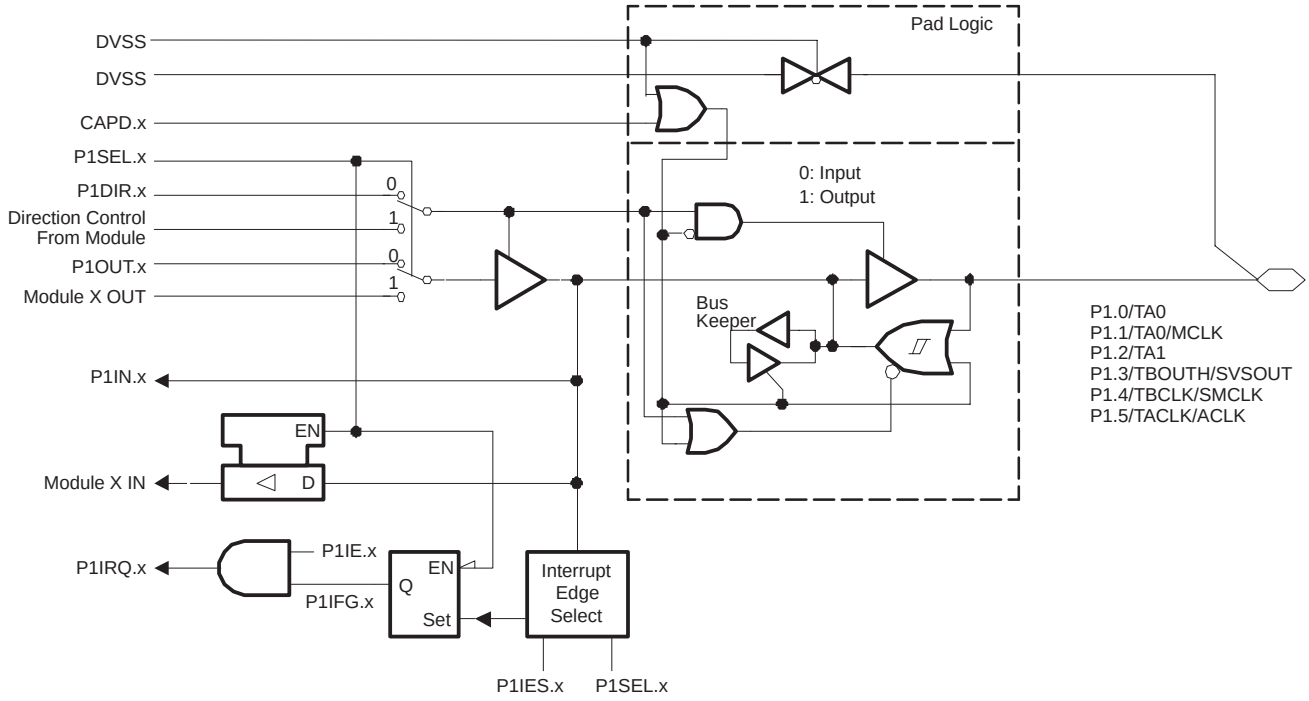
PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C		2.5			V
V_{FB}	Voltage level on TDI/TCLK for fuse-blow: F versions			6		7	V
I_{FB}	Supply current into TDI/TCLK during fuse blow					100	mA
t_{FB}	Time to blow fuse					1	ms

NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

APPLICATION INFORMATION

input/output schematic

Port P1, P1.0 to P1.5, input/output with Schmitt-trigger



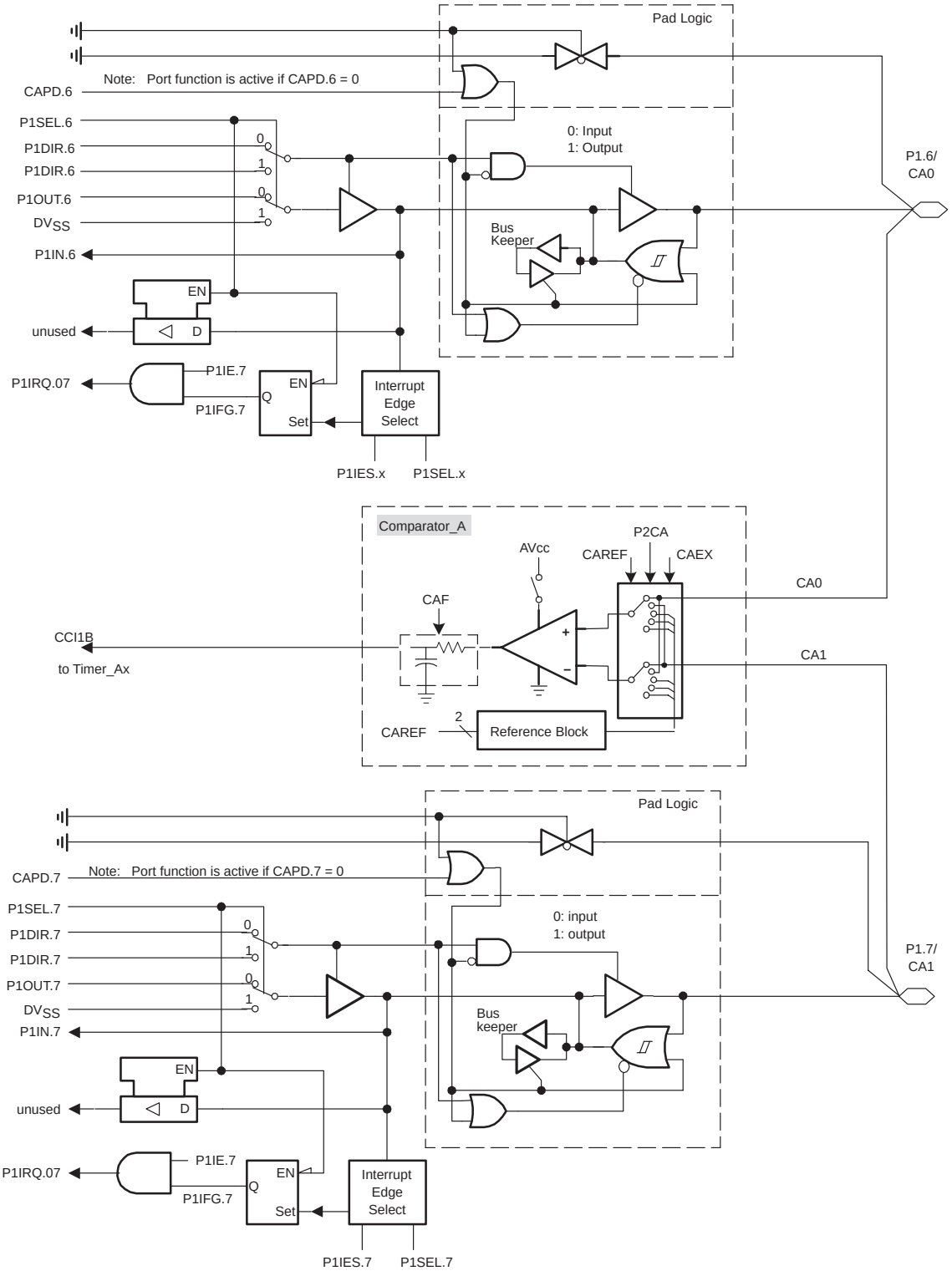
Note: $0 \le x \le 5$
Note: Port function is active if CAPD.x = 0

PnSEL.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P1SEL.0	P1DIR.0	P1DIR.0	P1OUT0	Out0 sig.†	P1IN.0	CCI0A†	P1IE.0	P1IFG.0	P1IES.0
P1SEL.1	P1DIR.1	P1DIR.1	P1OUT.1	MCLK	P1IN.1	CCI0B†	P1IE.1	P1IFG.1	P1IES.1
P1SEL.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 sig.†	P1IN.2	CCI1A†	P1IE.2	P1IFG.2	P1IES.2
P1SEL.3	P1DIR.3	P1DIR.3	P1OUT.3	SVSOUT	P1IN.3	TBOUTH‡	P1IE.3	P1IFG.3	P1IES.3
P1SEL.4	P1DIR.4	P1DIR.4	P1OUT.4	SMCLK	P1IN.4	TBCLK‡	P1IE.4	P1IFG.4	P1IES.4
P1SEL.5	P1DIR.5	P1DIR5	P1OUT.5	ACLK	P1IN.5	TACLK†	P1IE.5	P1IFG.5	P1IES.5

† Timer_A
‡ Timer_B

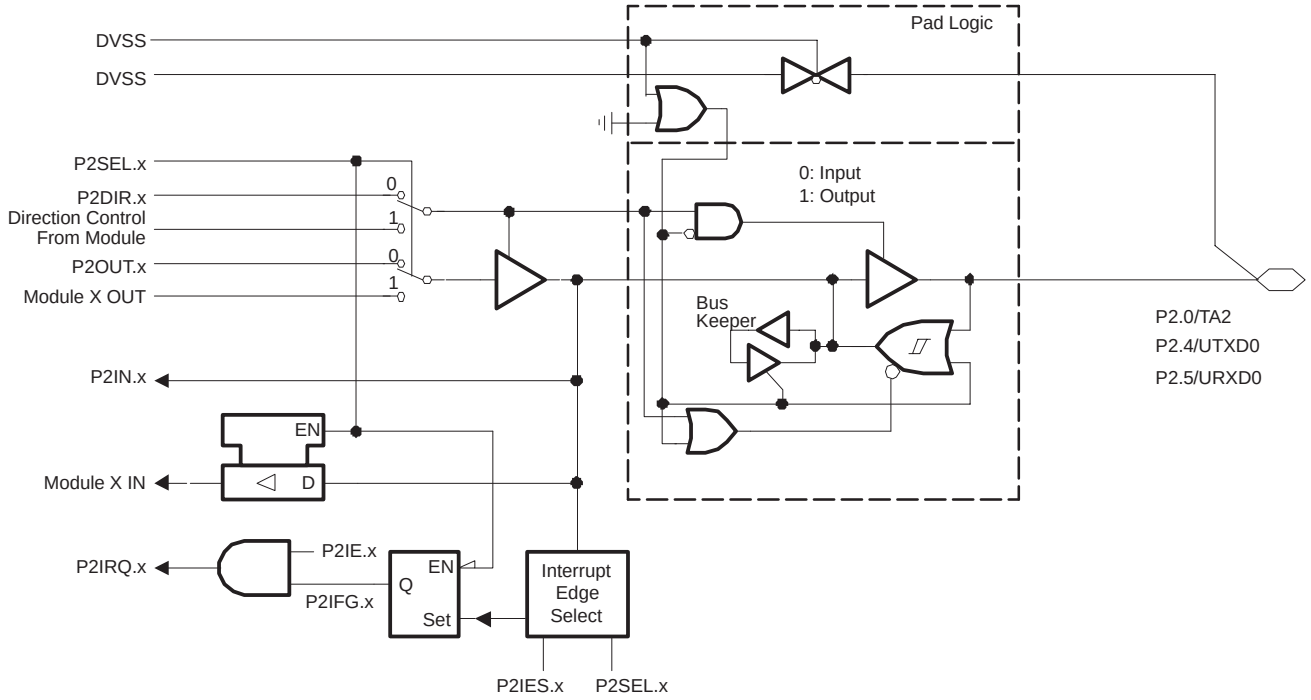
input/output schematic (continued)

Port P1, P1.6, P1.7, input/output with Schmitt-trigger



input/output schematic (continued)

port P2, P2.0, P2.4 to P2.5, input/output with Schmitt-trigger



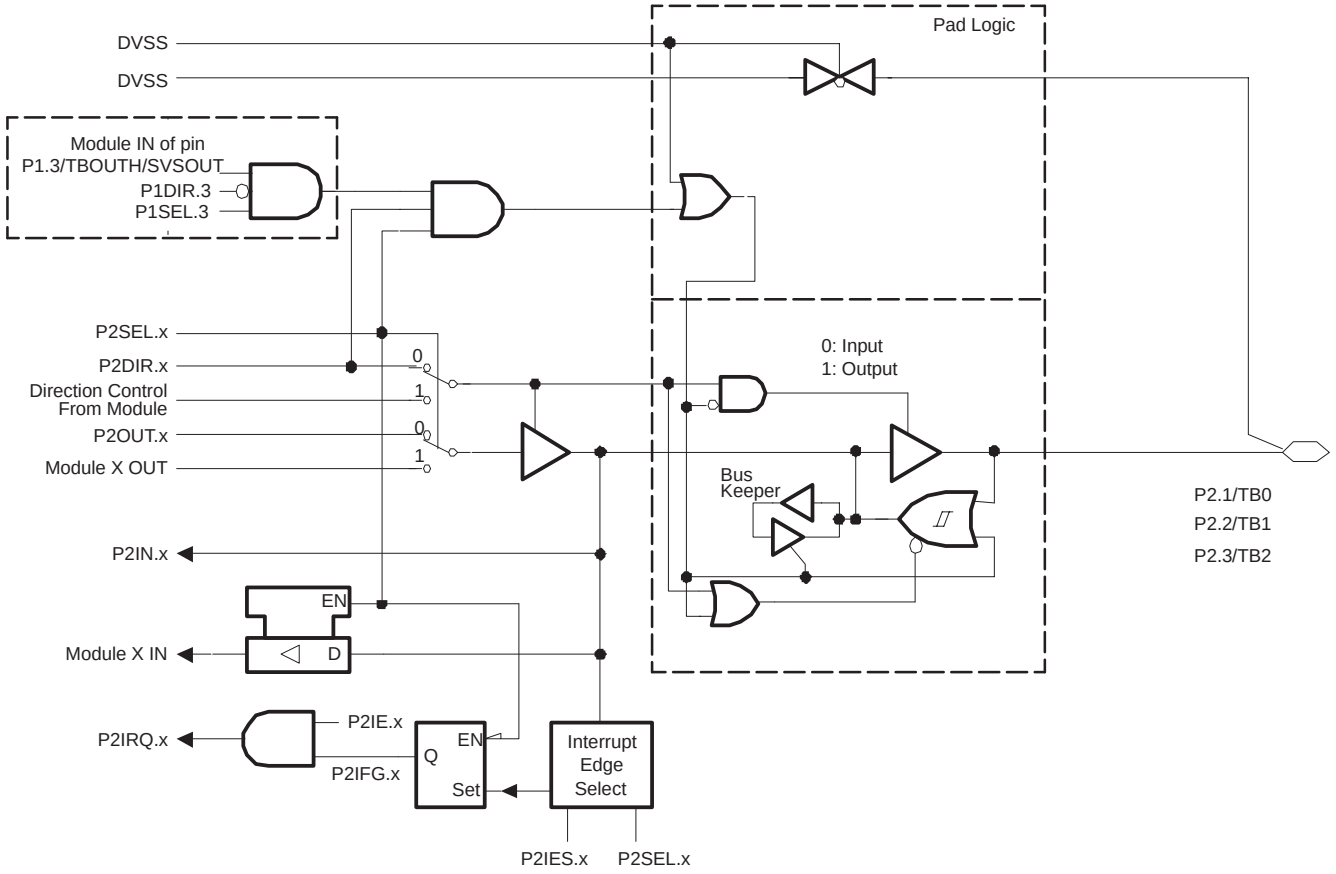
Note: x {0,4,5}

PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	Out2 sig. †	P2IN.0	CCI2A†	P2IE.0	P2IFG.0	P2IES.0
P2Sel.4	P2DIR.4	DVCC	P2OUT.4	UTXD0‡	P2IN.4	unused	P2IE.4	P2IFG.4	P2IES.4
P2Sel.5	P2DIR.5	DVSS	P2OUT.5	DVSS	P2IN.5	URXD0‡	P2IE.5	P2IFG.5	P2IES.5

†Timer_A
‡USART0

input/output schematic (continued)

port P2, P2.1 to P2.3, input/output with Schmitt-trigger



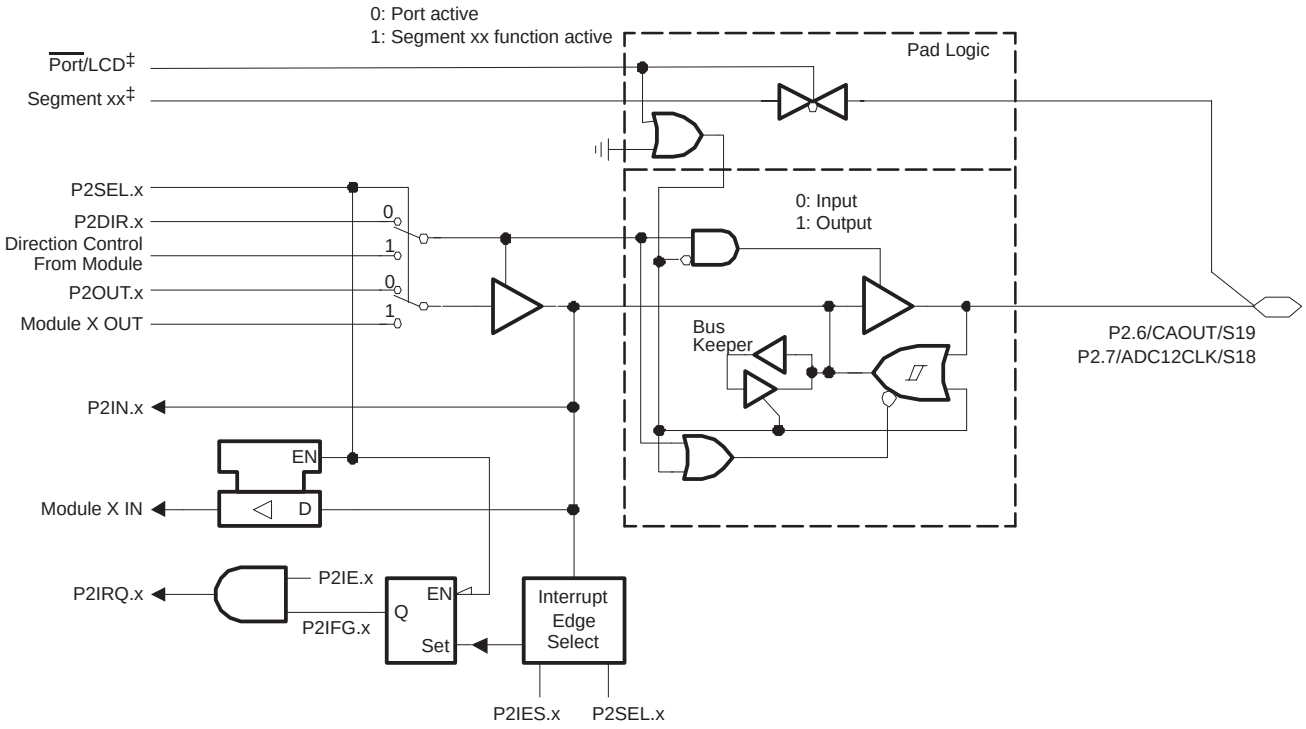
Note: $1 \le x \le 3$

PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.1	P2DIR.1	P2DIR.1	P2OUT.1	Out0 sig. †	P2IN.1	CCI0A † CCI0B	P2IE.1	P2IFG.1	P2IES.1
P2Sel.2	P2DIR.2	P2DIR.2	P2OUT.2	Out1 sig. †	P2IN.2	CCI1A † CCI1B	P2IE.2	P2IFG.2	P2IES.2
P2Sel.3	P2DIR.3	P2DIR.3	P2OUT.3	Out2 sig. †	P2IN.3	CCI2A † CCI2B	P2IE.3	P2IFG.3	P2IES.3

†Timer_B

input/output schematic (continued)

port P2, P2.6 to P2.7, input/output with Schmitt-trigger



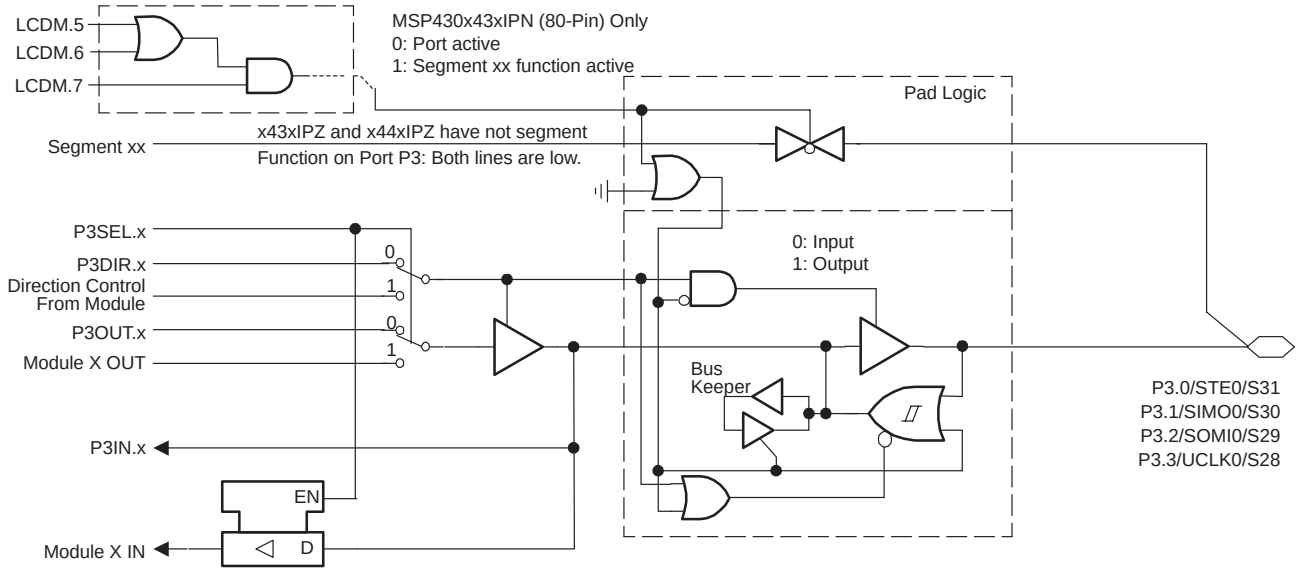
Note: $6 \le x \le 7$

PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x	Port/LCD
P2Sel.6	P2DIR.6	P2DIR.6	P2OUT.6	CAOUT †	P2IN.6	unused	P2IE.6	P2IFG.6	P2IES.6	0: LCDM<40h
P2Sel.7	P2DIR.7	P2DIR.7	P2OUT.7	ADC12CLK§	P2IN.7	unused	P2IE.7	P2IFG.7	P2IES.7	0: LCDM<40h

† Comparator_A
§ ADC12

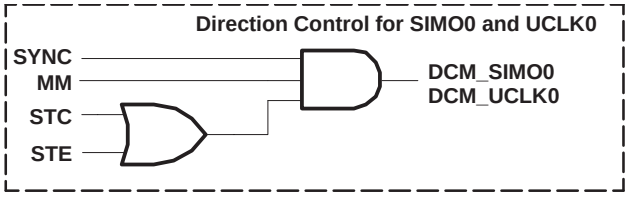
input/output schematic (continued)

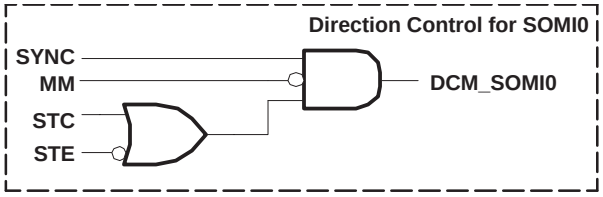
port P3, P3.0 to P3.3, input/output with Schmitt-trigger



Note: $0 \le x \le 3$

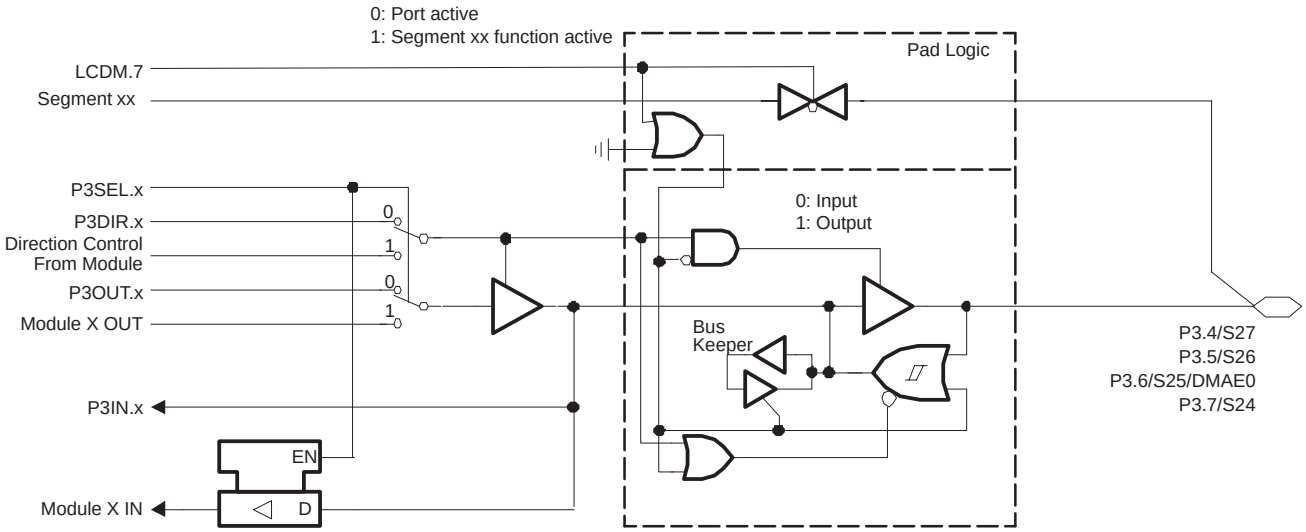
PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P3Sel.0	P3DIR.0	DV_{SS}	P3OUT.0	DV_{SS}	P3IN.0	STE0(in)
P3Sel.1	P3DIR.1	DCM_SIMO0	P3OUT.1	SIMO0(out)	P3IN.1	SIMO0(in)
P3Sel.2	P3DIR.2	DCM_SOMI0	P3OUT.2	SOMIO(out)	P3IN.2	SOMI0(in)
P3Sel.3	P3DIR.3	DCM_UCLK0	P3OUT.3	UCLK0(out)	P3IN.3	UCLK0(in)





input/output schematic (continued)

port P3, P3.4 to P3.7, input/output with Schmitt-trigger

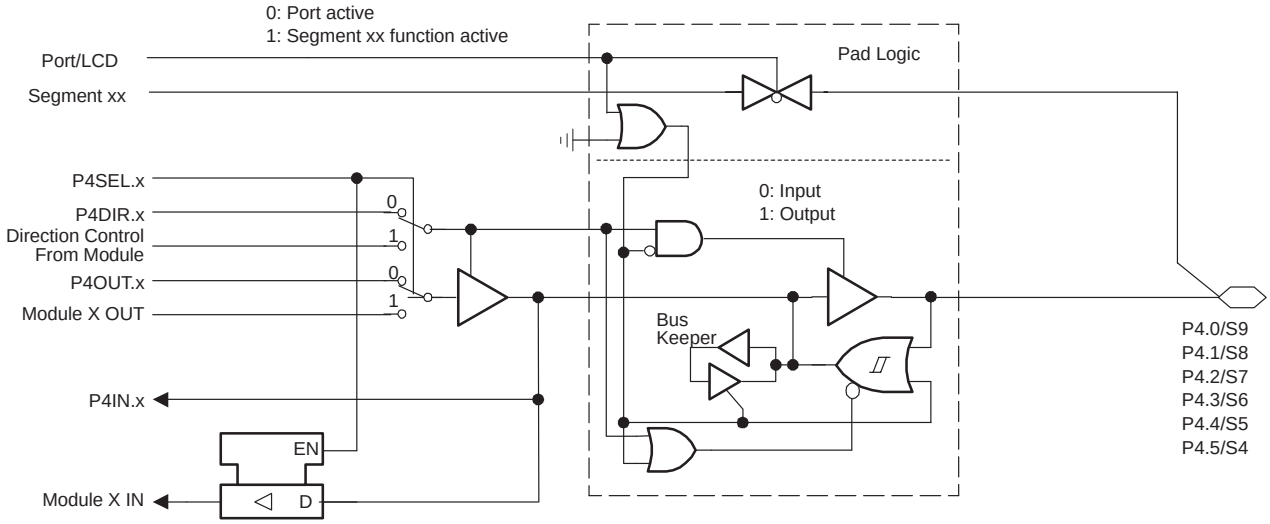


Note: $4 \le x \le 7$

PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P3SEL.4	P3DIR.4	P3DIR.4	P3OUT.4	DVSS	P3IN.4	unused
P3SEL.5	P3DIR.5	P3DIR.5	P3OUT.5	DVSS	P3IN.5	unused
P3SEL.6	P3DIR.6	P3DIR.6	P3OUT.6	DVSS	P3IN.6	DMAE0
P3SEL.7	P3DIR.7	P3DIR.7	P3OUT.7	DVSS	P3IN.7	unused

input/output schematic (continued)

port P4, P4.0 to P4.5, input/output with Schmitt-trigger



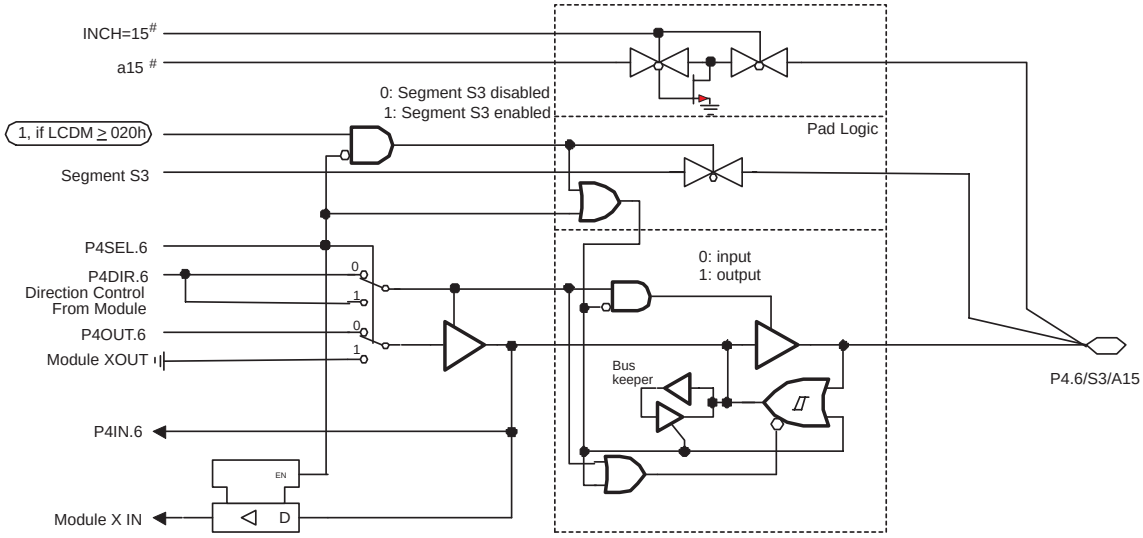
Note: $0 \le x \le 5$

PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P4SEL.0	P4DIR.0	P4DIR.0	P4OUT.0	DVSS	P4IN.0	unused
P4SEL.1	P4DIR.1	P4DIR.1	P4OUT.1	DVSS	P4IN.1	unused
P4SEL.2	P4DIR.2	P4DIR.2	P4OUT.2	DVSS	P4IN.2	unused
P4SEL.3	P4DIR.3	P4DIR.3	P4OUT.3	DVSS	P4IN.3	unused
P4SEL.4	P4DIR.4	P4DIR.4	P4OUT.4	DVSS	P4IN.4	unused
P4SEL.5	P4DIR.5	P4DIR.5	P4OUT.5	DVSS	P4IN.5	unused

DEVICE	PORT BITS	PORT FUNCTION	LCD SEG. FUNCTION
xG43xIPN 80-pin QFP	P4.0 to P4.5	LCDM < 020h	LVDM ≥ 020h

input/output schematic (continued)

port P4, P4.6, input/output with Schmitt-trigger



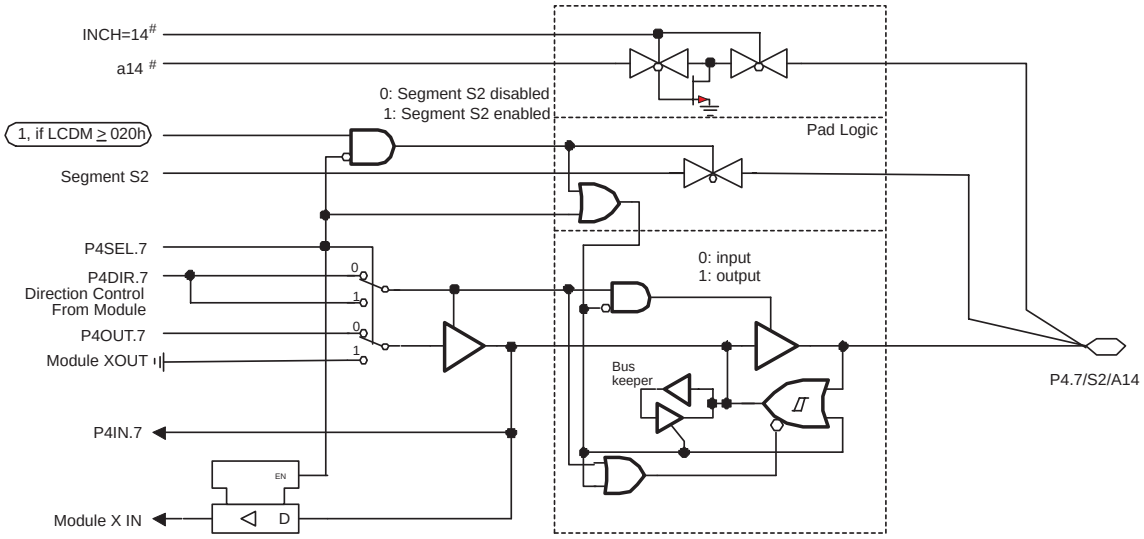
Signal from or to ADC12

PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P4SEL.6	P4DIR.6	P4DIR.6	P4OUT.6	DVSS	P4IN.6	unused

DEVICE	PORT BITS	PORT FUNCTION	LCD SEG. FUNCTION
xG43xIPN 80-pin QFP	P4.6	LCDM < 020h	LVDM ≥ 020h

input/output schematic (continued)

port P4, P4.7, input/output with Schmitt-trigger



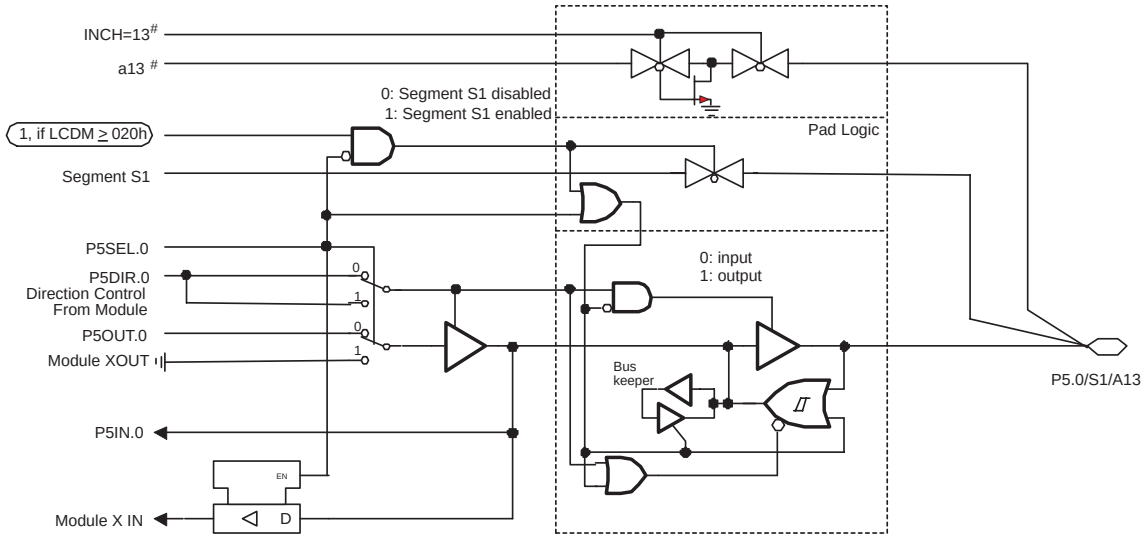
Signal from or to ADC12

PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P4Sel.7	P4DIR.7	P4DIR.7	P4OUT.7	DV_{SS}	P4IN.7	Unused

DEVICE	PORT BITS	PORT FUNCTION	LCD SEG. FUNCTION
xG43xIPN 80-pin QFP	P4.7	LCDM < 020h	LVDM ≥ 020h

input/output schematic (continued)

port P5, P5.0, input/output with Schmitt-trigger



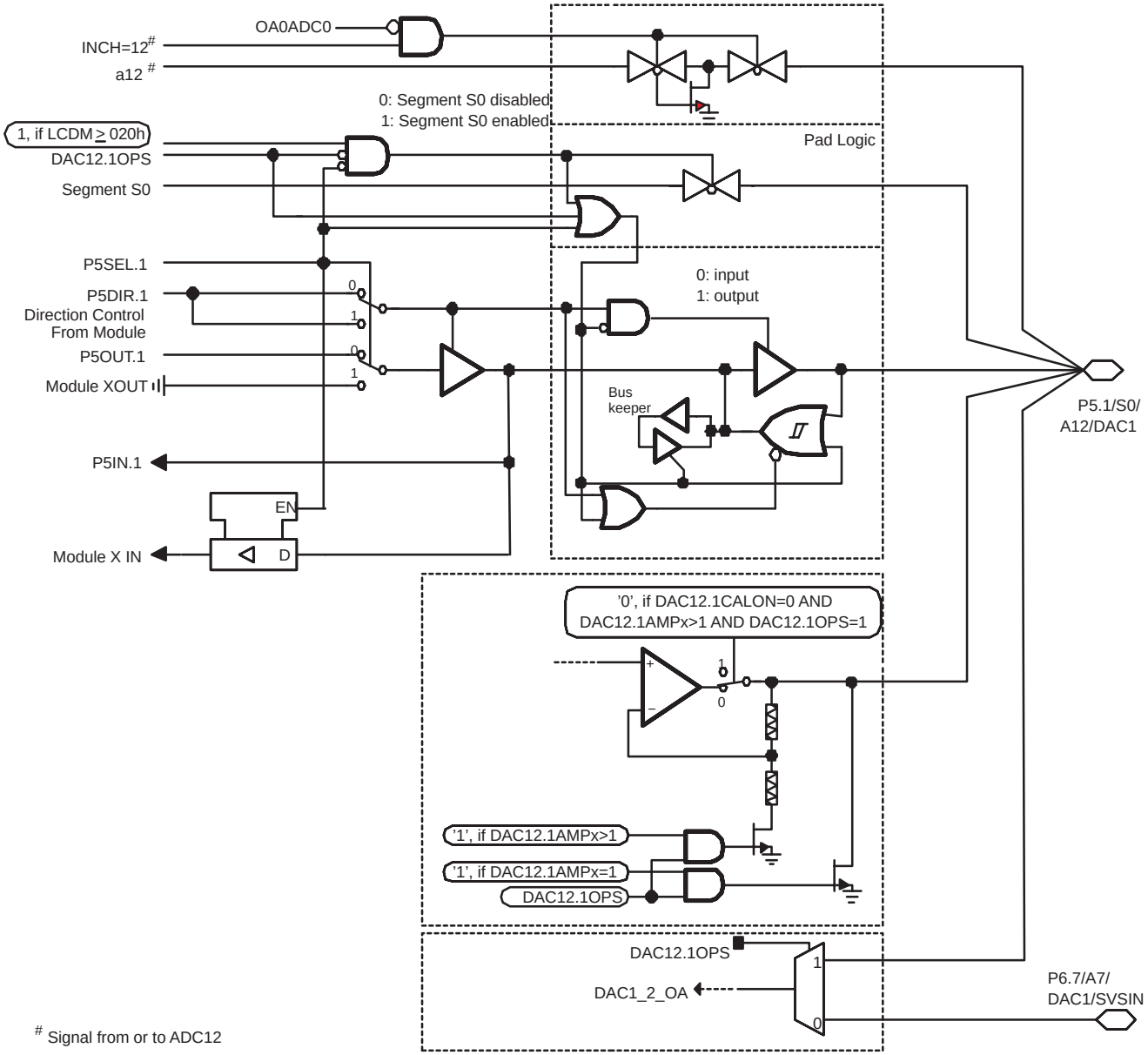
Signal from or to ADC12

PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P5SEL.0	P5DIR.0	P5DIR.0	P5OUT.0	DVSS	P5IN.0	unused

DEVICE	PORT BITS	PORT FUNCTION	LCD SEG. FUNCTION
xG43xIPN 80-pin QFP	P5.0	LCDM < 020h	LVDM ≥ 020h

input/output schematic (continued)

port P5, P5.1, input/output with Schmitt-trigger



Signal from or to ADC12

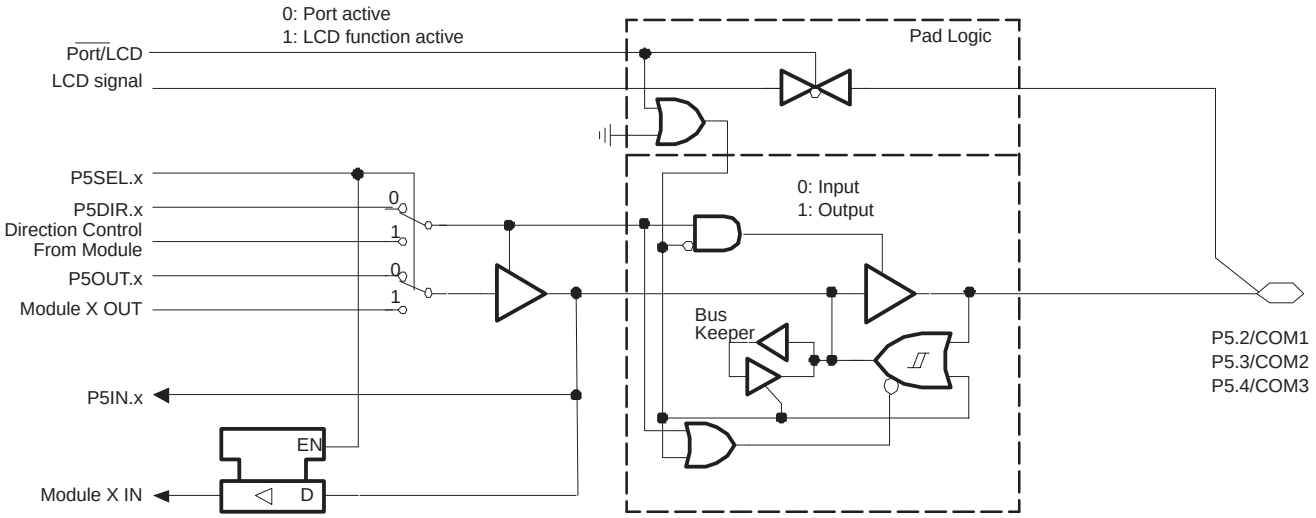
Function	Description	P5SEL.1	LCDM	DAC12.1OPS	DAC12.1AMPx
DAC12	3-State	X	X	1	= 0
	0 V	X	X	1	= 1
	DAC1 output	X	X	1	> 1
	(the o/p voltage can be converted with ADC12, channel A12)				
ADC12	Channel 12, A12	1	X	0	X
LCD	Segment S0, initial state	0	≥ 20h	0	X
Port	P5.1	0	< 20h	0	X

input/output schematic (continued)

port P5, P5.1, input/output with Schmitt-trigger (continued)

PnSEL.x	PnDIR.x	Dir. Control from Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	Segment	$\overline{\text{Port}}$/LCD
P5SEL.1	P5DIR.1	P5DIR.1	P5OUT.1	DVSS	P5IN.1	Unused	S0	0: LCDM<20h

port P5, P5.2 to P5.4, input/output with Schmitt-trigger

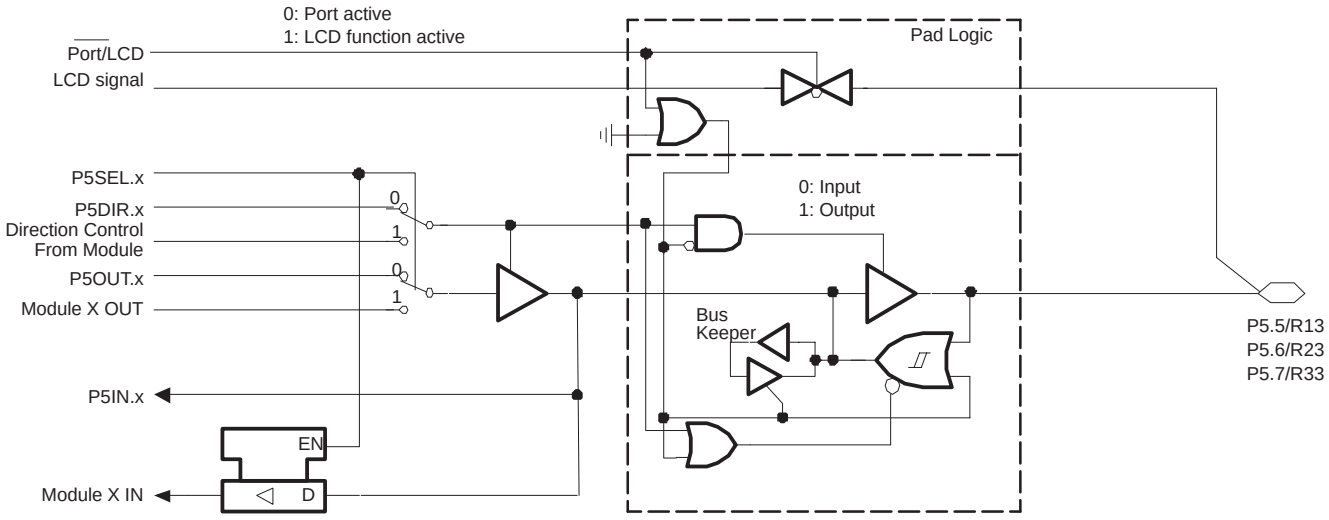


Note: $2 \le x \le 4$

PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	LCD signal	$\overline{\text{Port}}$/LCD
P5Sel.2	P5DIR.2	P5DIR.2	P5OUT.2	DVSS	P5IN.2	Unused	COM1	P5SEL.2
P5Sel.3	P5DIR.3	P5DIR.3	P5OUT.3	DVSS	P5IN.3	Unused	COM2	P5SEL.3
P5Sel.4	P5DIR.4	P5DIR.4	P5OUT.4	DVSS	P5IN.4	Unused	COM3	P5SEL.4

input/output schematic (continued)

port P5, P5.5 to P5.7, input/output with Schmitt-trigger

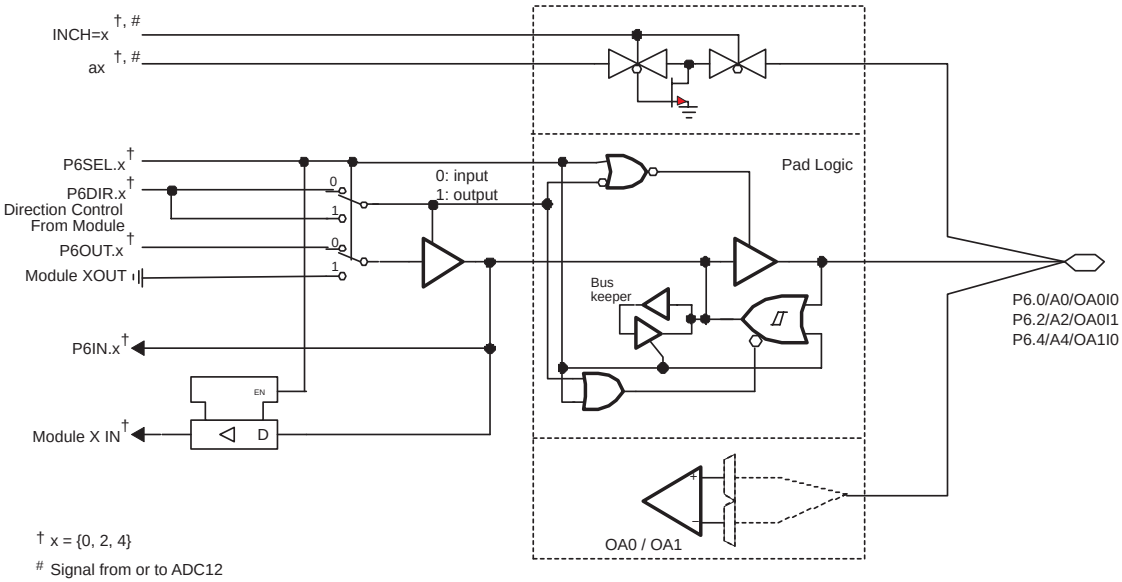


Note: $5 \le x \le 7$

PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	LCD signal	$\overline{\text{Port/LCD}}$
P5Sel.5	P5DIR.5	P5DIR.5	P5OUT.5	DVSS	P5IN.5	Unused	R13	P5SEL.5
P5Sel.6	P5DIR.6	P5DIR.6	P5OUT.6	DVSS	P5IN.6	Unused	R23	P5SEL.6
P5Sel.7	P5DIR.7	P5DIR.7	P5OUT.7	DVSS	P5IN.7	Unused	R33	P5SEL.7

input/output schematic (continued)

port P6, P6.0, P6.2, and P6.4, input/output with Schmitt-trigger

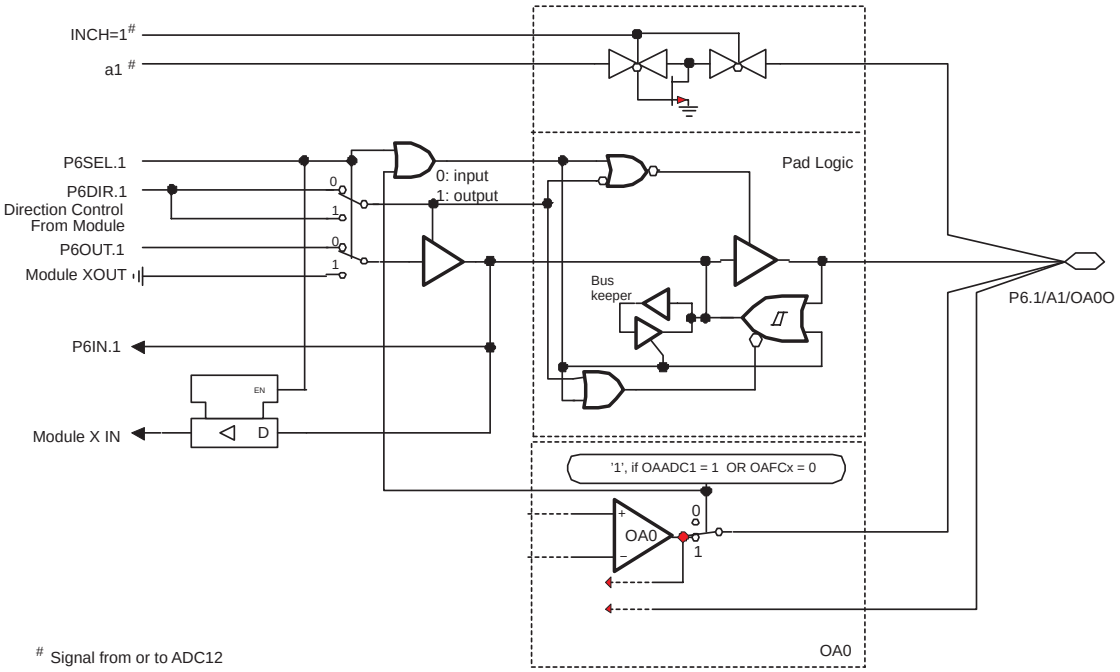


PnSel.x	PnDIR.x	Dir. Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P6Sel.0	P6DIR.0	P6DIR.0	P6OUT.0	DV_{SS}	P6IN.0	unused
P6Sel.2	P6DIR.2	P6DIR.2	P6OUT.2	DV_{SS}	P6IN.2	unused
P6Sel.4	P6DIR.4	P6DIR.4	P6OUT.4	DV_{SS}	P6IN.4	unused

NOTE: The signal at pins P6.x/Ax is used by the 12-bit ADC module.

input/output schematic (continued)

port P6, P6.1, input/output with Schmitt-trigger

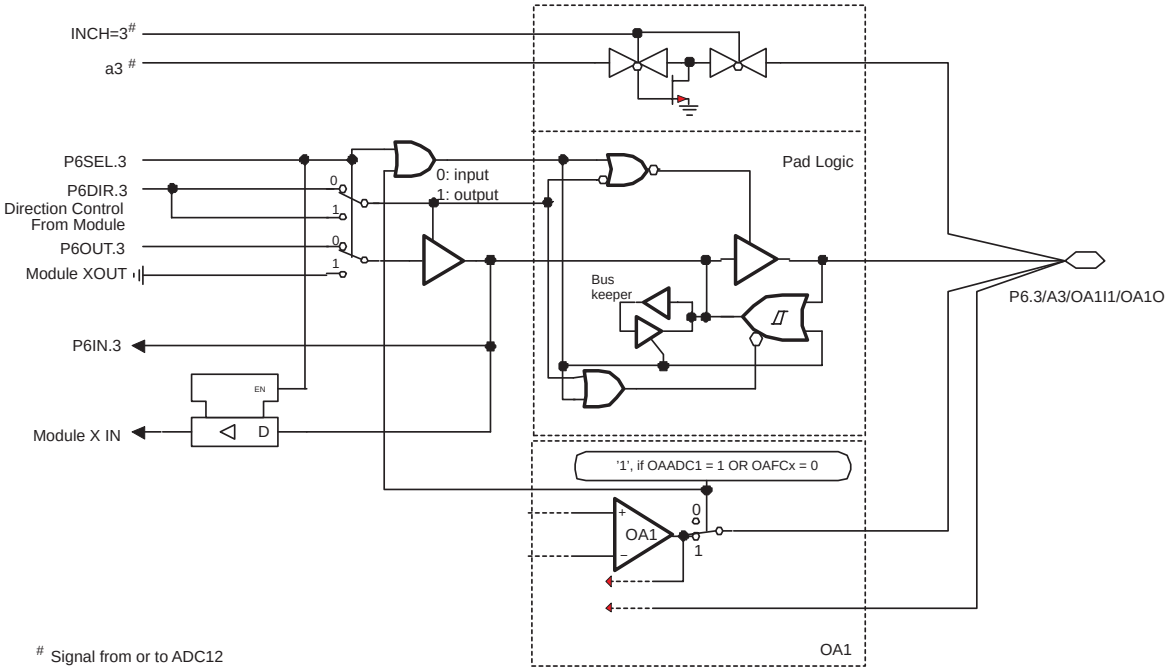


PnSel.x	PnDIR.x	Dir. Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P6Sel.1	P6DIR.1	P6DIR.1	P6OUT.1	DV_{SS}	P6IN.1	unused

NOTE: The signal at pins P6.x/Ax is used by the 12-bit ADC module.

input/output schematic (continued)

port P6, P6.3, input/output with Schmitt-trigger

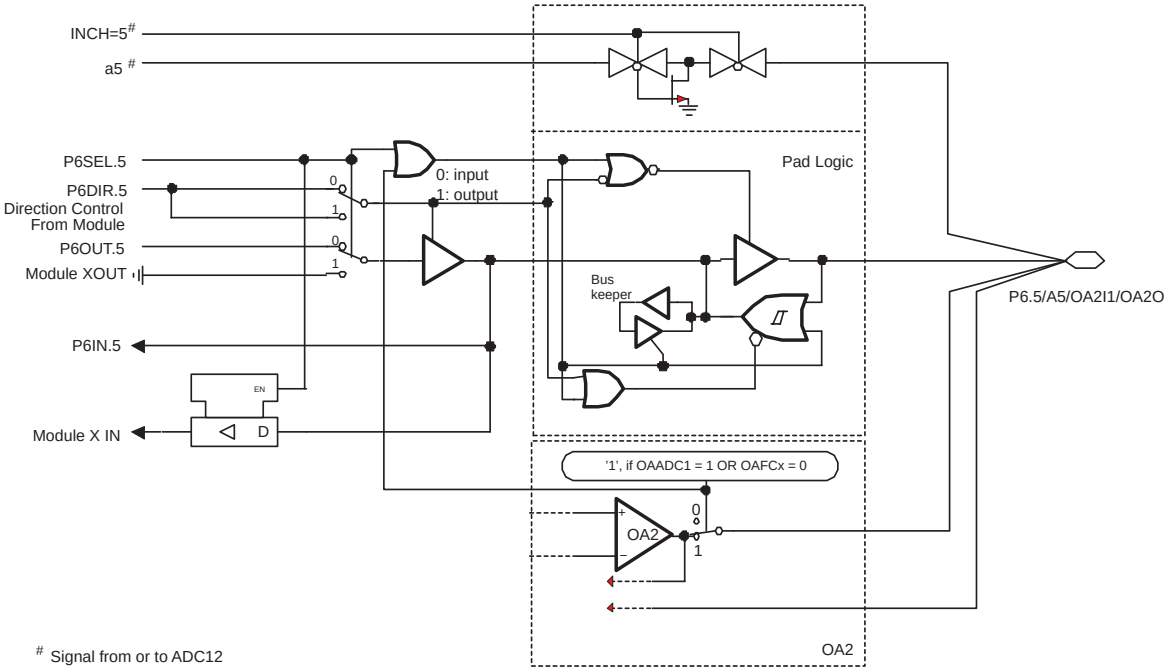


PnSel.x	PnDIR.x	Dir. Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P6Sel.3	P6DIR.3	P6DIR.3	P6OUT.3	DV_{SS}	P6IN.3	unused

NOTE: The signal at pins P6.x/Ax is used by the 12-bit ADC module.

input/output schematic (continued)

port P6, P6.5, input/output with Schmitt-trigger

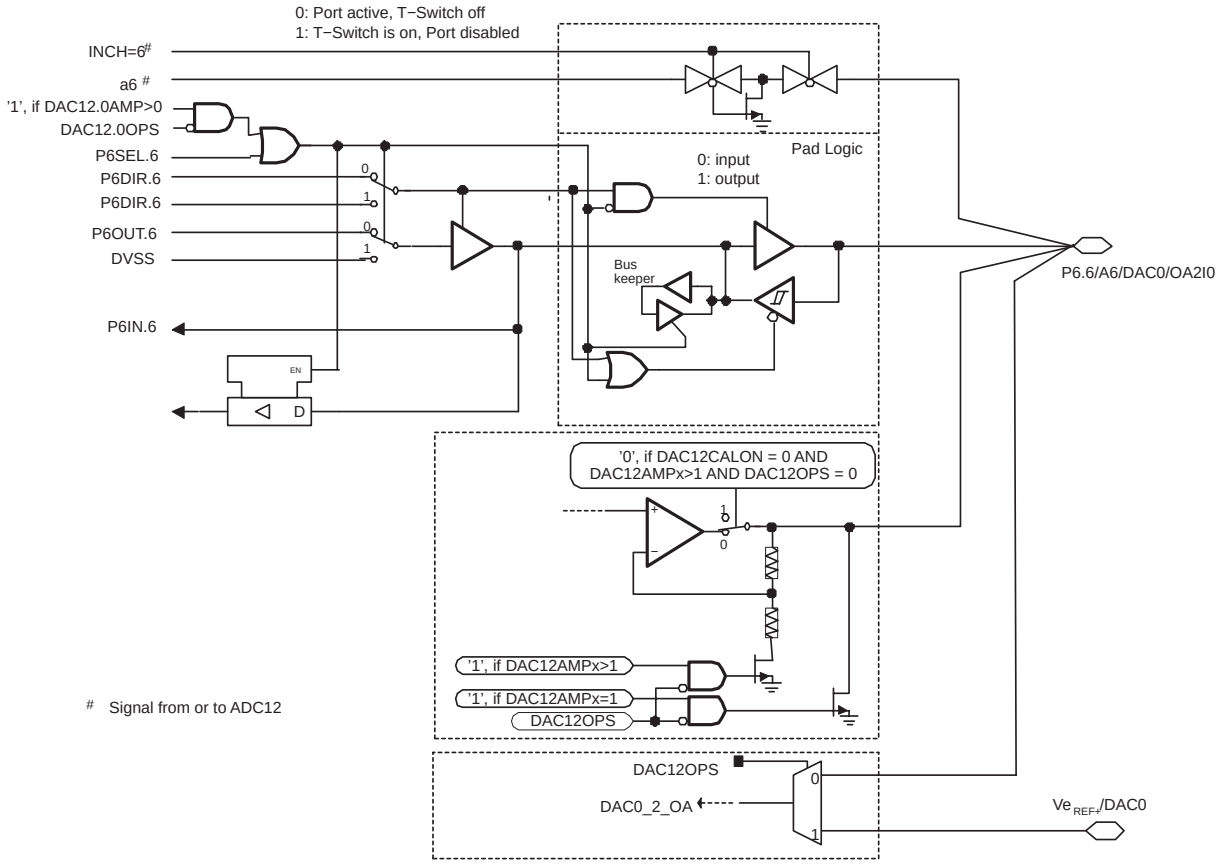


PnSel.x	PnDIR.x	Dir. Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P6Sel.5	P6DIR.5	P6DIR.5	P6OUT.5	DV_{SS}	P6IN.5	unused

NOTE: The signal at pins P6.x/Ax is used by the 12-bit ADC module.

input/output schematic (continued)

port P6, P6.6, input/output with Schmitt-trigger

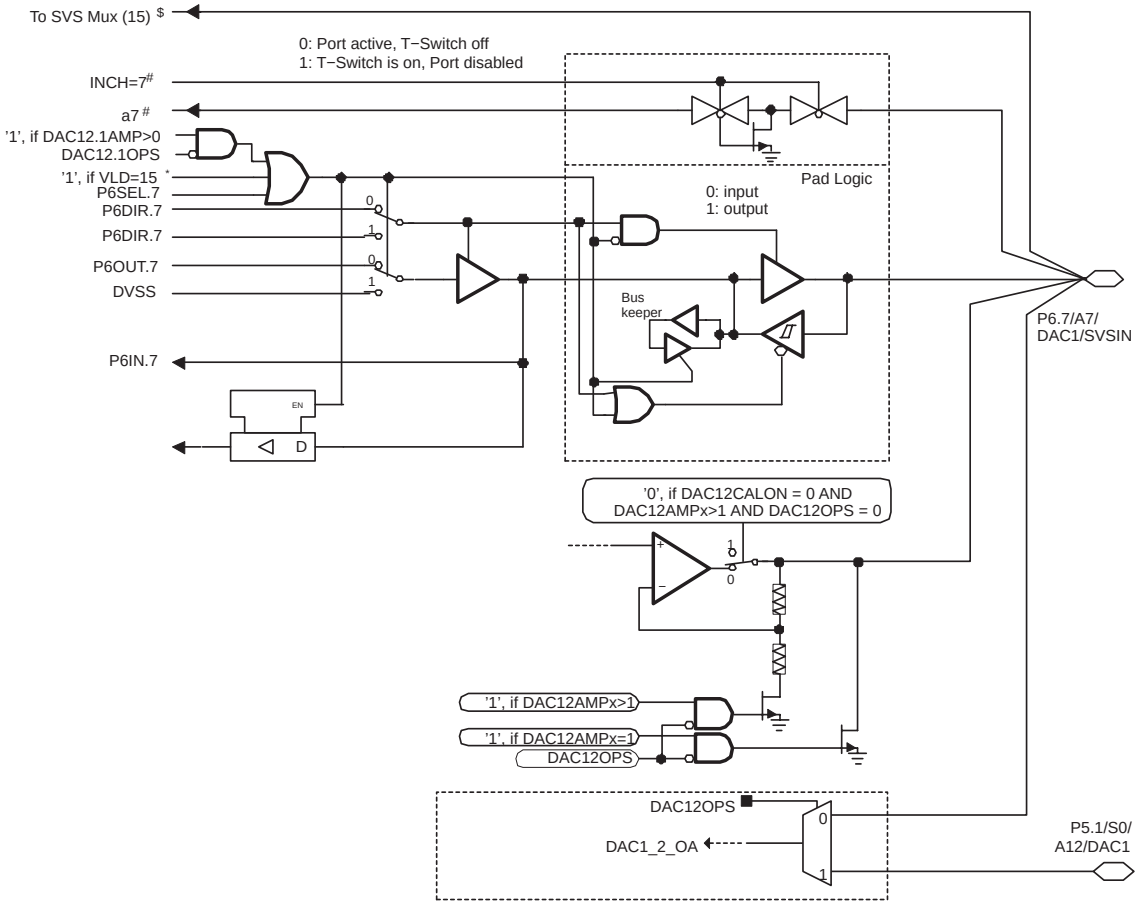


PnSel.x	PnDIR.x	Dir. Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P6Sel.6	P6DIR.6	P6DIR.6	P6OUT.6	DV_{SS}	P6IN.6	unused

NOTE: The signal at pins P6.x/Ax is used by the 12-bit ADC module.

input/output schematic (continued)

port P6, P6.7, input/output with Schmitt-trigger



Signal from or to ADC12

$ Signal to SVS block, selected if VLD=15

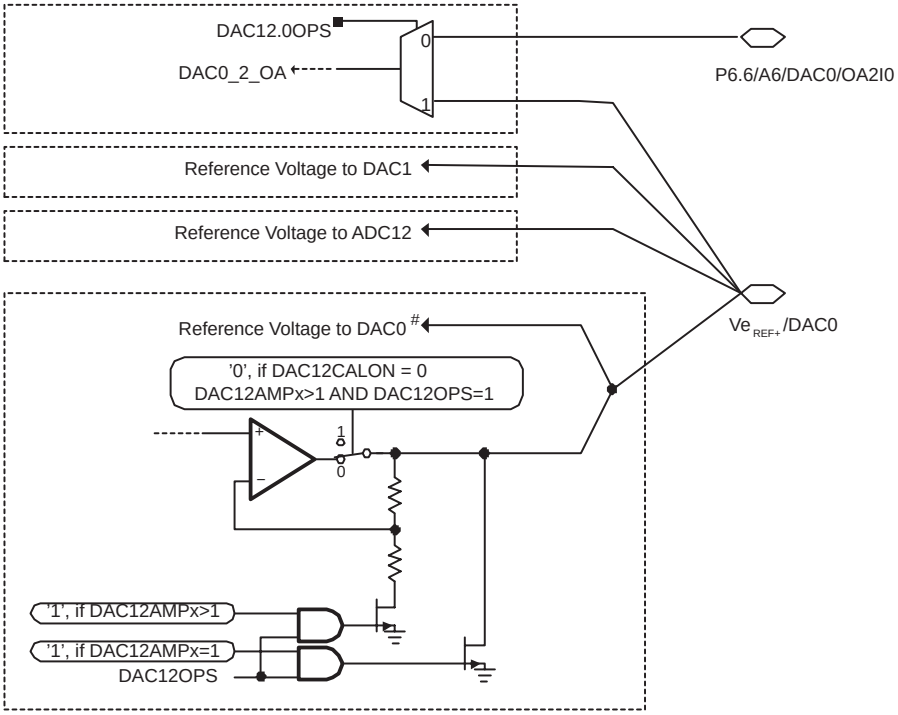
* VLD control bits are located in SVS

PnSel.x	PnDIR.x	Dir. Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P6Sel.7	P6DIR.7	P6DIR.7	P6OUT.7	DV_{SS}	P6IN.7	unused

NOTE: The signal at pins P6.x/Ax is used by the 12-bit ADC module.
The signal at pin P6.7/A7/SVSIN is also connected to the input multiplexer in the module brownout/supply voltage supervisor.

input/output schematic (continued)

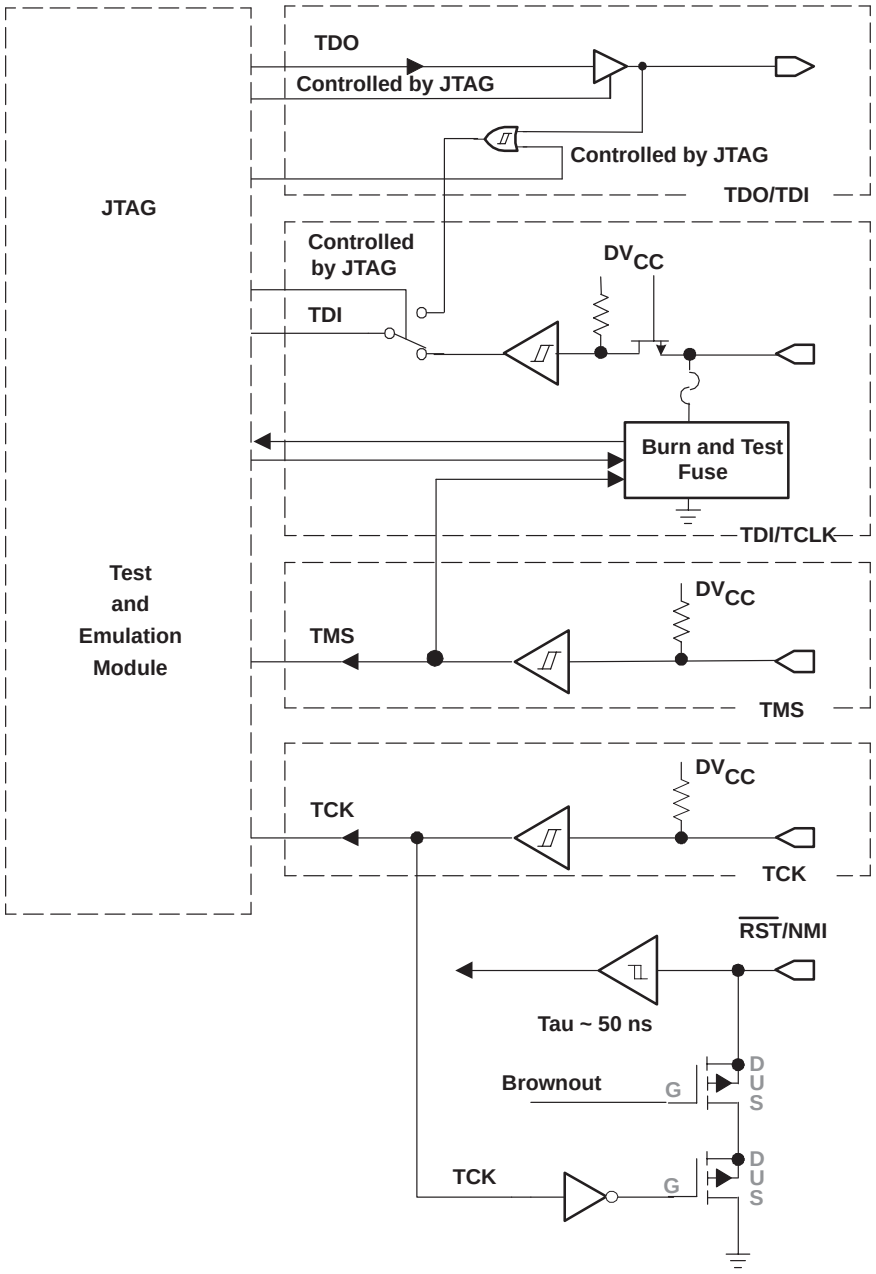
Ve_{REF+}/DAC0



If the reference of DAC0 is taken from pin Ve_{REF+}/DAC0, unpredictable voltage levels will be on pin. In this situation, the DAC0 output is fed back to its own reference input.

input/output schematic (continued)

JTAG pins TMS, TCK, TDI/TCLK, TDO/TDI, input/output with Schmitt-trigger or output



JTAG fuse check mode

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current ($I_{(TF)}$) of 1 mA at 3 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current only flows when the fuse check mode is active and the TMS pin is in a low state (see Figure 32). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition). The JTAG pins are terminated internally and therefore do not require external termination.

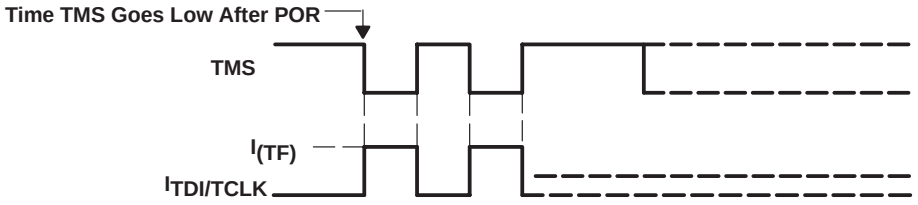


Figure 32. Fuse Check Mode Current

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
MSP430FG437IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430FG437IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430FG438IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430FG438IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430FG439IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430FG439IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

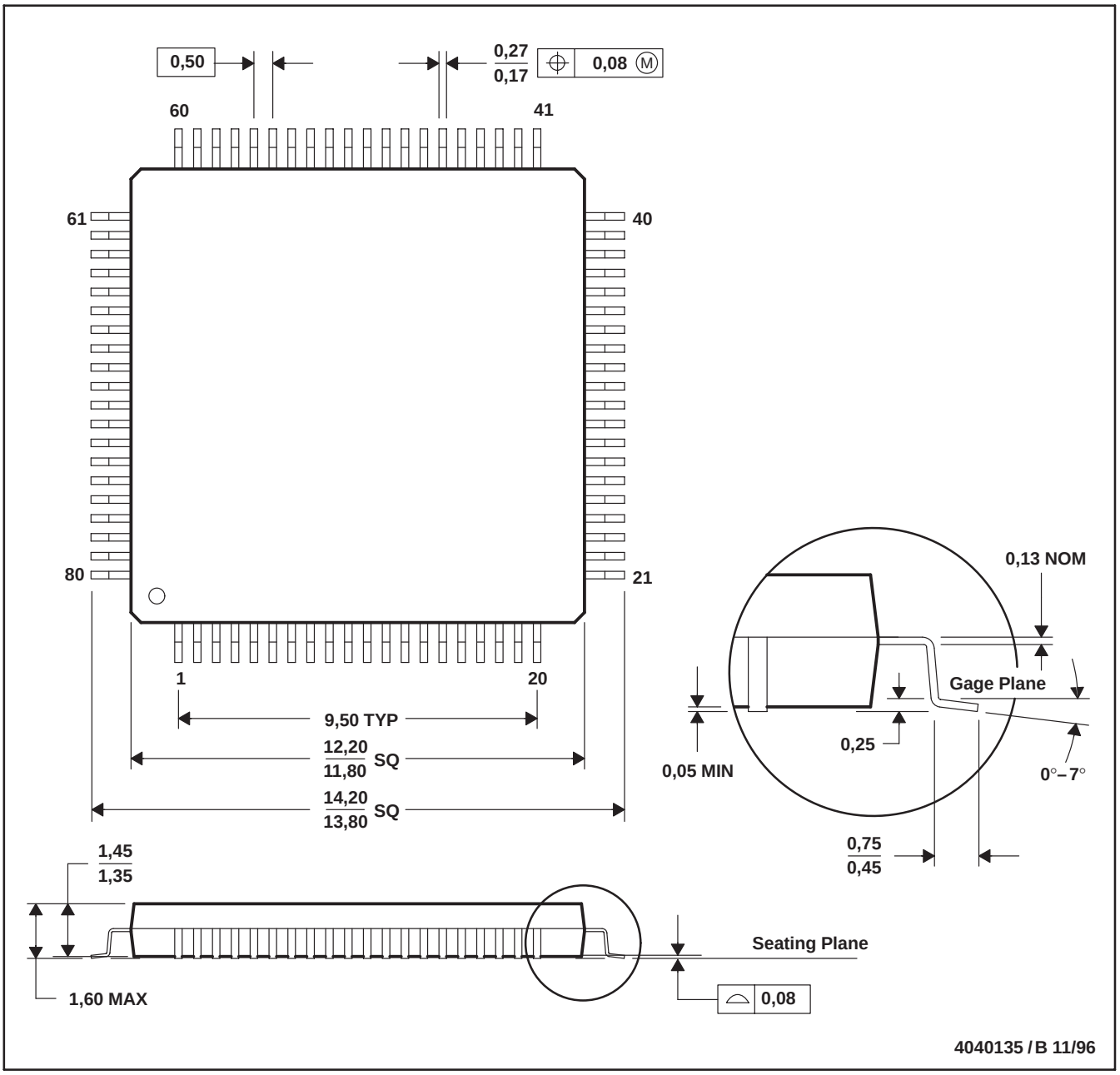
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MTQF010A – JANUARY 1995 – REVISED DECEMBER 1996

PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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