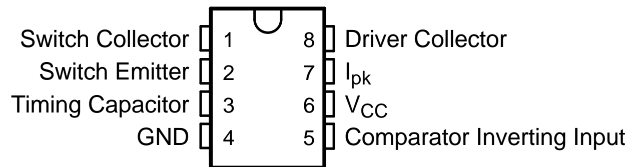
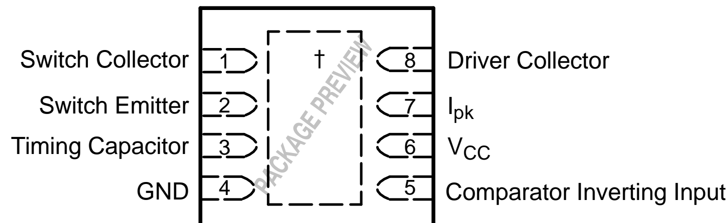
## FEATURES

- **Wide Input Voltage Range…3 V to 40 V**
- **High Output Switch Current…Up to 1.5 A**
- **Adjustable Output Voltage**
- **Oscillator Frequency…Up to 100 kHz**
- **Precision Internal Reference…2%**
- **Short-Circuit Current Limiting**
- **Low Standby Current**




† Exposed thermal pad is connected internally to GND via die attach.

## DESCRIPTION/ORDERING INFORMATION

The MC33063A and MC34063A are easy-to-use ICs containing all the primary circuitry needed for building simple dc-dc converters. These devices primarily consist of an internal temperature-compensated reference, a comparator, an oscillator, a PWM controller with active current limiting, a driver, and a high-current output switch. Thus, the devices require minimal external components to build converters in the boost, buck, and inverting topologies.

The MC33063A is characterized for operation from –40°C to 85°C, while the MC34063A is characterized for operation from 0°C to 70°C.

### ORDERING INFORMATION

| $T_A$ | PACKAGE(1) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | PDIP – P | Tube of 50 | MC33063AP | MC33063AP |
| | QFN – DRJ | Reel of 1000 | MC33063ADRJR | PREVIEW |
| | SOIC – D | Tube of 75 | MC33063AD | M33063A |
| | | Reel of 2500 | MC33063ADR | |
| 0°C to 70°C | PDIP – P | Tube of 50 | MC34063AP | MC34063AP |
| | QFN – DRJ | Reel of 1000 | MC34063ADRJR | PREVIEW |
| | SOIC – D | Tube of 75 | MC34063AD | M34063A |
| | | Reel of 2500 | MC34063ADR | |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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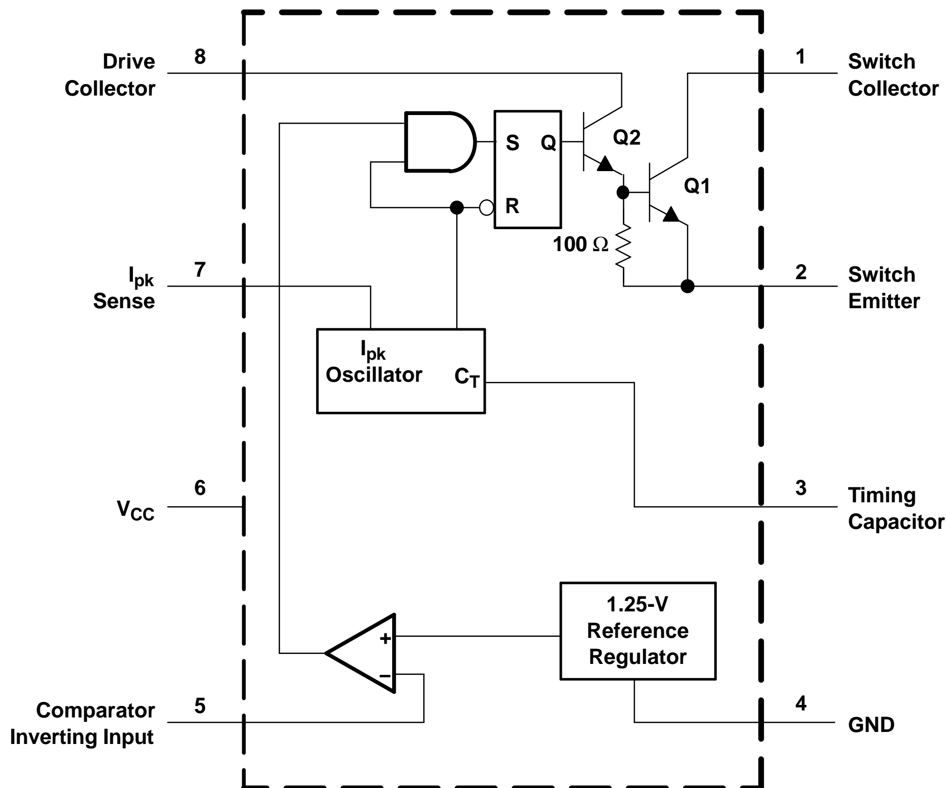
## FUNCTIONAL BLOCK DIAGRAM




## Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | 40 | V |
| $V_{IR}$ | Comparator Inverting Input voltage range | | –0.3 | 40 | V |
| $V_{C(switch)}$ | Switch Collector voltage | | | 40 | V |
| $V_{E(switch)}$ | Switch Emitter voltage | $V_{PIN1}$ = 40 V | | 40 | V |
| $V_{CE(switch)}$ | Switch Collector to Switch Emitter voltage | | | 40 | V |
| $V_{C(driver)}$ | Driver Collector voltage | | | 40 | V |
| $I_{C(driver)}$ | Driver Collector current | | | 100 | mA |
| $I_{SW}$ | Switch current | | | 1.5 | A |
| $\theta_{JA}$ | Package thermal impedance[2][3] | D package | | 97 | °C/W |
| | | DRJ package | | TBD | |
| | | P package | | 85 | |
| $T_J$ | Operating virtual junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum power dissipation is a function of $T_J$(max), $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 3 | 40 | V |
| $T_A$ | Operating free-air temperature | MC33063A | –40 | 85 | °C |
| | | MC34063A | 0 | 70 | |

## Electrical Characteristics

$V_{CC}$ = 5 V, $T_A$ = full operating range (unless otherwise noted) (see block diagram)

### Oscillator

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{osc}$ | Oscillator frequency | $V_{PIN5}$ = 0 V, $C_T$ = 1 nF | 25°C | 24 | 33 | 42 | kHz |
| $I_{chg}$ | Charge current | $V_{CC}$ = 5 V to 40 V | 25°C | 24 | 35 | 42 | µA |
| $I_{dischg}$ | Discharge current | $V_{CC}$ = 5 V to 40 V | 25°C | 140 | 220 | 260 | µA |
| $I_{dischg}/I_{chg}$ | Discharge-to-charge current ratio | $V_{PIN7}$ = $V_{CC}$ | 25°C | 5.2 | 6.5 | 7.5 | |
| $V_{Ipk}$ | Current-limit sense voltage | $I_{dischg}$ = $I_{chg}$ | 25°C | 250 | 300 | 350 | mV |

### Output Switch(1)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CE(sat)}$ | Saturation voltage – Darlington connection | $I_{SW}$ = 1 A, pins 1 and 8 connected | Full range | | 1 | 1.3 | V |
| $V_{CE(sat)}$ | Saturation voltage – non-Darlington connection (2) | $I_{SW}$ = 1 A, $R_{PIN8}$ = 82 Ω to $V_{CC}$, forced β ~ 20 | Full range | | 0.45 | 0.7 | V |
| $h_{FE}$ | DC current gain | $I_{SW}$ = 1 A, $V_{CE}$ = 5 V | 25°C | 50 | 75 | | |
| $I_{C(off)}$ | Collector off-state current | $V_{CE}$ = 40 V | Full range | | 0.01 | 100 | µA |

(1) Low duty-cycle pulse testing is used to maintain junction temperature as close to ambient temperature as possible.
(2) In the non-Darlington configuration, if the output switch is driven into hard saturation at low switch currents (≤300 mA) and high driver currents (≥30 mA), it may take up to 2 µs for the switch to come out of saturation. This condition effectively shortens the off time at frequencies ≥30 kHz, becoming magnified as temperature increases. The following output drive condition is recommended in the non-Darlington configuration:
Forced β of output switch = $I_{C,SW}$ / ($I_{C,driver}$ – 7 mA) ≥ 10, where ~7 mA is required by the 100-Ω resistor in the emitter of the driver to forward bias the $V_{be}$ of the switch.

### Comparator

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{th}$ | Threshold voltage | | 25°C | 1.225 | 1.25 | 1.275 | V |
| | | | Full range | 1.21 | | 1.29 | |
| $\Delta V_{th}$ | Threshold-voltage line regulation | $V_{CC}$ = 5 V to 40 V | Full range | | 1.4 | 5 | mV |
| $I_{IB}$ | Input bias current | $V_{IN}$ = 0 V | Full range | | –20 | –400 | nA |

### Total Device

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply current | $V_{CC}$ = 5 V to 40 V, $C_T$ = 1 nF, $V_{PIN7}$ = $V_{CC}$, $V_{PIN5}$ > $V_{th}$, $V_{PIN2}$ = GND, All other pins open | Full range | | 4 | mA |

## TYPICAL CHARACTERISTICS

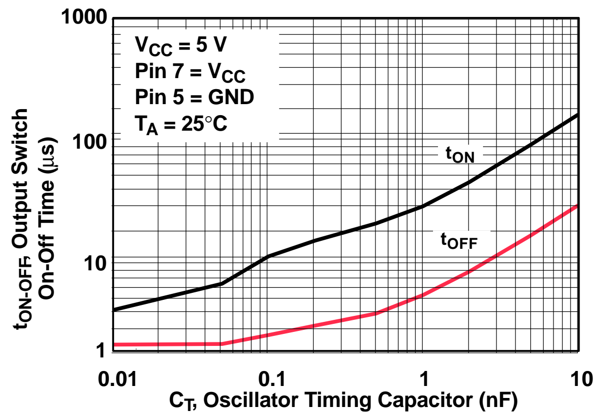



**Figure 1. Output Switch On-Off Time vs Oscillator Timing Capacitor**

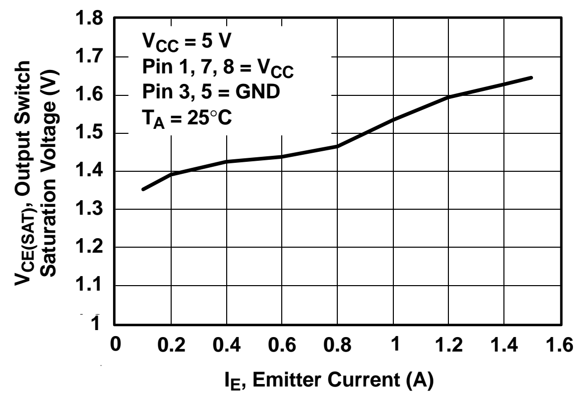



**Figure 2. Output Switch Saturation Voltage vs Emitter Current (Emitter-Follower Configuration)**

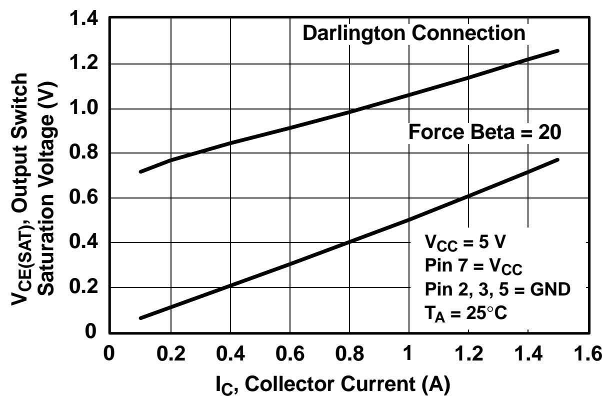



**Figure 3. Output Switch Saturation Voltage vs Collector Current (Common-Emitter Configuration)**

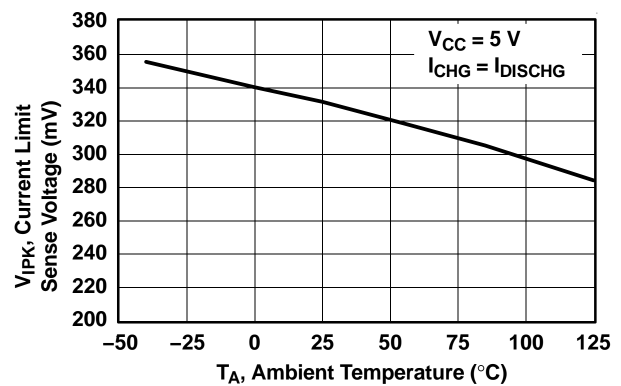



**Figure 4. Current-Limit Sense Voltage vs Temperature**

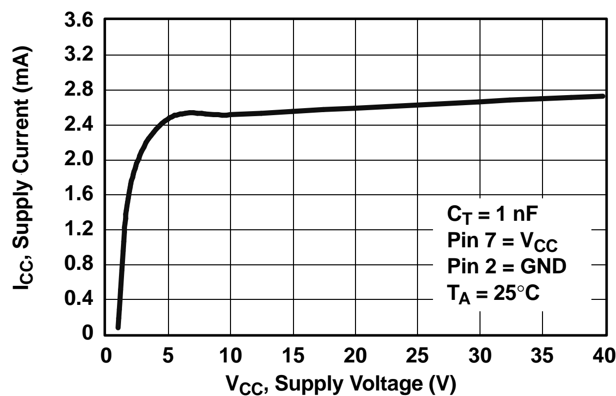



**Figure 5. Standby Supply Current vs Supply Voltage**

## TYPICAL CHARACTERISTICS (continued)

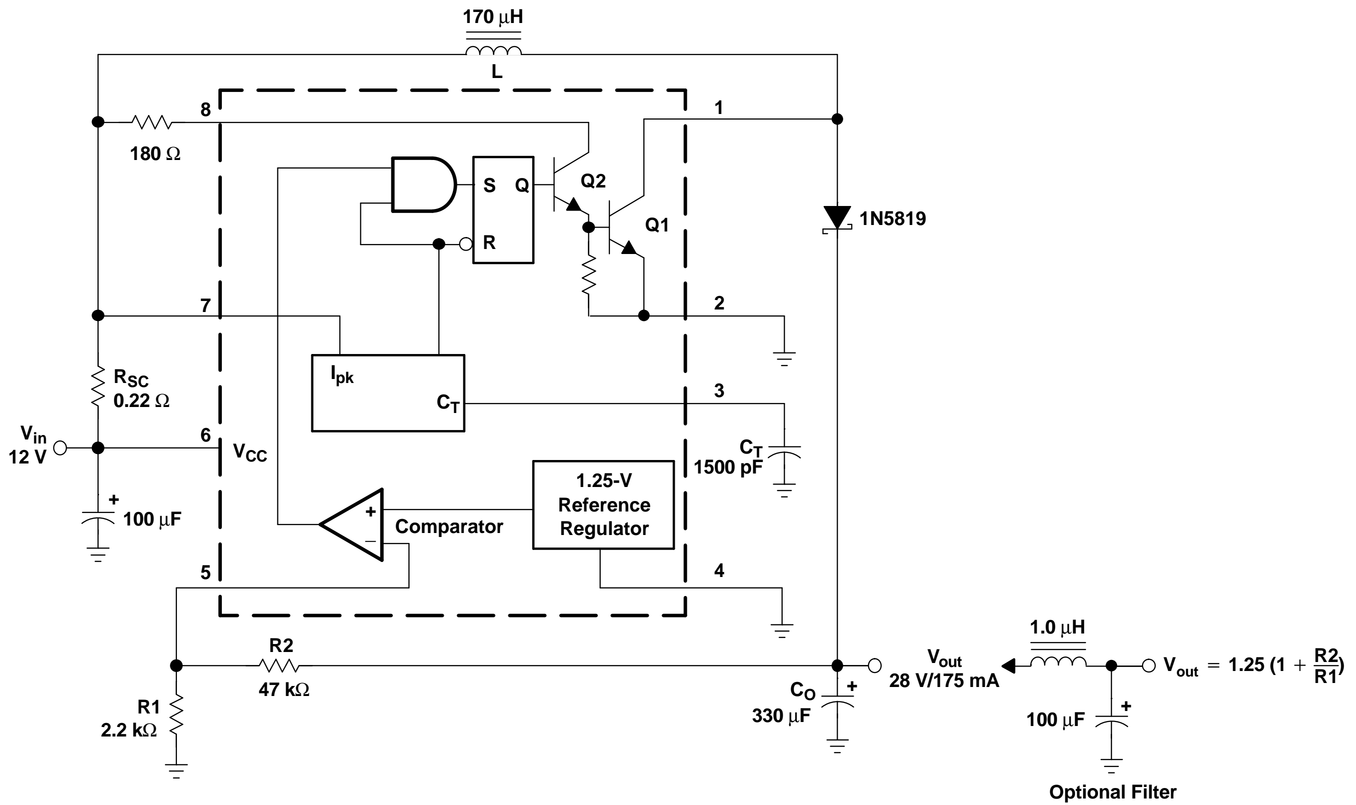
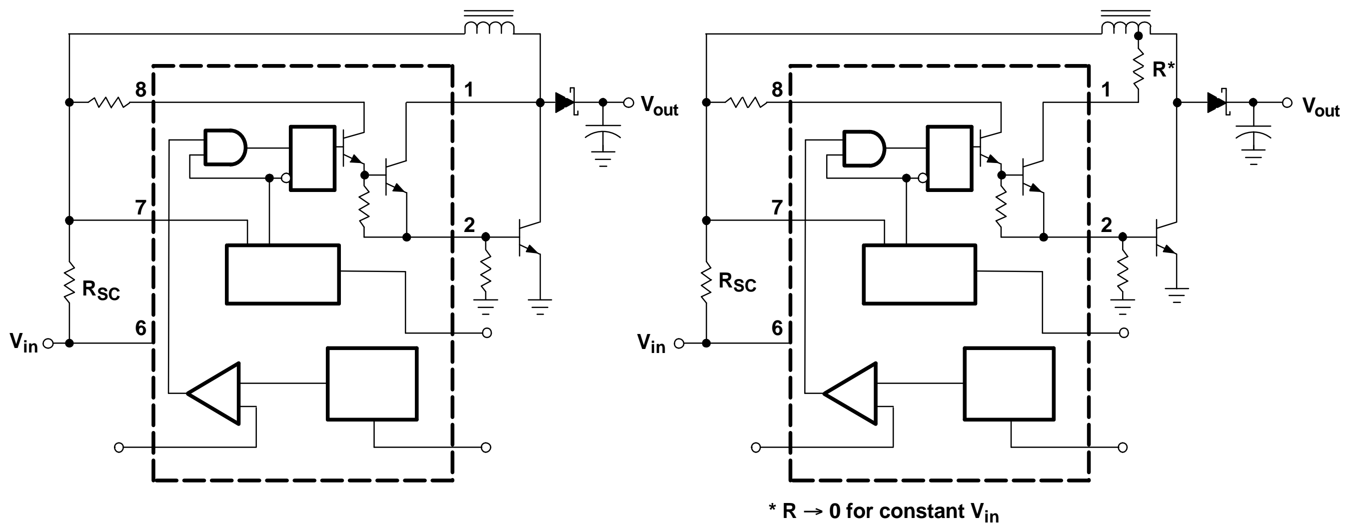



**Figure 6. Step-Up Converter**

| TEST | CONDITIONS | RESULTS |
|---|---|---|
| Line regulation | $V_{IN}$ = 8 V to 16 V, $I_O$ = 175 mA | 30 mV ± 0.05% |
| Load regulation | $V_{IN}$ = 12 V, $I_O$ = 75 mA to 175 mA | 10 mV ± 0.017% |
| Output ripple | $V_{IN}$ = 12 V, $I_O$ = 175 mA | 400 $mV_{PP}$ |
| Efficiency | $V_{IN}$ = 12 V, $I_O$ = 175 mA | 87.7% |
| Output ripple with optional filter | $V_{IN}$ = 12 V, $I_O$ = 175 mA | 40 $mV_{PP}$ |




a) EXTERNAL npn SWITCH

b) EXTERNAL pnp SATURATED SWITCH (see Note A)

A. If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents (≤300 mA) and high driver currents (≥30 mA), it may take up to 2 µs to come out of saturation. This condition will shorten the off time at frequencies ≥30 kHz and is magnified at high temperatures. This condition does not occur with a Darlington configuration because the output switch cannot saturate. If a non-Darlington configuration is used, the output drive configuration in Figure 7b is recommended.

**Figure 7. External Current-Boost Connections for $I_C$ Peak Greater Than 1.5 A**

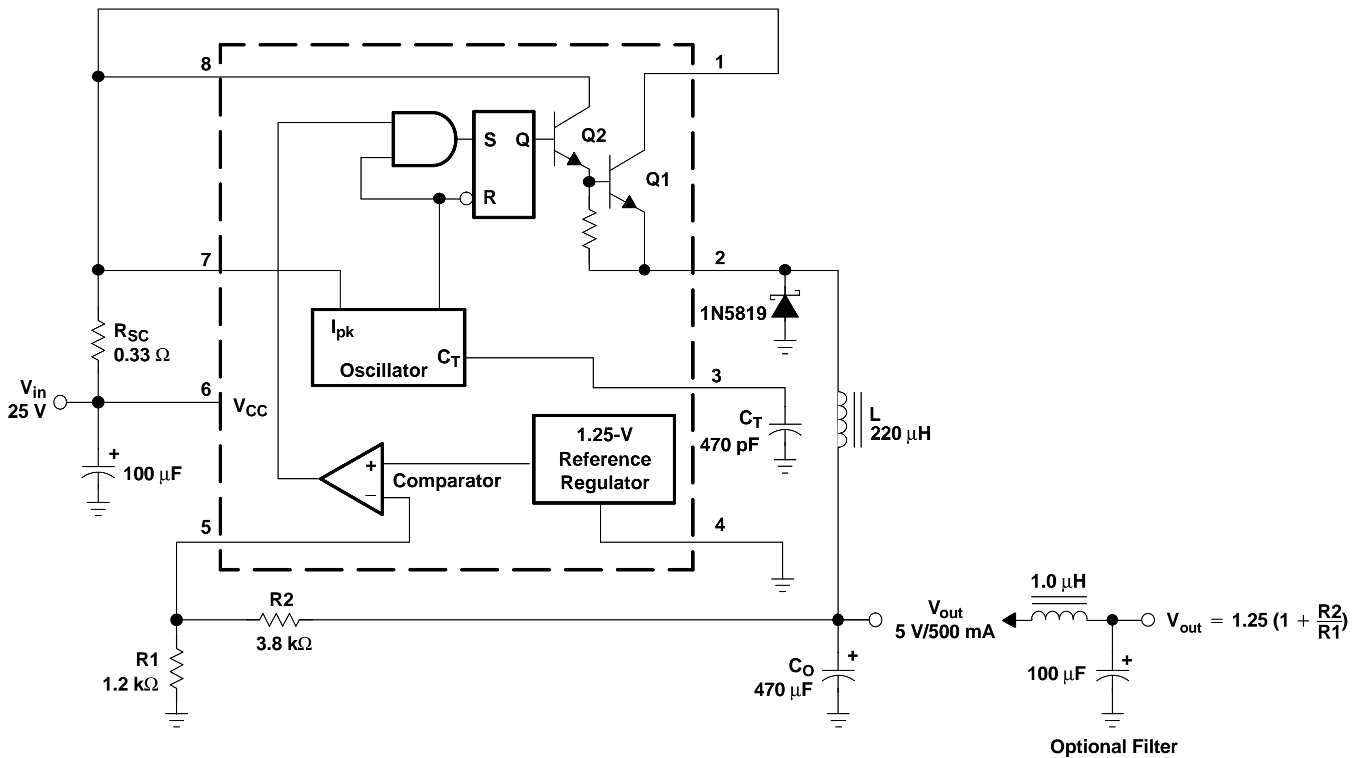



**Figure 8. Step-Down Converter**

| TEST | CONDITIONS | RESULTS |
|---|---|---|
| Line regulation | $V_{IN}$ = 15 V to 25 V, $I_O$ = 500 mA | 12 mV ± 0.12% |
| Load regulation | $V_{IN}$ = 25 V, $I_O$ = 50 mA to 500 mA | 3 mV ± 0.03% |
| Output ripple | $V_{IN}$ = 25 V, $I_O$ = 500 mA | 120 $mV_{PP}$ |
| Short-circuit current | $V_{IN}$ = 25 V, $R_L$ = 0.1 Ω | 1.1 A |
| Efficiency | $V_{IN}$ = 25 V, $I_O$ = 500 mA | 83.7% |
| Output ripple with optional filter | $V_{IN}$ = 25 V, $I_O$ = 500 mA | 40 $mV_{PP}$ |

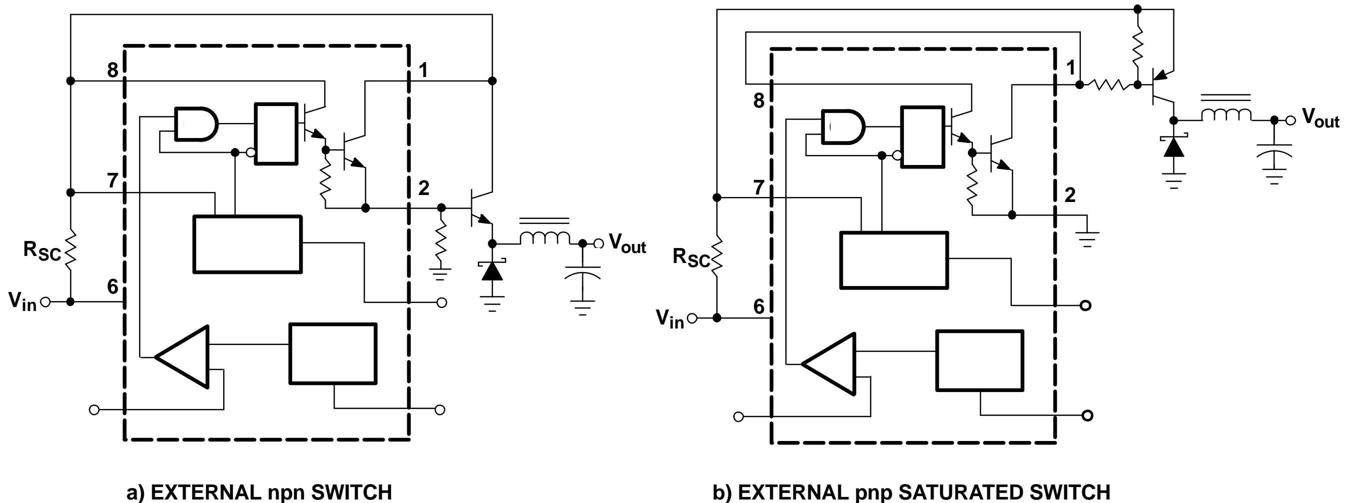



**Figure 9. External Current-Boost Connections for $I_C$ Peak Greater Than 1.5 A**

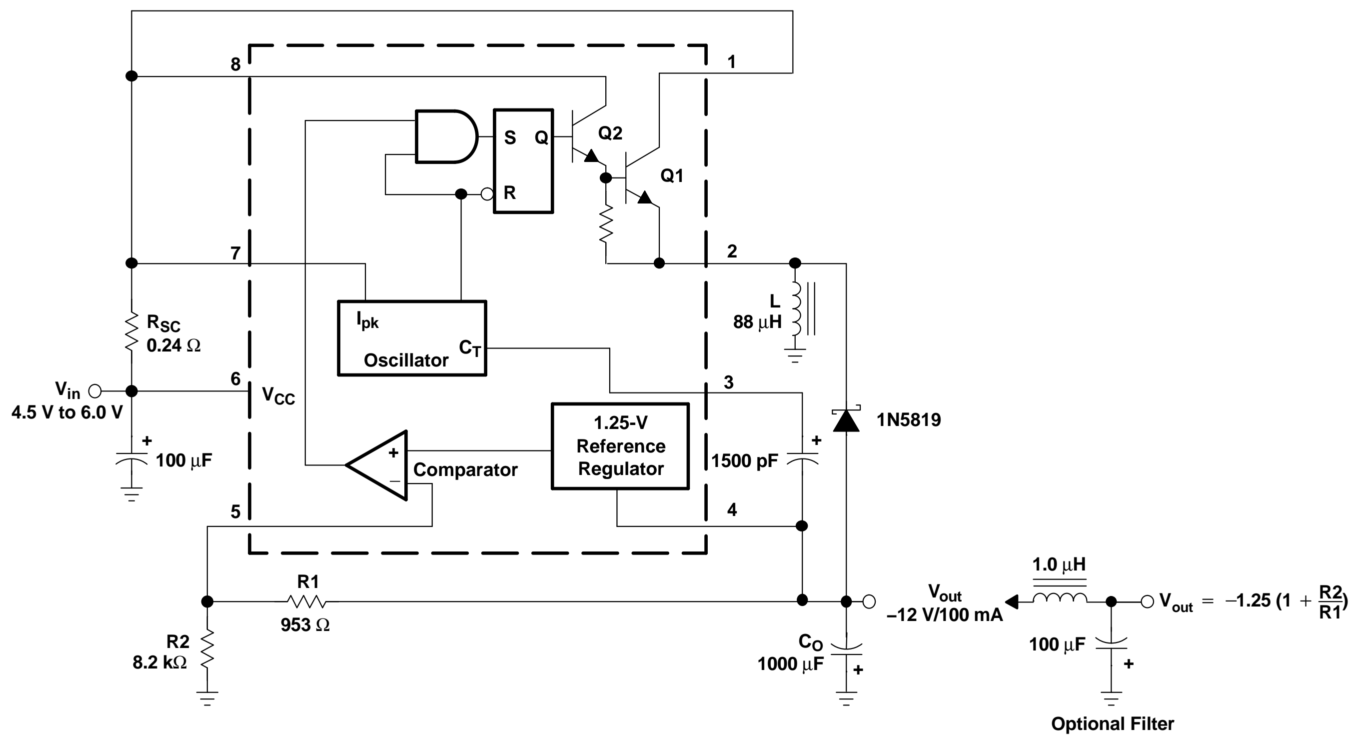



**Figure 10. Voltage-Inverting Converter**

| TEST | CONDITIONS | RESULTS |
|---|---|---|
| Line regulation | $V_{IN}$ = 4.5 V to 6 V, $I_O$ = 100 mA | 3 mV ± 0.12% |
| Load regulation | $V_{IN}$ = 5 V, $I_O$ = 10 mA to 100 mA | 0.022 V ± 0.09% |
| Output ripple | $V_{IN}$ = 5 V, $I_O$ = 100 mA | 500 $mV_{PP}$ |
| Short-circuit current | $V_{IN}$ = 5 V, $R_L$ = 0.1 Ω | 910 mA |
| Efficiency | $V_{IN}$ = 5 V, $I_O$ = 100 mA | 62.2% |
| Output ripple with optional filter | $V_{IN}$ = 5 V, $I_O$ = 100 mA | 70 $mV_{PP}$ |

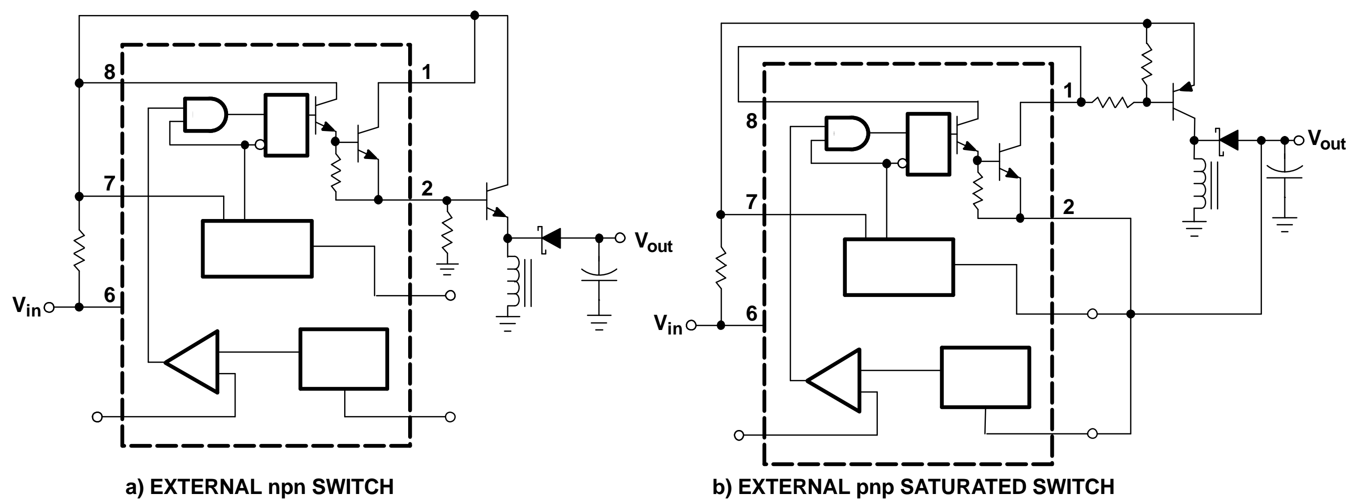



**Figure 11. External Current-Boost Connections for $I_C$ Peak Greater Than 1.5 A**

## APPLICATION INFORMATION

| CALCULATION | STEP UP | STEP DOWN | VOLTAGE INVERTING |
|---|---|---|---|
| $t_{on}/t_{off}$ | $\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$ | $\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$ | $\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{sat}}$ |
| $(t_{on} + t_{off})$ | $\frac{1}{f}$ | $\frac{1}{f}$ | $\frac{1}{f}$ |
| $t_{off}$ | $\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$ | $\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$ | $\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$ |
| $t_{on}$ | $(t_{on} + t_{off}) - t_{off}$ | $(t_{on} + t_{off}) - t_{off}$ | $(t_{on} + t_{off}) - t_{off}$ |
| $C_T$ | $4 \times 10^{-5}\, t_{on}$ | $4 \times 10^{-5}\, t_{on}$ | $4 \times 10^{-5}\, t_{on}$ |
| $I_{pk(switch)}$ | $2I_{out(max)}\left(\frac{t_{on}}{t_{off}} + 1\right)$ | $2I_{out(max)}$ | $2I_{out(max)}\left(\frac{t_{on}}{t_{off}} + 1\right)$ |
| $R_{SC}$ | $\frac{0.3}{I_{pk(switch)}}$ | $\frac{0.3}{I_{pk(switch)}}$ | $\frac{0.3}{I_{pk(switch)}}$ |
| $L_{(min)}$ | $\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}}\right)t_{on(max)}$ | $\left(\frac{(V_{in(min)} - V_{sat} - V_{out})}{I_{pk(switch)}}\right)t_{on(max)}$ | $\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}}\right)t_{on(max)}$ |
| $C_O$ | $9\frac{I_{out}t_{on}}{V_{ripple(pp)}}$ | $\frac{I_{pk(switch)}(t_{on} + t_{off})}{8V_{ripple(pp)}}$ | $9\frac{I_{out}t_{on}}{V_{ripple(pp)}}$ |
| $V_{out}$ | $1.25(1 + \frac{R2}{R1})$ See Figure 6 | $1.25(1 + \frac{R2}{R1})$ See Figure 8 | $-1.25(1 + \frac{R2}{R1})$ See Figure 10 |

$V_{sat}$ = Saturation voltage of the output switch

$V_F$ = Forward voltage drop of the chosen output rectifier

The following power-supply parameters are set by the user:

- $V_{in}$ = Nominal input voltage
- $V_{out}$ = Desired output voltage
- $I_{out}$ = Desired output current
- $f_{min}$ = Minimum desired output switching frequency at the selected values of $V_{in}$ and $I_{out}$
- $V_{ripple}$ = Desired peak-to-peak output ripple voltage. The ripple voltage directly affects the line and load regulation and, thus, must be considered. In practice, the actual capacitor value should be larger than the calculated value, to account for the capacitor's equivalent series resistance and board layout.

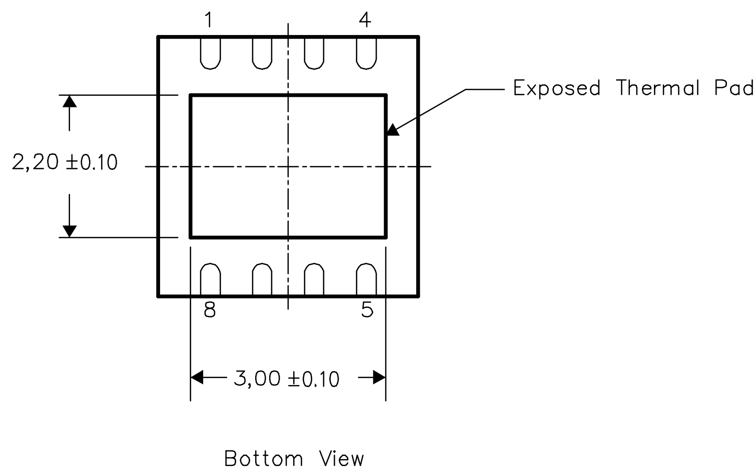
# THERMAL PAD MECHANICAL DATA
# DRJ (S-PDSO-N8)

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No−Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

4206882/A 03/05

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| MC33063AD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| MC33063ADE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| MC33063ADG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| MC33063ADR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| MC33063ADRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| MC33063ADRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| MC33063ADRJR | ACTIVE | SON | DRJ | 8 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| MC33063ADRJRG4 | ACTIVE | SON | DRJ | 8 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| MC33063AP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| MC33063APE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| MC34063AD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| MC34063ADE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| MC34063ADG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| MC34063ADR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| MC34063ADRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| MC34063ADRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| MC34063ADRJR | ACTIVE | SON | DRJ | 8 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| MC34063ADRJRG4 | ACTIVE | SON | DRJ | 8 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| MC34063AP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| MC34063APE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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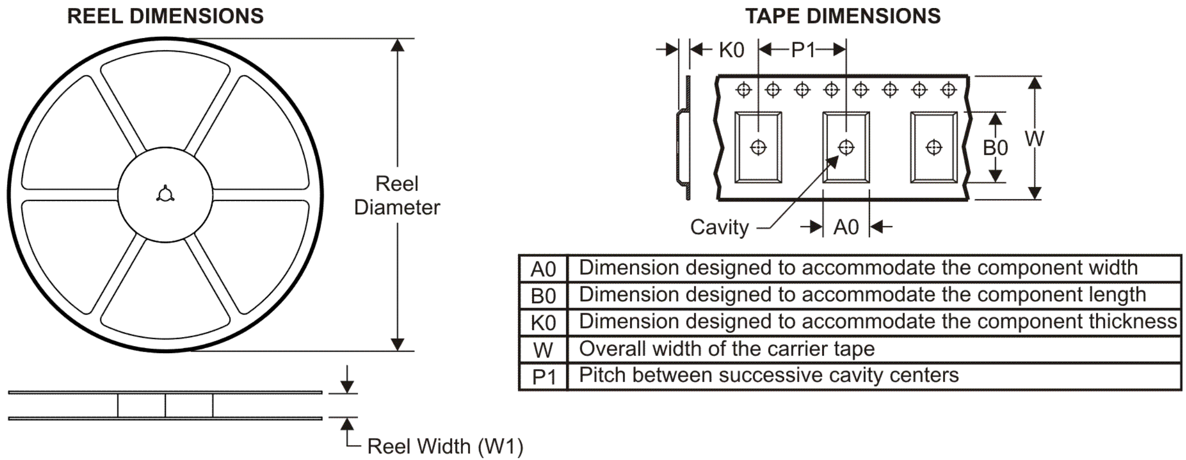
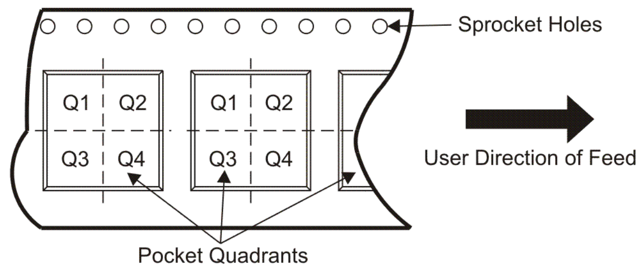
## TAPE AND REEL INFORMATION




| A0 | Dimension designed to accommodate the component width |
|---|---|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

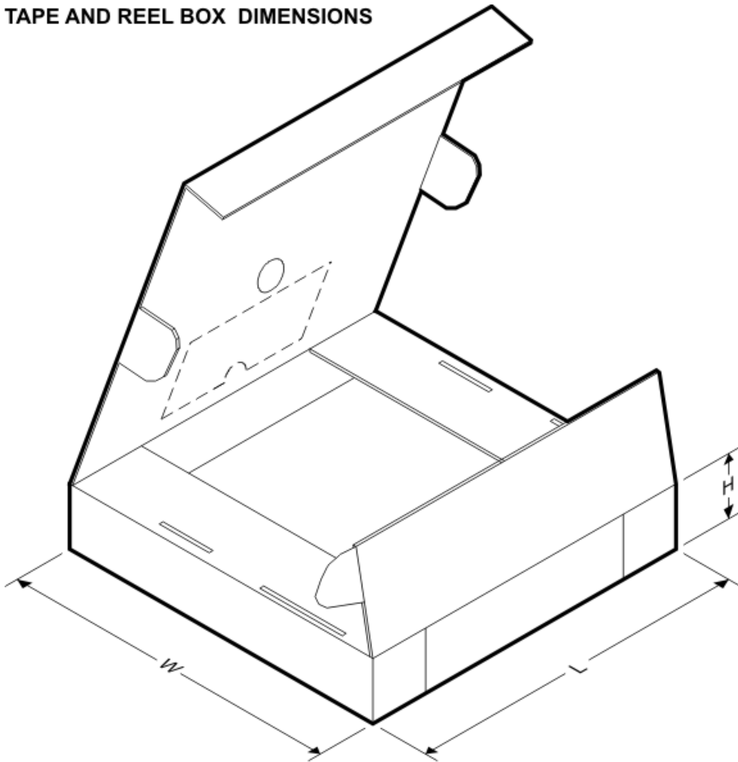
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MC33063ADR | SOIC | D | 8 | 2500 | 330.0 | 12.0 | 6.0 | 5.0 | 2.0 | 8.0 | 12.0 | Q1 |
| MC33063ADRJR | SON | DRJ | 8 | 1000 | 180.0 | 12.0 | 4.0 | 4.0 | 2.0 | 8.0 | 12.0 | Q2 |
| MC34063ADR | SOIC | D | 8 | 2500 | 330.0 | 12.0 | 6.0 | 5.0 | 2.0 | 8.0 | 12.0 | Q1 |
| MC34063ADRJR | SON | DRJ | 8 | 1000 | 180.0 | 12.0 | 4.0 | 4.0 | 2.0 | 8.0 | 12.0 | Q2 |

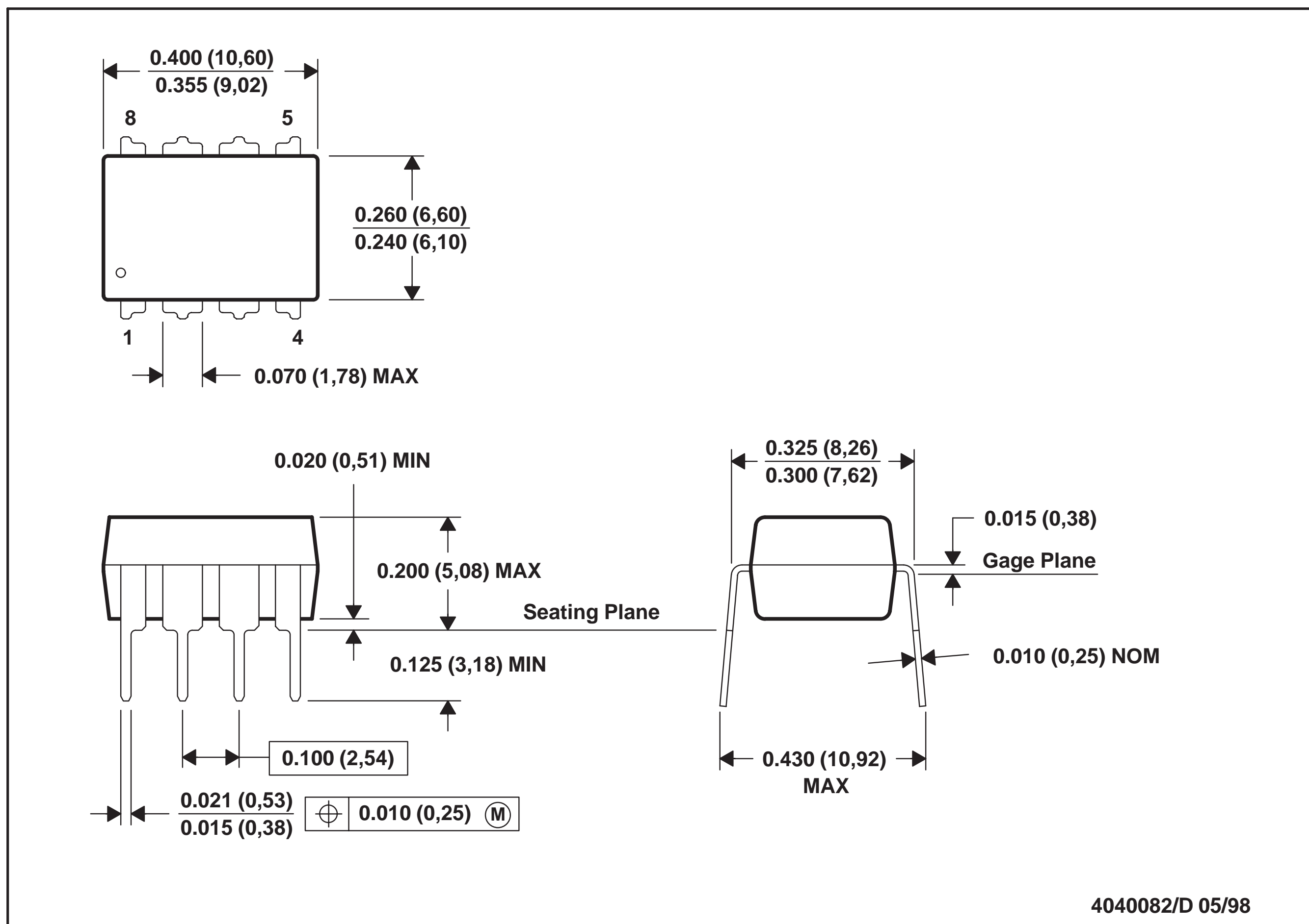
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| MC33063ADR | SOIC | D | 8 | 2500 | 343.0 | 338.0 | 21.0 |
| MC33063ADRJR | SON | DRJ | 8 | 1000 | 191.0 | 213.0 | 32.0 |
| MC34063ADR | SOIC | D | 8 | 2500 | 343.0 | 338.0 | 21.0 |
| MC34063ADRJR | SON | DRJ | 8 | 1000 | 191.0 | 213.0 | 32.0 |

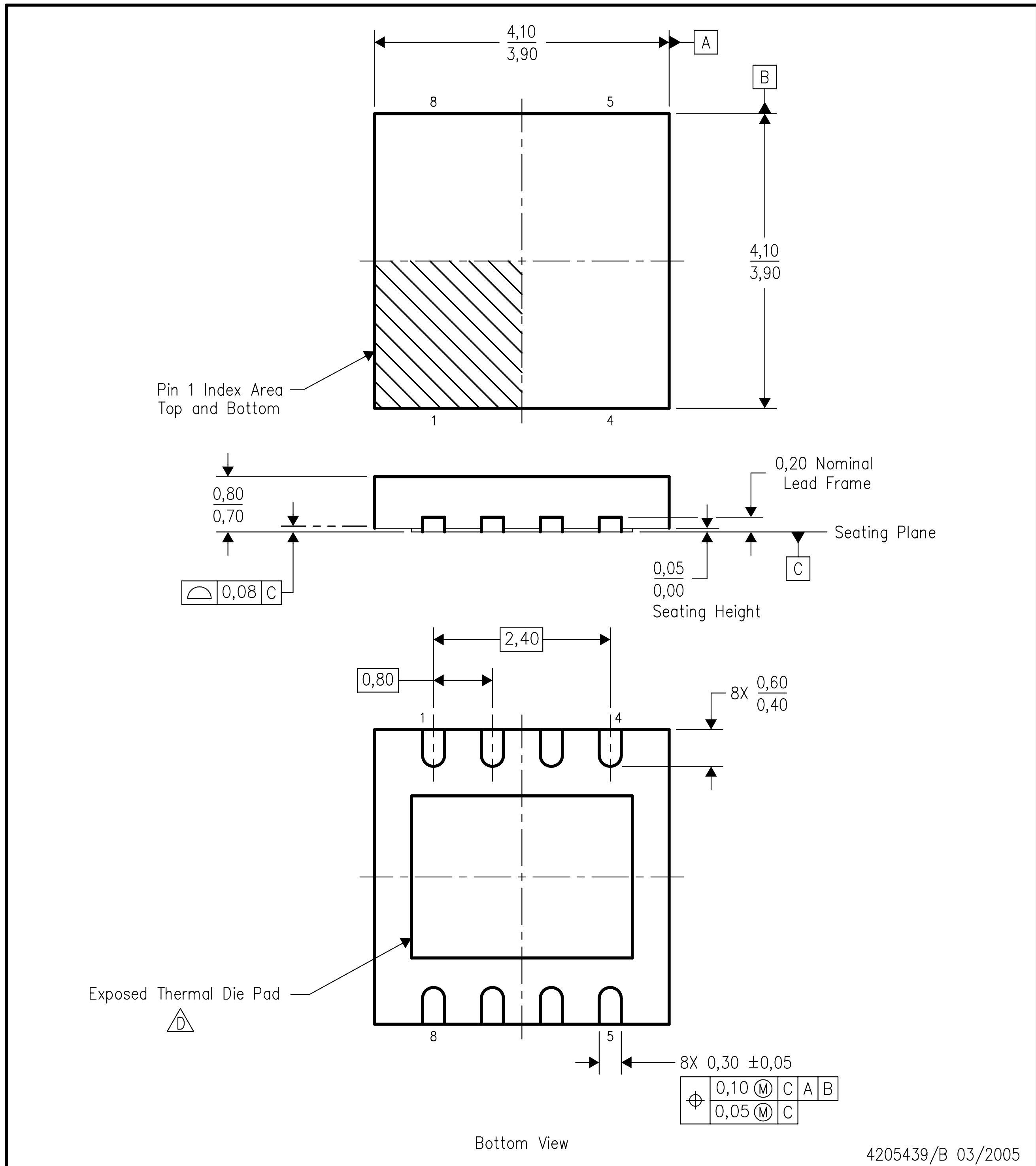
**P (R-PDIP-T8)** **PLASTIC DUAL-IN-LINE**




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

DRJ (S–PDSO–N8) PLASTIC SMALL OUTLINE




NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. SON (Small Outline No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Package complies to JEDEC MO–229 variation WGGB.

# THERMAL PAD MECHANICAL DATA

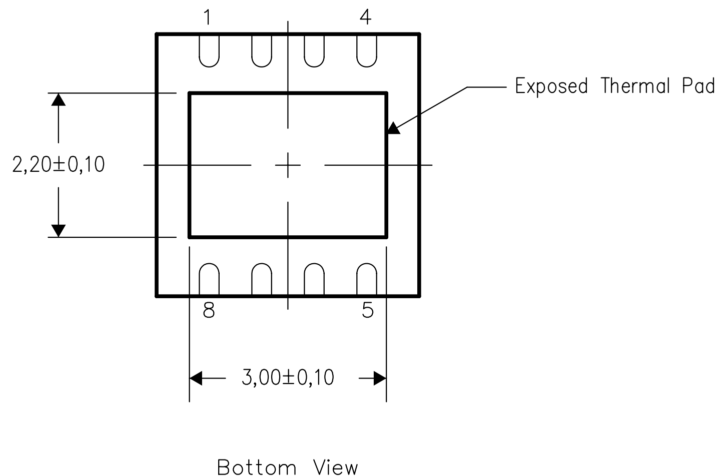
## DRJ (S–PDSO–N8)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

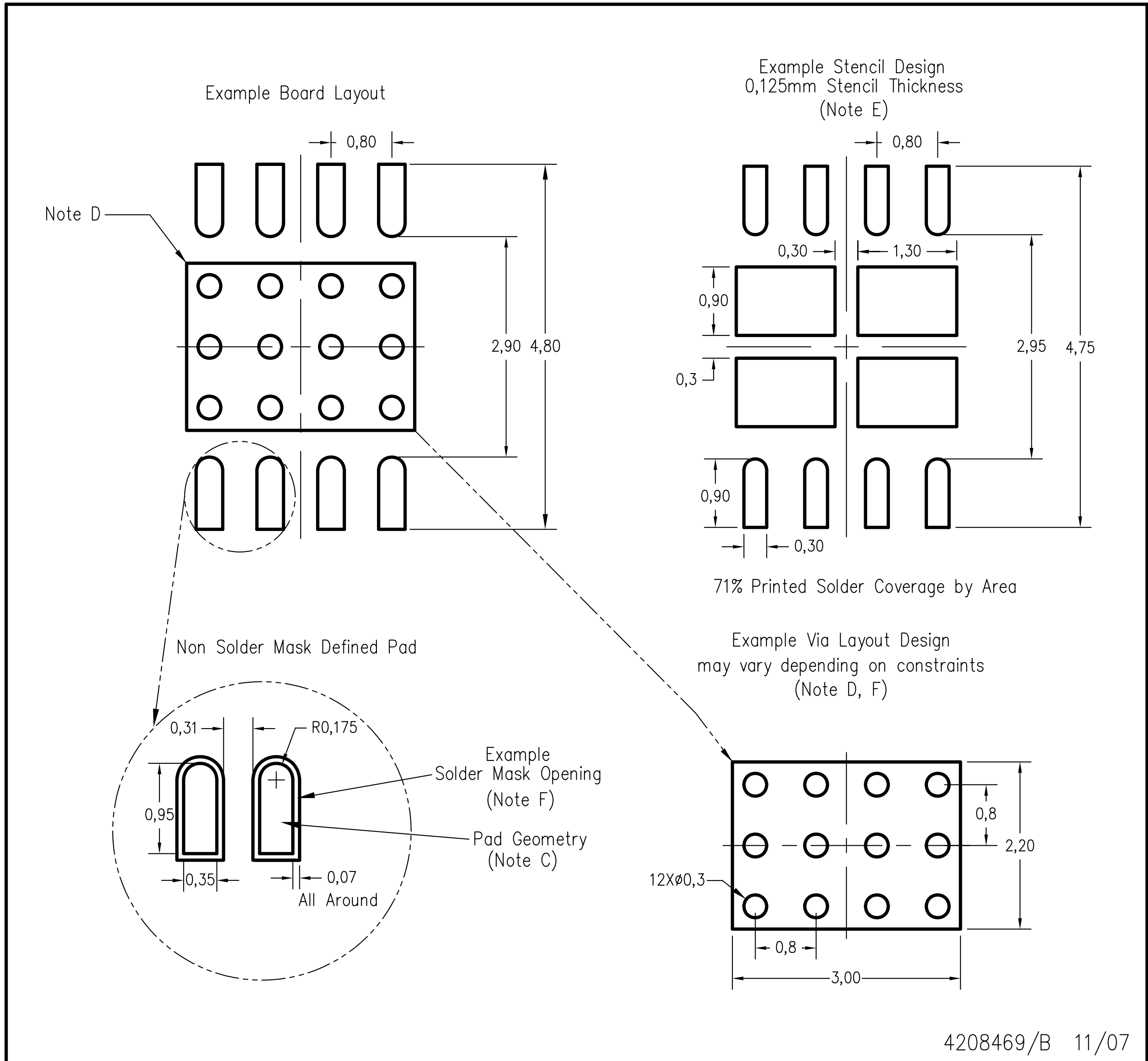
The exposed thermal pad dimensions for this package are shown in the following illustration.




NOTE: All linear dimensions are in millimeters

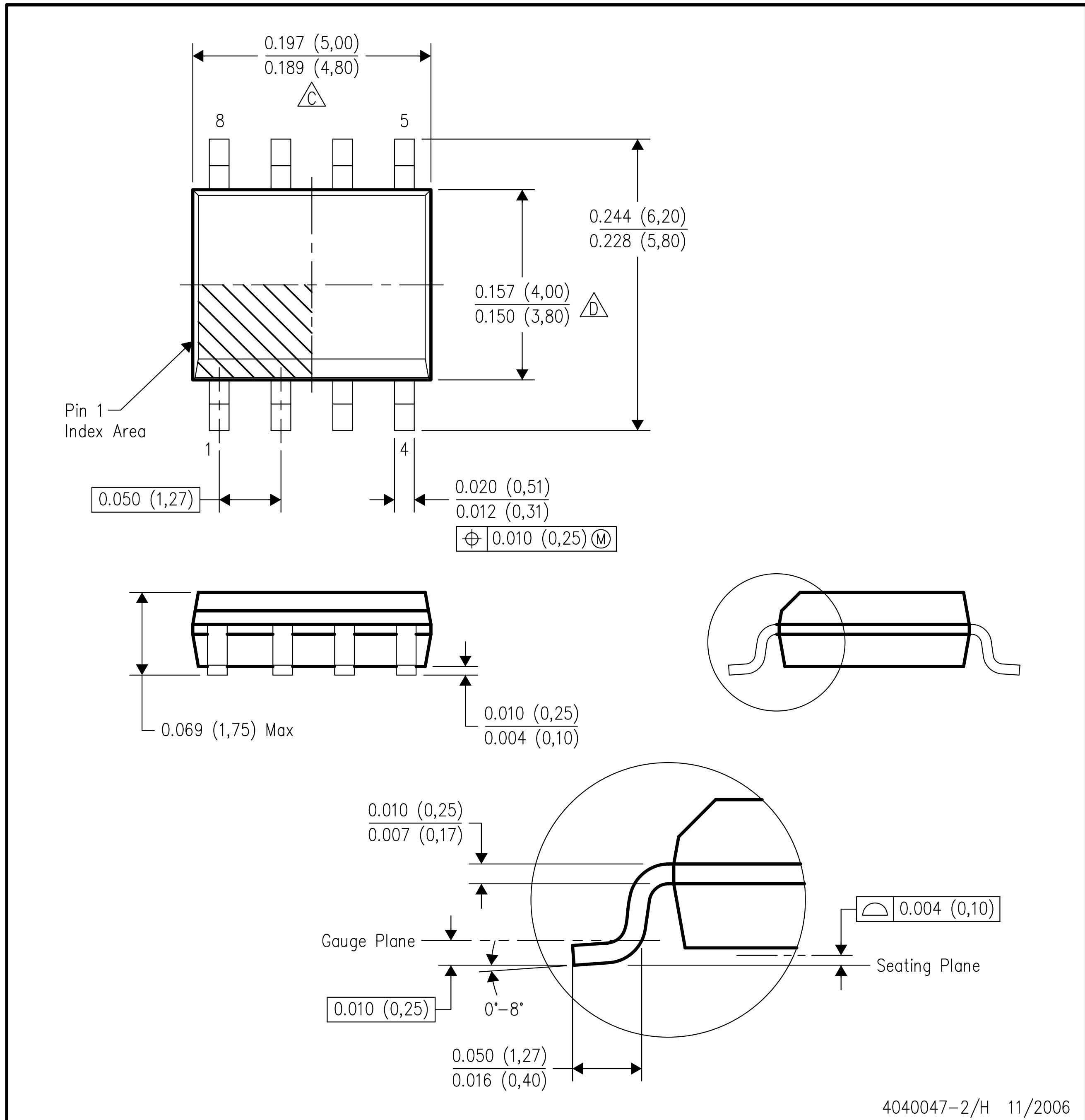
Exposed Thermal Pad Dimensions

# DRJ (S–PDSO–N8)




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances and vias tenting recommendations for vias placed in the thermal pad.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265


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