

MicroPOWER INSTRUMENTATION AMPLIFIER

Single and Dual Versions

FEATURES

- **LOW QUIESCENT CURRENT:** 175µA/chan.
- **WIDE SUPPLY RANGE:** ±1.35V to ±18V
- **LOW OFFSET VOLTAGE:** 250µV max
- **LOW OFFSET DRIFT:** 3µV/°C max
- **LOW NOISE:** 35nV/√Hz
- **LOW INPUT BIAS CURRENT:** 25nA max
- **8-PIN DIP, SO-8, MSOP-8 SURFACE-MOUNT**
DUAL: 16-Pin DIP, SO-16, SSOP-16

APPLICATIONS

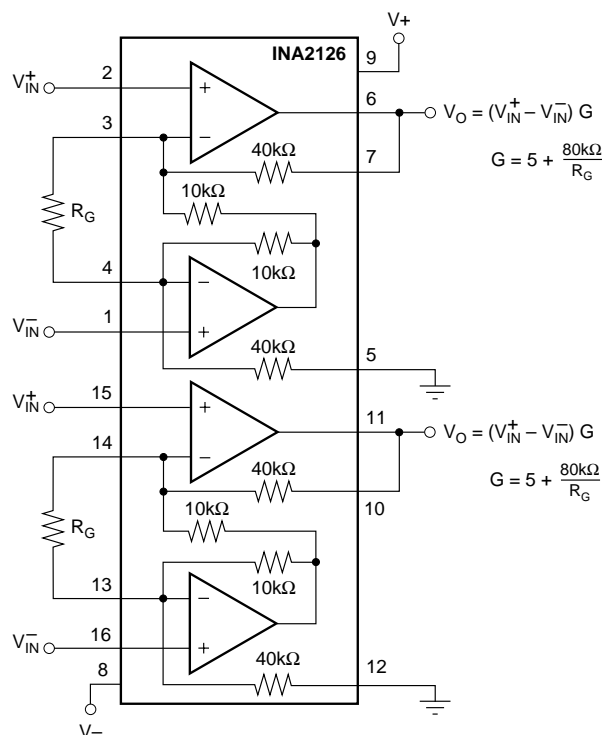
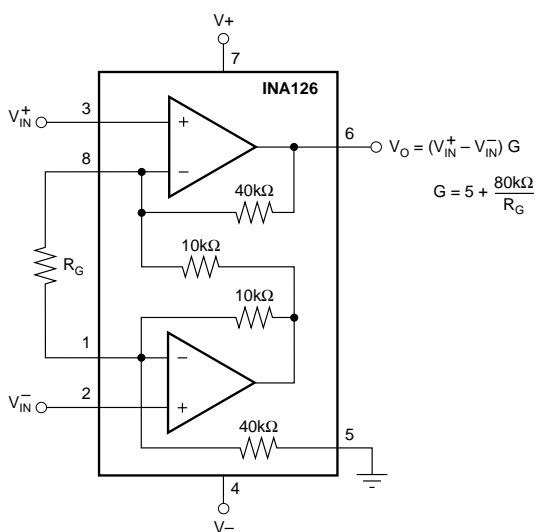
- **INDUSTRIAL SENSOR AMPLIFIER:**
Bridge, RTD, Thermocouple
- **PHYSIOLOGICAL AMPLIFIER:**
ECG, EEG, EMG
- **MULTI-CHANNEL DATA ACQUISITION**
- **PORTABLE, BATTERY OPERATED SYSTEMS**

DESCRIPTION

The INA126 and INA2126 are precision instrumentation amplifiers for accurate, low noise differential signal acquisition. Their two-op-amp design provides excellent performance with very low quiescent current (175µA/channel). This, combined with a wide operating voltage range of ±1.35V to ±18V, makes them ideal for portable instrumentation and data acquisition systems.

Gain can be set from 5V/V to 10000V/V with a single external resistor. Laser trimmed input circuitry provides low offset voltage (250µV max), low offset voltage drift (3µV/°C max) and excellent common-mode rejection.

Single version package options include 8-pin plastic DIP, SO-8 surface mount, and fine-pitch MSOP-8 surface-mount. Dual version is available in the space-saving SSOP-16 fine-pitch surface mount, SO-16, and 16-pin DIP. All are specified for the -40°C to +85°C industrial temperature range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

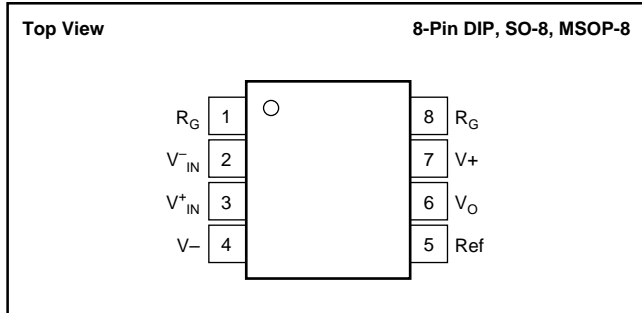
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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

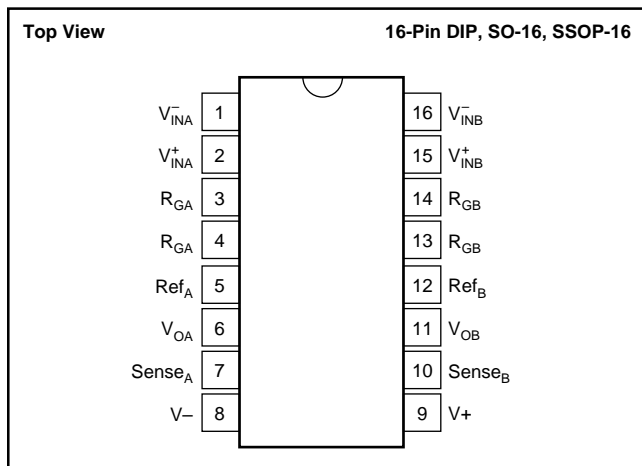
Power Supply Voltage, $V+$ to $V-$	36V
Input Signal Voltage ⁽²⁾	$(V-)-0.7$ to $(V+)+0.7V$
Input Signal Current ⁽²⁾	10mA
Output Short Circuit	Continuous
Operating Temperature	-55°C to $+125^{\circ}\text{C}$
Storage Temperature	-55°C to $+125^{\circ}\text{C}$
Lead Temperature (soldering, 10s)	$+300^{\circ}\text{C}$

NOTES: (1) Stresses above these ratings may cause permanent damage.
 (2) Input signal voltage is limited by internal diodes connected to power supplies. See text.

PIN CONFIGURATION (Single)



PIN CONFIGURATION (Dual)



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE MARKING
Single		
INA126PA INA126P	DIP-8 DIP-8	INA126PA INA126P
INA126UA INA126U	SO-8 SO-8	INA126UA INA126U
INA126EA ⁽²⁾ " INA126E ⁽²⁾ "	MSOP-8 " MSOP-8 "	A26 ⁽³⁾ " A26 ⁽³⁾ "
Dual		
INA2126PA INA2126P	DIP-16 DIP-16	INA2126PA INA2126P
INA2126UA INA2126U	SO-16 SO-16	INA2126UA INA2126U
INA2126EA ⁽²⁾ " INA2126E ⁽²⁾ "	SSOP-16 " SSOP-16 "	INA2126EA " INA2126E "

NOTES: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com. (2) MSOP-8 and SSOP-16 packages are available only on 250 or 2500 piece reels. (3) Grade designation is marked on reel.

ELECTRICAL CHARACTERISTICS

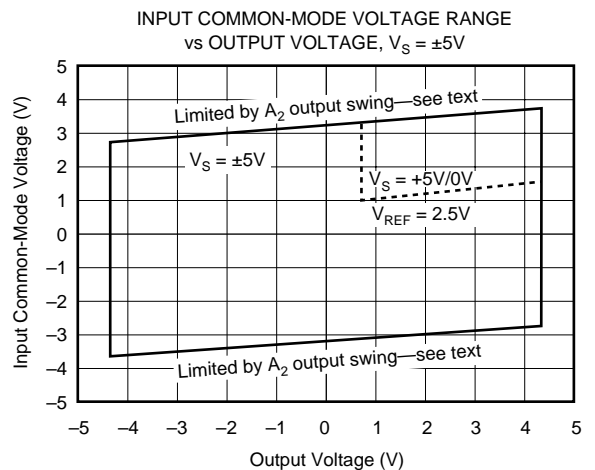
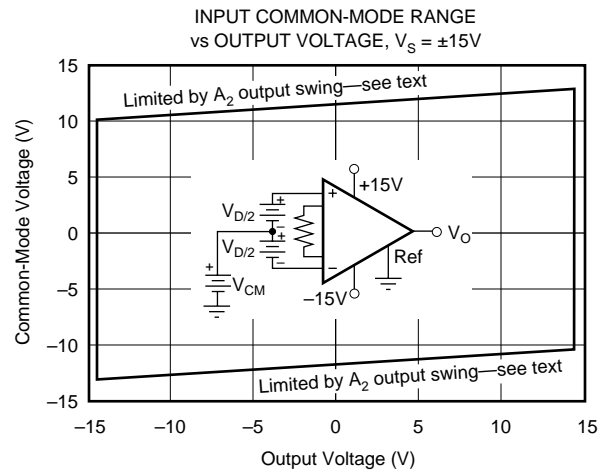
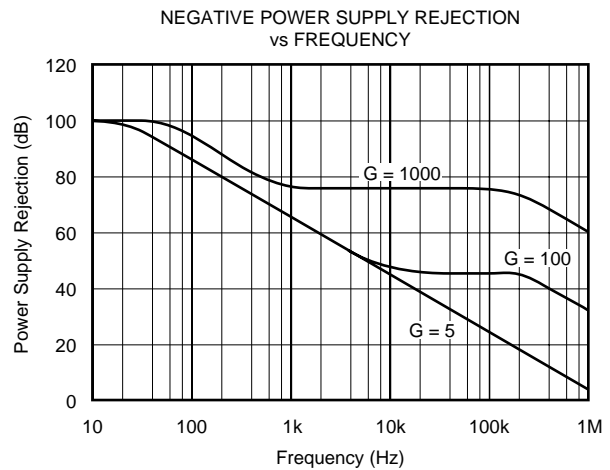
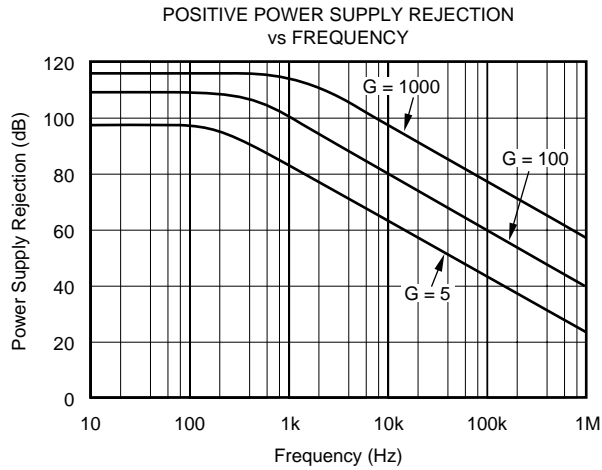
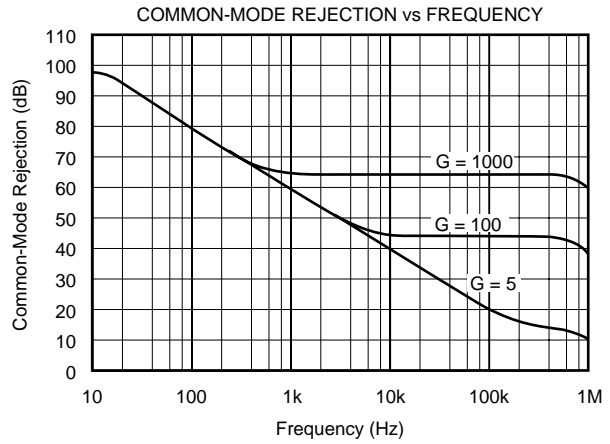
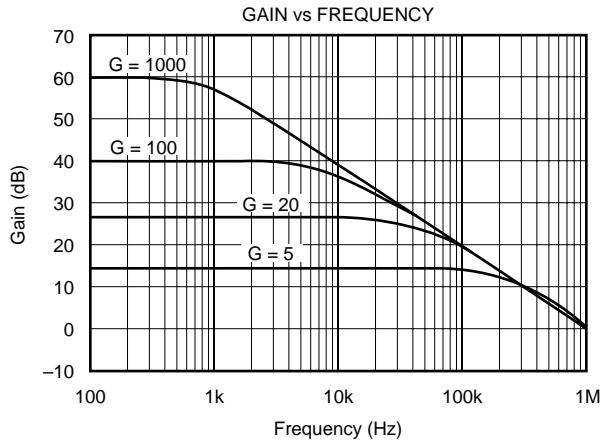
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 25\text{k}\Omega$, unless otherwise noted.

PARAMETER	CONDITIONS	INA126P, U, E INA2126P, U, E			INA126PA, UA, EA INA2126PA, UA, EA			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
INPUT									
Offset Voltage, RTI vs Temperature	$V_S = \pm 1.35\text{V to } \pm 18\text{V}$		± 100	± 250		± 150	± 500	μV	
vs Power Supply (PSRR)			± 0.5	± 3		*	± 5	$\mu\text{V}/^\circ\text{C}$	
Input Impedance				5	15		*	50	$\mu\text{V}/\text{V}$
Safe Input Voltage		$R_S = 0$	$(V^-) - 0.5$		$(V^+) + 0.5$	*		*	$\Omega \parallel \text{pF}$
	$R_S = 1\text{k}\Omega$	$(V^-) - 10$		$(V^+) + 10$	*		*	V	
Common-Mode Voltage Range	$V_O = 0\text{V}$	± 11.25	± 11.5		*	*		V	
Channel Separation (dual)	$G = 5, \text{dc}$		130					dB	
Common-Mode Rejection INA2126U (dual SO-16)	$R_S = 0, V_{\text{CM}} = \pm 11.25\text{V}$	83	94		74	90		dB	
		80	94					dB	
INPUT BIAS CURRENT									
vs Temperature			-10	-25		*	-50	nA	
Offset Current vs Temperature			± 30			*		$\text{pA}/^\circ\text{C}$	
			± 0.5	± 2		*	± 5	nA	
			± 10			*		$\text{pA}/^\circ\text{C}$	
GAIN									
Gain Equation			$G = 5 \text{ to } 10\text{k}$			*		V/V	
Gain Error			$G = 5 + 80\text{k}\Omega/R_G$			*		V/V	
vs Temperature	$V_O = \pm 14\text{V}, G = 5$		± 0.02	± 0.1		*	± 0.18	%	
Gain Error vs Temperature	$G = 5$		± 2	± 10		*	*	$\text{ppm}/^\circ\text{C}$	
Gain Error vs Temperature	$V_O = \pm 12\text{V}, G = 100$		± 0.2	± 0.5		*	± 1	%	
Nonlinearity	$G = 100, V_O = \pm 14\text{V}$		± 25	± 100		*	*	$\text{ppm}/^\circ\text{C}$	
			± 0.002	± 0.012		*	*	%	
NOISE									
Voltage Noise, $f = 1\text{kHz}$			35			*		$\text{nV}/\sqrt{\text{Hz}}$	
$f = 100\text{Hz}$			35			*		$\text{nV}/\sqrt{\text{Hz}}$	
$f = 10\text{Hz}$			45			*		$\text{nV}/\sqrt{\text{Hz}}$	
$f_B = 0.1\text{Hz to } 10\text{Hz}$			0.7			*		μV_{PP}	
Current Noise, $f = 1\text{kHz}$			60			*		$\text{fA}/\sqrt{\text{Hz}}$	
$f_B = 0.1\text{Hz to } 10\text{Hz}$			2			*		pA_{PP}	
OUTPUT									
Voltage, Positive	$R_L = 25\text{k}\Omega$	$(V^+) - 0.9$	$(V^+) - 0.75$		*	*		V	
Negative	$R_L = 25\text{k}\Omega$	$(V^-) + 0.95$	$(V^-) + 0.8$		*	*		V	
Short-Circuit Current	Short-Circuit to Ground		$+10/-5$			*		mA	
Capacitive Load Drive			1000			*		pF	
FREQUENCY RESPONSE									
Bandwidth, -3dB	$G = 5$		200			*		kHz	
	$G = 100$		9			*		kHz	
	$G = 500$		1.8			*		kHz	
Slew Rate	$V_O = \pm 10\text{V}, G = 5$		0.4			*		V/ μs	
Settling Time, 0.01%	10V Step, $G = 5$		30			*		μs	
	10V Step, $G = 100$		160			*		μs	
	10V Step, $G = 500$		1500			*		μs	
Overload Recovery	50% Input Overload		4			*		μs	
POWER SUPPLY									
Voltage Range		± 1.35	± 15	± 18	*	*	*	V	
Current (per channel)	$I_O = 0$		± 175	± 200		*	*	μA	
TEMPERATURE RANGE									
Specification Range		-40		+85	*		*	$^\circ\text{C}$	
Operation Range		-55		+125	*		*	$^\circ\text{C}$	
Storage Range		-55		+125	*		*	$^\circ\text{C}$	
Thermal Resistance, θ_{JA}									
8-Pin DIP			100			*		$^\circ\text{C}/\text{W}$	
SO-8 Surface-Mount			150			*		$^\circ\text{C}/\text{W}$	
MSOP-8 Surface-Mount			200			*		$^\circ\text{C}/\text{W}$	
16-Pin DIP (dual)			80			*		$^\circ\text{C}/\text{W}$	
SO-16 (dual)			100			*		$^\circ\text{C}/\text{W}$	
SSOP-16 (dual)			100			*		$^\circ\text{C}/\text{W}$	

* Specification same as INA126P, INA126U, INA126E; INA2126P, INA2126U, INA2126E.

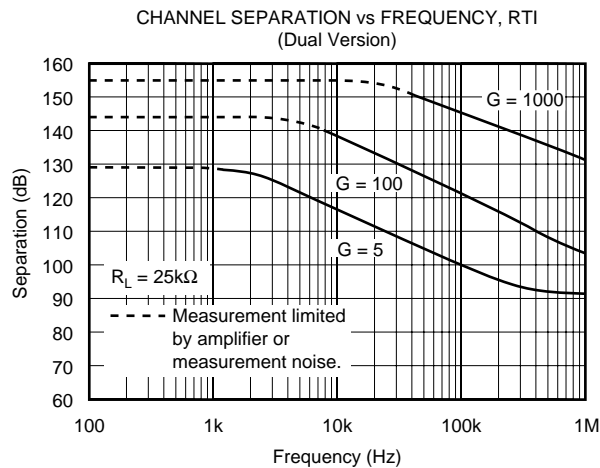
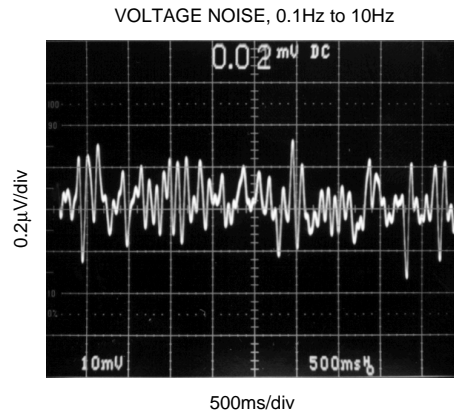
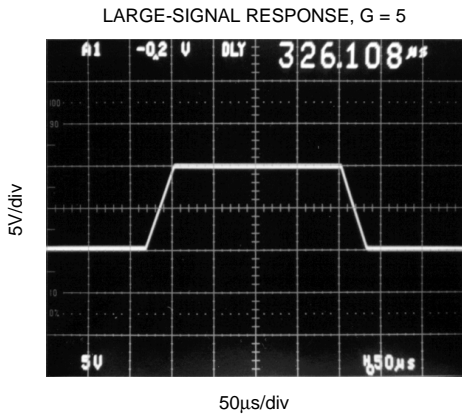
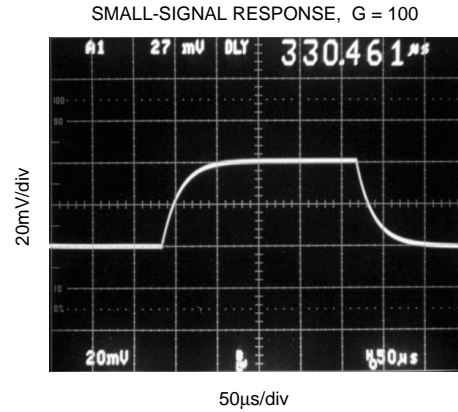
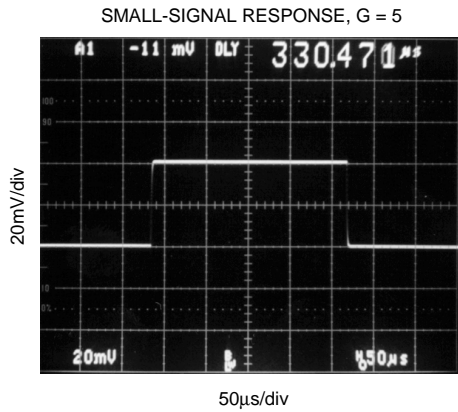
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$ and $V_S = \pm 15\text{V}$, unless otherwise noted.



TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$ and $V_S = \pm 15\text{V}$, unless otherwise noted.



INPUT BIAS CURRENT RETURN

The input impedance of the INA126/2126 is extremely high—approximately $10^9\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically -10nA (current flows out of the input terminals). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

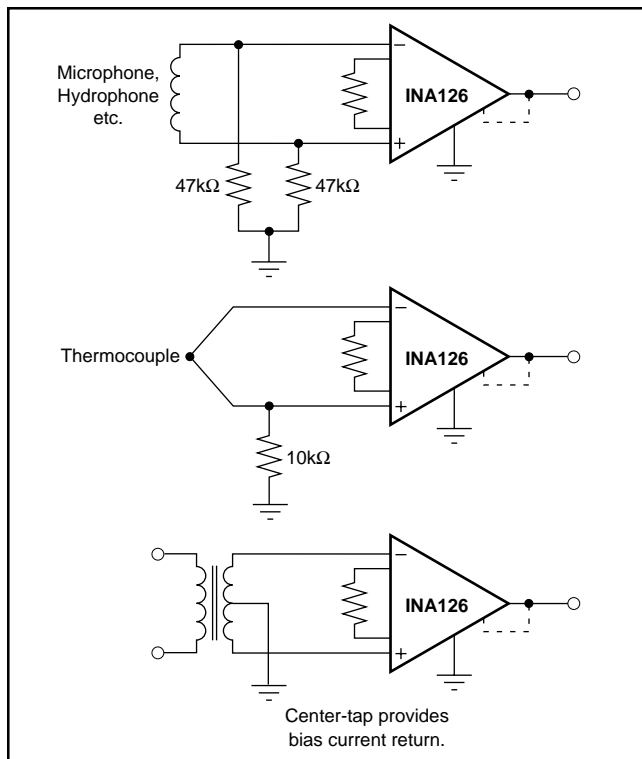


FIGURE 3. Providing an Input Common-Mode Current Path.

INPUT COMMON-MODE RANGE

The input common-mode range of the INA126/2126 is shown in the typical characteristic curves. The common-mode range is limited on the negative side by the output voltage swing of A_2 , an internal circuit node that cannot be measured on an external pin. The output voltage of A_2 can be expressed as:

$$V_{O2} = 1.25 V_{IN}^- - (V_{IN}^+ - V_{IN}^-) (10\text{k}\Omega/R_G) \quad (2)$$

(Voltages referred to Ref terminal, pin 5)

The internal op amp A_2 is identical to A_1 and its output swing is limited to typically 0.7V from the supply rails. When the input common-mode range is exceeded (A_2 's output is saturated), A_1 can still be in linear operation and respond to changes in the non-inverting input voltage. The output voltage, however, will be invalid.

LOW VOLTAGE OPERATION

The INA126/2126 can be operated on power supplies as low as $\pm 1.35\text{V}$. Performance remains excellent with power supplies ranging from $\pm 1.35\text{V}$ to $\pm 18\text{V}$. Most parameters vary only slightly throughout this supply voltage range—see typical characteristic curves. Operation at very low supply voltage requires careful attention to ensure that the common-mode voltage remains within its linear range. See “Input Common-Mode Voltage Range.”

The INA126/2126 can be operated from a single power supply with careful attention to input common-mode range, output voltage swing of both op amps and the voltage applied to the Ref terminal. Figure 4 shows a bridge amplifier circuit operated from a single $+5\text{V}$ power supply. The bridge provides an input common-mode voltage near 2.5V , with a relatively small differential voltage.

INPUT PROTECTION

The inputs are protected with internal diodes connected to the power supply rails. These diodes will clamp the applied signal to prevent it from exceeding the power supplies by more than approximately 0.7V . If the signal source voltage can exceed the power supplies, the source current should be limited to less than 10mA . This can generally be done with a series resistor. Some signal sources are inherently current-limited and do not require limiting resistors.

CHANNEL CROSSTALK—DUAL VERSION

The two channels of the INA2126 are completely independent, including all bias circuitry. At DC and low frequency there is virtually no signal coupling between channels. Crosstalk increases with frequency and is dependent on circuit gain, source impedance and signal characteristics.

As source impedance increases, careful circuit layout will help achieve lowest channel crosstalk. Most crosstalk is produced by capacitive coupling of signals from one channel to the input section of the other channel. To minimize coupling, separate the input traces as far as practical from any signals associated with the opposite channel. A grounded guard trace surrounding the inputs helps reduce stray coupling between channels. Carefully balance the stray capacitance of each input to ground, and run the differential inputs of each channel parallel to each other, or directly adjacent on top and bottom side of a circuit board. Stray coupling then tends to produce a common-mode signal that is rejected by the IA's input.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
INA126E/250	ACTIVE	MSOP	DGK	8	250	TBD	CU NIPDAU	Level-3-220C-168 HR
INA126E/2K5	ACTIVE	MSOP	DGK	8	2500	TBD	CU NIPDAU	Level-3-220C-168 HR
INA126EA/250	ACTIVE	MSOP	DGK	8	250	TBD	CU NIPDAU	Level-3-220C-168 HR
INA126EA/2K5	ACTIVE	MSOP	DGK	8	2500	TBD	CU NIPDAU	Level-3-220C-168 HR
INA126P	ACTIVE	PDIP	P	8	50	TBD	Call TI	Level-NA-NA-NA
INA126PA	ACTIVE	PDIP	P	8	50	TBD	Call TI	Level-NA-NA-NA
INA126U	ACTIVE	SOIC	D	8	100	TBD	CU SNPB	Level-2-220C-1 YEAR
INA126U/2K5	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-2-220C-1 YEAR
INA126UA	ACTIVE	SOIC	D	8	100	TBD	CU SNPB	Level-2-220C-1 YEAR
INA126UA/2K5	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-2-220C-1 YEAR
INA2126E/250	ACTIVE	SSOP/ QSOP	DBQ	16	250	TBD	CU NIPDAU	Level-3-220C-168 HR
INA2126E/2K5	ACTIVE	SSOP/ QSOP	DBQ	16	2500	TBD	CU NIPDAU	Level-3-220C-168 HR
INA2126E/2K5G4	ACTIVE	SSOP/ QSOP	DBQ	16		TBD	Call TI	Call TI
INA2126EA/250	ACTIVE	SSOP/ QSOP	DBQ	16	250	TBD	CU NIPDAU	Level-3-220C-168 HR
INA2126EA/2K5	ACTIVE	SSOP/ QSOP	DBQ	16	2500	TBD	CU NIPDAU	Level-3-220C-168 HR
INA2126EA/2K5G4	ACTIVE	SSOP/ QSOP	DBQ	16		TBD	Call TI	Call TI
INA2126P	ACTIVE	PDIP	N	16	25	TBD	Call TI	Level-NA-NA-NA
INA2126PA	ACTIVE	PDIP	N	16	25	TBD	Call TI	Level-NA-NA-NA
INA2126U	ACTIVE	SOIC	D	16	48	TBD	CU SNPB	Level-3-220C-168 HR
INA2126U/2K5	ACTIVE	SOIC	D	16	2500	TBD	CU SNPB	Level-3-220C-168 HR
INA2126UA	ACTIVE	SOIC	D	16	48	TBD	CU SNPB	Level-3-220C-168 HR
INA2126UA/2K5	ACTIVE	SOIC	D	16	2500	TBD	CU SNPB	Level-3-220C-168 HR
INA2126UA/2K5E4	PREVIEW	SOIC	D	16	2500	TBD	Call TI	Call TI
INA2126UAE4	PREVIEW	SOIC	D	16	48	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder

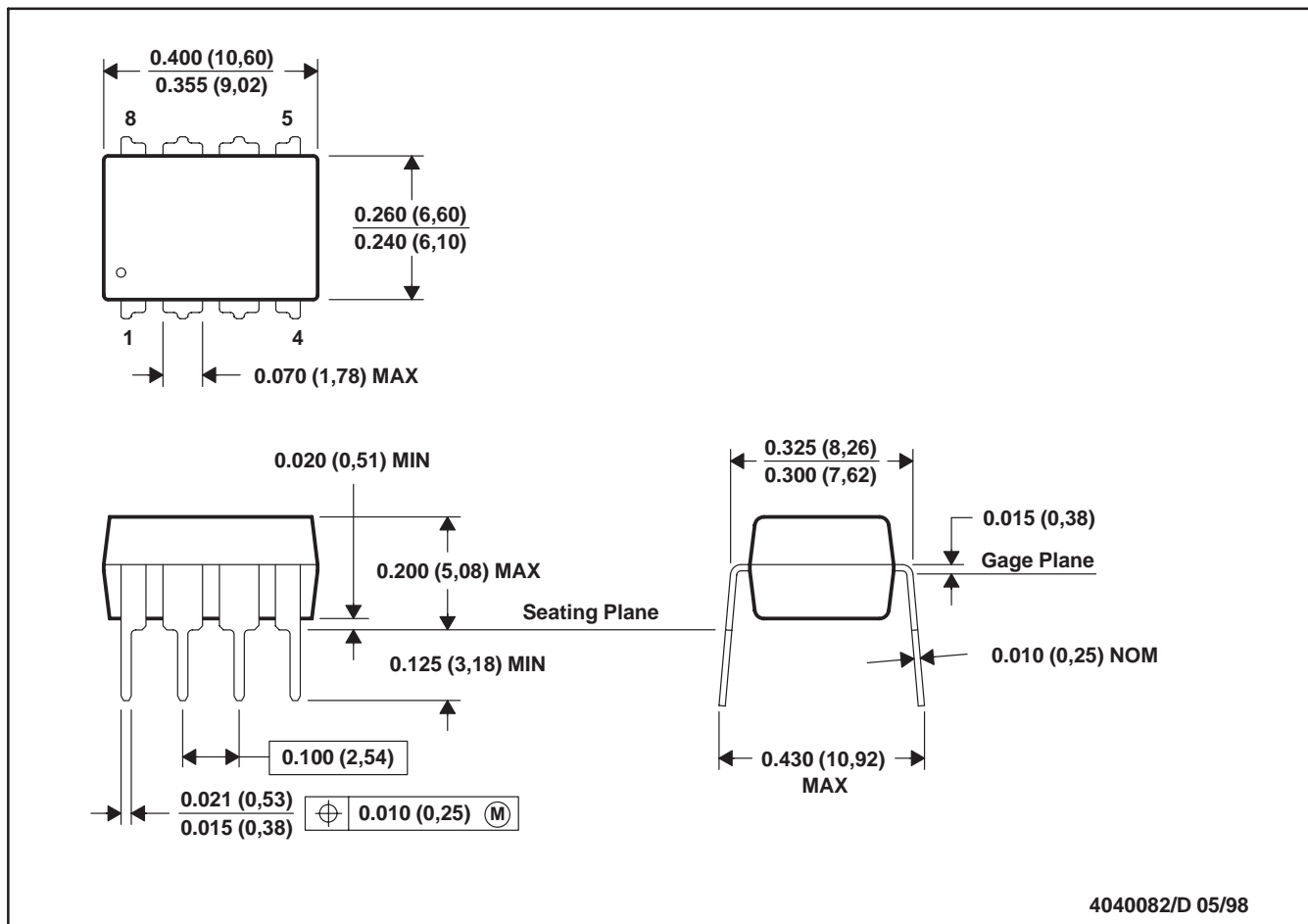
temperature.

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P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



4040082/D 05/98

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

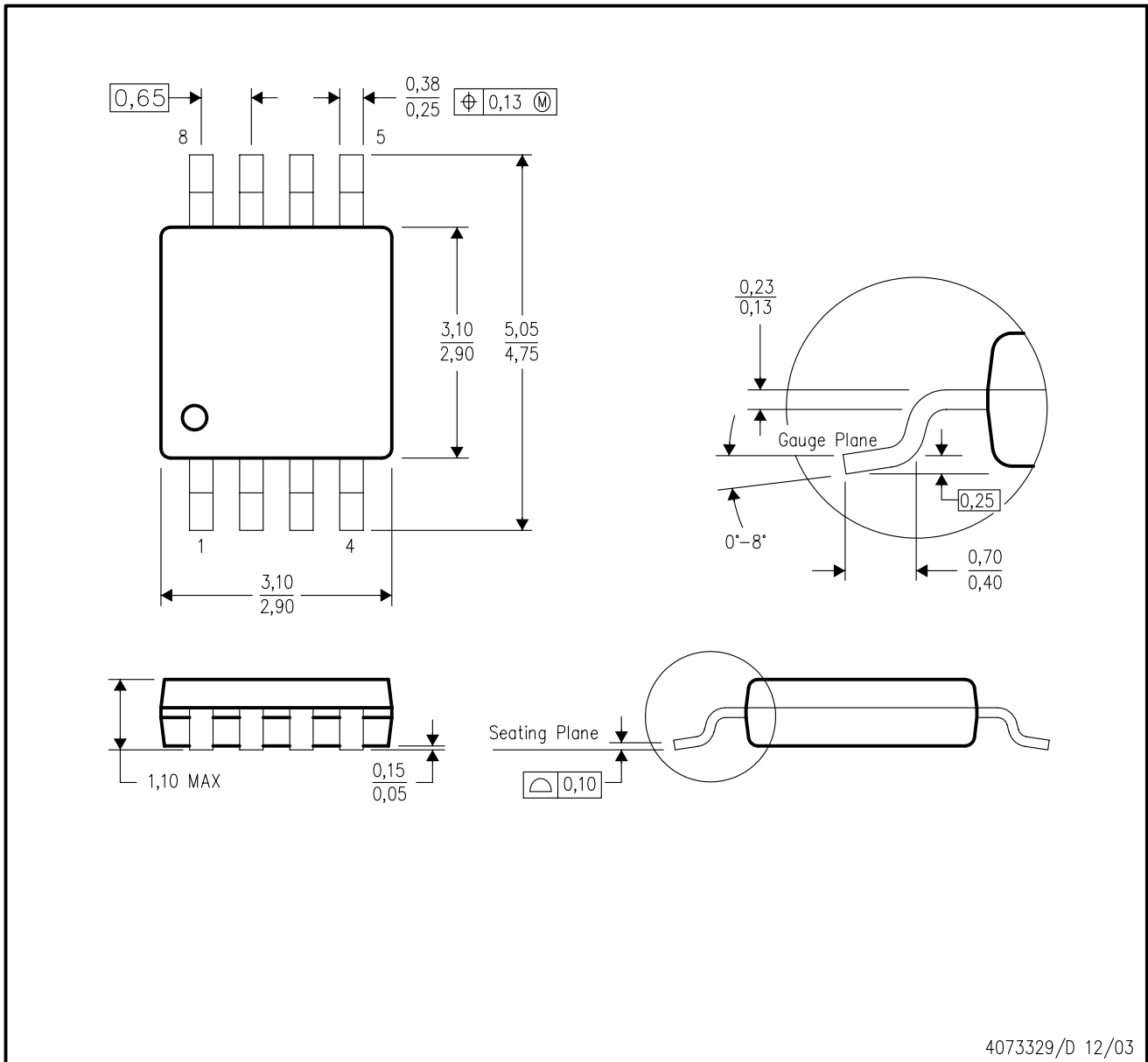
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGK (S-PDSO-G8)

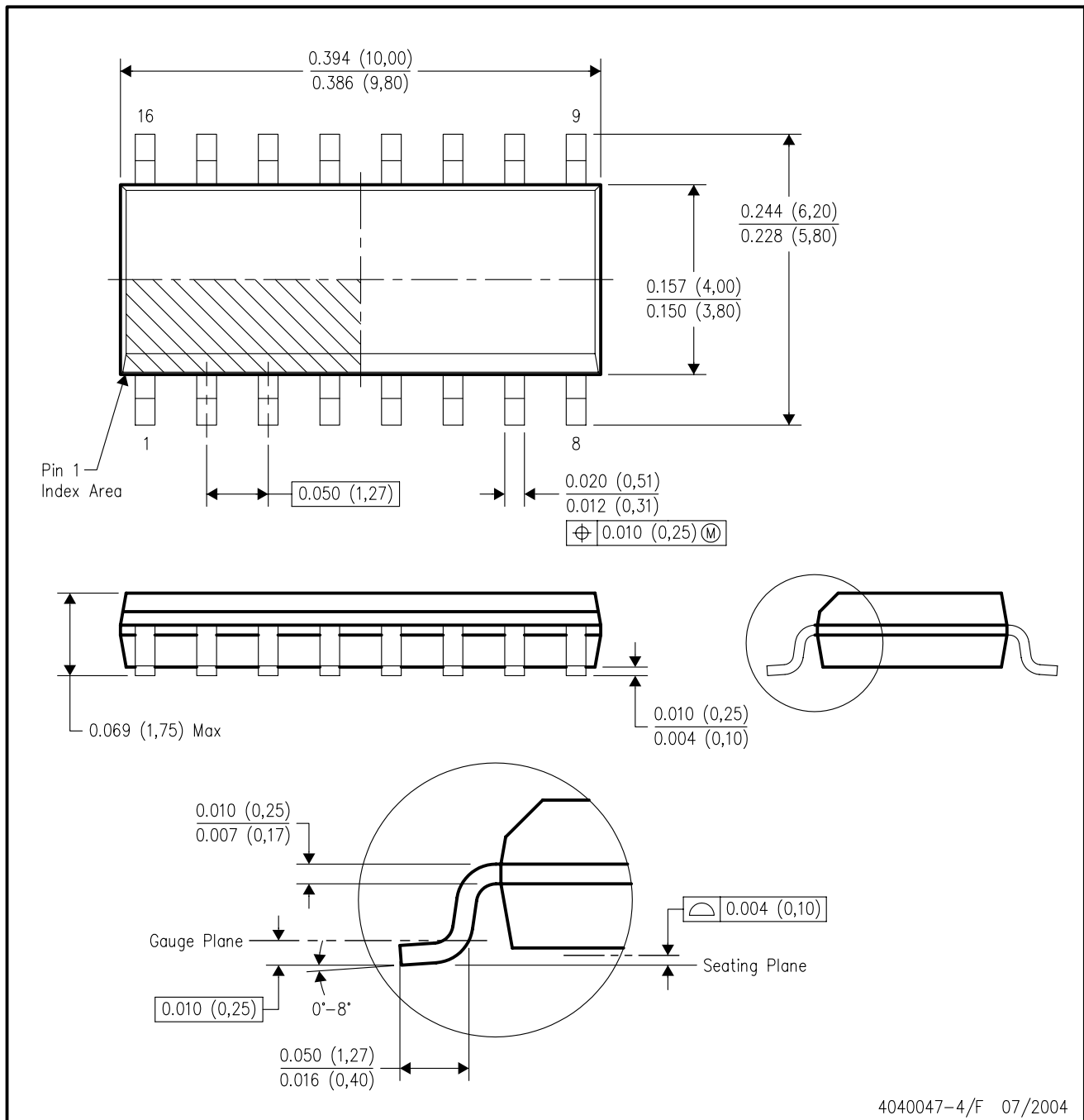
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation AA.

D (R-PDSO-G16)

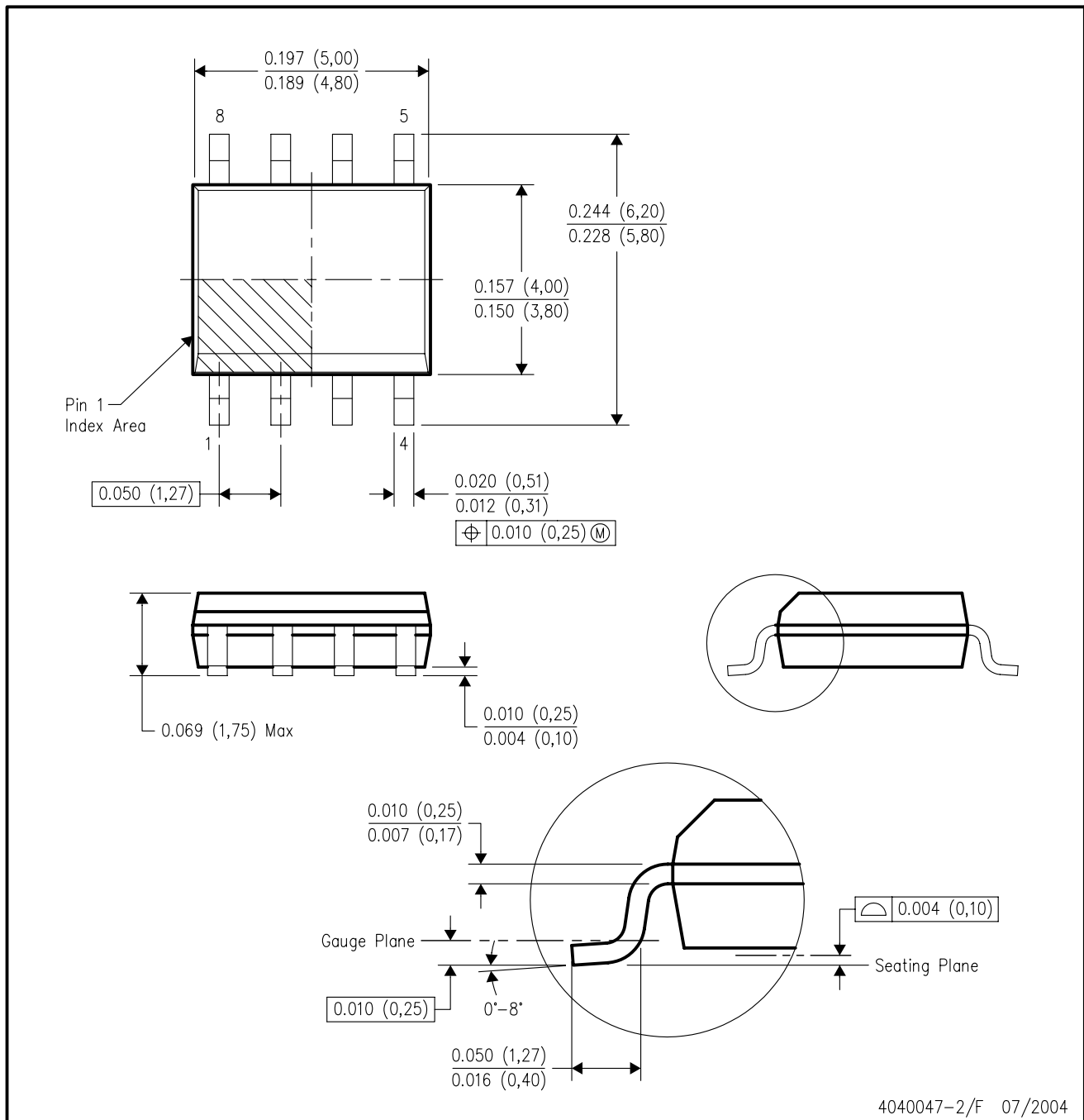
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AC.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AA.

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