



**DAC7734**

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## 16-Bit, Quad Voltage Output, Serial Input DIGITAL-TO-ANALOG CONVERTER

### FEATURES

- **LOW POWER: 200mW**
- **UNIPOLAR OR BIPOLAR OPERATION**
- **SINGLE SUPPLY OUTPUT RANGE: +10V**
- **DUAL SUPPLY OUTPUT RANGE:  $\pm 10V$**
- **SETTLING TIME: 10 $\mu$ s to 0.003%**
- **16-BIT MONOTONICITY:  $-40^{\circ}C$  to  $+85^{\circ}C$**
- **PROGRAMMABLE RESET TO MID-SCALE OR ZERO-SCALE**
- **DOUBLE-BUFFERED DATA INPUTS**
- **$\pm 1$  LSB DNL:  $-40^{\circ}C$  to  $+85^{\circ}C$**

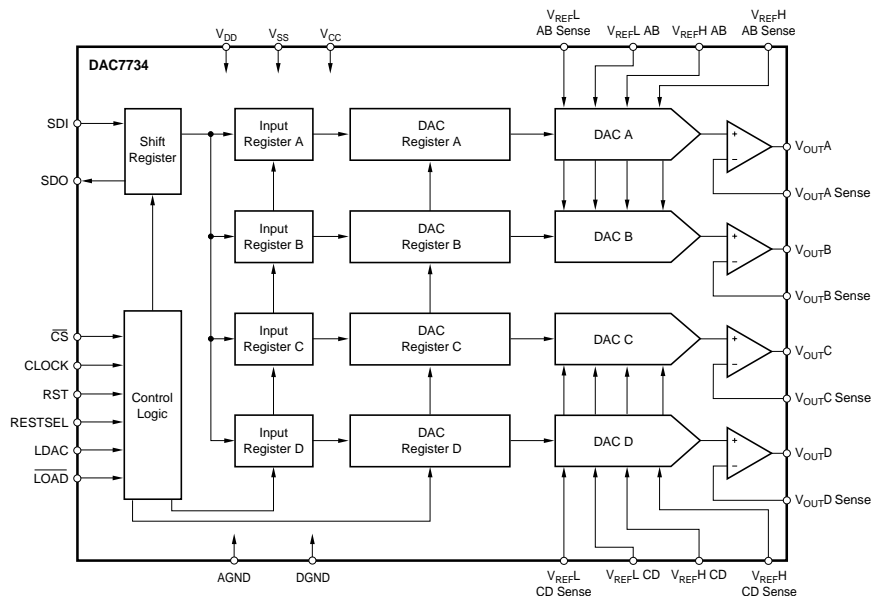
### APPLICATIONS

- **PROCESS CONTROL**
- **ATE PIN ELECTRONICS**
- **CLOSED-LOOP SERVO-CONTROL**
- **MOTOR CONTROL**
- **DATA ACQUISITION SYSTEMS**
- **DAC-PER-PIN PROGRAMMERS**

### DESCRIPTION

The DAC7734 is a 16-bit, quad voltage output, digital-to-analog converter with guaranteed 16-bit monotonic performance over the specified temperature range. It accepts 24-bit serial input data, has double-buffered DAC input logic (allowing simultaneous update of all DACs), and provides a serial data output for daisy chaining multiple DACs. Programmable asynchronous reset clears all registers to a mid-scale code of 8000<sub>H</sub> or to a zero-scale of 0000<sub>H</sub>. The DAC7734 can operate from a single +15V supply or from +15V and -15V, and +5V supplies.

Low power and small size per DAC make the DAC7734 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo-control. The DAC7734 is available in a 48-lead SSOP package and offers guaranteed specifications over the  $-40^{\circ}C$  to  $+85^{\circ}C$  temperature range.



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 Twx: 910-952-1111 • Internet: <http://www.burr-brown.com/> • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS (Dual Supply)

At  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{CC} = +15V$ ,  $V_{DD} = +5V$ ,  $V_{SS} = -15V$ ,  $V_{REFH} = +10V$ , and  $V_{REFL} = -10V$ , unless otherwise noted.

| PARAMETER  | CONDITIONS   | DAC7734E           |            |                    | DAC7734EB |     |     | DAC7734EC |                    |                    | UNITS          |
|--|--|--------------------|------------|--------------------|-----------|-----|-----|-----------|--------------------|--------------------|----------------|
|  |  | MIN                | TYP        | MAX                | MIN       | TYP | MAX | MIN       | TYP                | MAX                |                |
| <b>ACCURACY</b>  |  |                    |            |                    |           |     |     |           |                    |                    |                |
| Linearity Error (INL)<br>$T_{MIN}$ to $T_{MAX}$              | $T = 25^{\circ}C$                                  |                    |            | $\pm 3$<br>$\pm 4$ |           |     | *   |           |                    | $\pm 2$<br>$\pm 3$ | LSB<br>LSB     |
| Linearity Match  |  |                    | $\pm 4$    |                    |           | *   |     |           | $\pm 2$            |                    | LSB            |
| Differential Linearity Error (DNL)<br>$T_{MIN}$ to $T_{MAX}$ | $T = 25^{\circ}C$                                  |                    |            | $\pm 3$<br>$\pm 3$ |           |     |     |           | $\pm 2$<br>$\pm 2$ |                    | LSB<br>LSB     |
| Monotonicity, $T_{MIN}$ to $T_{MAX}$                         |  | 14                 |            |                    | 15        |     |     | 16        |                    |                    | Bits           |
| Bipolar Zero Error   | $T = 25^{\circ}C$                                  |                    | $\pm 0.01$ | $\pm 0.025$        |           |     | *   |           |                    | *                  | % of FSR       |
| Bipolar Zero Error, $T_{MIN}$ to $T_{MAX}$                   |  |                    |            | $\pm 0.05$         |           |     | *   |           |                    | *                  | % of FSR       |
| Full-Scale Error   | $T = 25^{\circ}C$                                  |                    |            | $\pm 0.025$        |           |     | *   |           |                    | *                  | % of FSR       |
| Full-Scale Error, $T_{MIN}$ to $T_{MAX}$                     |  |                    |            | $\pm 0.05$         |           |     | *   |           |                    | *                  | % of FSR       |
| Bipolar Zero Matching  | Channel-to-Channel Matching                        |                    |            | $\pm 0.024$        |           |     | *   |           |                    | *                  | % of FSR       |
| Full-Scale Matching  | Channel-to-Channel Matching                        |                    |            | $\pm 0.024$        |           |     | *   |           |                    | *                  | % of FSR       |
| Power Supply Rejection Ratio (PSRR)                          | At Full Scale                                      |                    |            | 25                 |           |     | *   |           |                    | *                  | ppm/V          |
| <b>ANALOG OUTPUT</b>   |  |                    |            |                    |           |     |     |           |                    |                    |                |
| Voltage Output   |  | $V_{REFL}$         |            | $V_{REFH}$         | *         |     | *   | *         |                    | *                  | V              |
| Output Current   |  | $\pm 5$            |            |                    | *         |     | *   | *         |                    | *                  | mA             |
| Maximum Load Capacitance                                     |  |                    | 500        |                    |           | *   |     | *         | *                  | *                  | pF             |
| Short-Circuit Current  |  |                    | $\pm 20$   |                    |           | *   |     | *         | *                  | *                  | mA             |
| Short-Circuit Duration                                       | To $V_{SS}$ , $V_{CC}$ or GND                      |                    | Indefinite |                    |           | *   |     | *         | *                  | *                  |                |
| <b>REFERENCE INPUT</b>                                       |  |                    |            |                    |           |     |     |           |                    |                    |                |
| Ref High Input Voltage Range                                 |  | $V_{REFL} + 1.25$  |            | +10                | *         |     | *   | *         |                    | *                  | V              |
| Ref Low Input Voltage Range                                  |  | -10                |            | $V_{REFH} - 1.25$  | *         |     | *   | *         |                    | *                  | V              |
| Ref High Input Current                                       |  | -0.3               |            | 2.6                |           | *   |     | *         | *                  | *                  | mA             |
| Ref Low Input Current  |  | -3.2               |            | -0.3               |           | *   |     | *         | *                  | *                  | mA             |
| <b>DYNAMIC PERFORMANCE</b>                                   |  |                    |            |                    |           |     |     |           |                    |                    |                |
| Settling Time  | To $\pm 0.003\%$ , 20V Output Step<br>See Figure 5 |                    | 9          | 11                 |           | *   | *   |           | *                  | *                  | $\mu s$        |
| Channel-to-Channel Crosstalk                                 |  |                    | 0.5        |                    |           | *   |     |           | *                  | *                  | LSB            |
| Digital Feedthrough  |  |                    | 2          |                    |           | *   |     |           | *                  | *                  | nV-s           |
| Output Noise Voltage   | $f = 10kHz$  |                    | 60         |                    |           | *   |     |           | *                  | *                  | $nV/\sqrt{Hz}$ |
| <b>DIGITAL INPUT</b>   |  |                    |            |                    |           |     |     |           |                    |                    |                |
| $V_{IH}$   |  | $0.7 \cdot V_{DD}$ |            | $V_{DD}$           | *         |     |     | *         |                    | *                  | V              |
| $V_{IL}$   |  | 0                  |            | $0.3 \cdot V_{DD}$ |           |     |     | *         |                    | *                  | V              |
| $I_{IH}$   |  |                    |            | $\pm 10$           |           |     |     | *         |                    | *                  | $\mu A$        |
| $I_{IL}$   |  |                    |            | $\pm 10$           |           |     |     | *         |                    | *                  | $\mu A$        |
| <b>DIGITAL OUTPUT</b>  |  |                    |            |                    |           |     |     |           |                    |                    |                |
| $V_{OH}$   | $I_{OH} = -0.8mA$                                  | 3.6                | 4.5        |                    | *         | *   |     | *         | *                  | *                  | V              |
| $V_{OL}$   | $I_{OL} = 1.6mA$                                   |                    | 0.3        | 0.4                |           | *   | *   |           | *                  | *                  | V              |
| <b>POWER SUPPLY</b>  |  |                    |            |                    |           |     |     |           |                    |                    |                |
| $V_{DD}$   |  | +4.75              | +5.0       | +5.25              | *         | *   | *   | *         | *                  | *                  | V              |
| $V_{CC}$   |  | +14.25             | +15.0      | +15.75             | *         | *   | *   | *         | *                  | *                  | V              |
| $V_{SS}$   |  | -14.25             | -15.0      | -15.75             | *         | *   | *   | *         | *                  | *                  | V              |
| $I_{DD}$   |  |                    | 50         |                    |           | *   |     | *         | *                  | *                  | $\mu A$        |
| $I_{CC}$   |  |                    | 6          |                    |           | *   |     | *         | *                  | *                  | mA             |
| $I_{SS}$   |  |                    | -5         |                    |           | *   |     | *         | *                  | *                  | mA             |
| Power  |  |                    | 170        | 200                |           | *   |     | *         | *                  | *                  | mW             |
| <b>TEMPERATURE RANGE</b>                                     |  |                    |            |                    |           |     |     |           |                    |                    |                |
| Specified Performance  |  | -40                |            | +85                | *         |     | *   | *         |                    | *                  | $^{\circ}C$    |

\* Specifications same as grade to the left.

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# SPECIFICATIONS (Single Supply)

At  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{CC} = +15V$ ,  $V_{DD} = +5V$ ,  $V_{SS} = GND$ ,  $V_{REFH} = +10V$ , and  $V_{REFL} = +50mV$ , unless otherwise noted.

| PARAMETER  | CONDITIONS  | DAC7734E           |            |                    | DAC7734EB |     |     | DAC7734EC |                    |                    | UNITS          |
|--|---|--------------------|------------|--------------------|-----------|-----|-----|-----------|--------------------|--------------------|----------------|
|  |   | MIN                | TYP        | MAX                | MIN       | TYP | MAX | MIN       | TYP                | MAX                |                |
| <b>ACCURACY</b>  |   |                    |            |                    |           |     |     |           |                    |                    |                |
| Linearity Error <sup>(1)</sup> (INL)<br>$T_{MIN}$ to $T_{MAX}$ | $T = 25^\circ C$                                      |                    |            | $\pm 3$<br>$\pm 4$ |           |     | *   |           |                    | $\pm 2$<br>$\pm 3$ | LSB<br>LSB     |
| Linearity Match  |   |                    | $\pm 4$    |                    |           | *   |     |           | $\pm 2$            |                    | LSB            |
| Differential Linearity Error (DNL)<br>$T_{MIN}$ to $T_{MAX}$   | $T = 25^\circ C$                                      |                    |            | $\pm 3$<br>$\pm 3$ |           |     |     |           | $\pm 2$<br>$\pm 2$ |                    | LSB<br>LSB     |
| Monotonicity, $T_{MIN}$ to $T_{MAX}$                           | $T = 25^\circ C$                                      | 14                 | $\pm 0.01$ |                    | 15        |     |     | 16        |                    |                    | Bits           |
| Unipolar Zero  | $T = 25^\circ C$                                      |                    |            | $\pm 0.025$        |           |     | *   |           |                    | *                  | % of FSR       |
| Unipolar Zero Error, $T_{MIN}$ to $T_{MAX}$                    |   |                    |            | $\pm 0.05$         |           |     | *   |           |                    | *                  | % of FSR       |
| Full-Scale Error   | $T = 25^\circ C$                                      |                    |            | $\pm 0.025$        |           |     | *   |           |                    | *                  | % of FSR       |
| Full-Scale Error, $T_{MIN}$ to $T_{MAX}$                       |   |                    |            | $\pm 0.05$         |           |     | *   |           |                    | *                  | % of FSR       |
| Unipolar Zero Matching   | Channel-to-Channel Matching                           |                    |            | $\pm 0.024$        |           |     | *   |           |                    | *                  | % of FSR       |
| Full-Scale Matching  | Channel-to-Channel Matching                           |                    |            | $\pm 0.024$        |           |     | *   |           |                    | *                  | % of FSR       |
| Power Supply Rejection Ratio (PSRR)                            | At Full Scale   |                    |            | 25                 |           |     | *   |           |                    | *                  | ppm/V          |
| <b>ANALOG OUTPUT</b>   |   |                    |            |                    |           |     |     |           |                    |                    |                |
| Voltage Output   | $V_{REFL} = 0V$ , $V_{SS} = 0V$<br>$R = 10k\Omega$    | 0                  |            | $V_{REFH}$         | *         |     | *   | *         |                    | *                  | V              |
| Output Current   |   | $\pm 5$            |            |                    | *         |     |     | *         |                    | *                  | mA             |
| Maximum Load Capacitance                                       |   |                    | 500        |                    |           | *   |     | *         | *                  | *                  | pF             |
| Short-Circuit Current  |   |                    | $\pm 20$   |                    |           | *   |     | *         | *                  | *                  | mA             |
| Short-Circuit Duration   | To $V_{CC}$ or GND                                    |                    | Indefinite |                    |           | *   |     | *         | *                  | *                  |                |
| <b>REFERENCE INPUT</b>   |   |                    |            |                    |           |     |     |           |                    |                    |                |
| Ref High Input Voltage Range                                   |   | $V_{REFL} + 1.25$  |            | +10                | *         |     | *   | *         |                    | *                  | V              |
| Ref Low Input Voltage Range                                    |   | 0                  |            | $V_{REFH} - 1.25$  | *         |     | *   | *         |                    | *                  | V              |
| Ref High Input Current   |   | -0.3               |            | 1.0                |           | *   |     |           | *                  | *                  | mA             |
| Ref Low Input Current  |   | -1.5               |            | -0.3               |           | *   |     |           | *                  | *                  | mA             |
| <b>DYNAMIC PERFORMANCE</b>                                     |   |                    |            |                    |           |     |     |           |                    |                    |                |
| Settling Time  | To $\pm 0.003\%$ , 10V<br>Output Step<br>See Figure 6 |                    | 8          | 10                 |           | *   | *   |           | *                  | *                  | $\mu s$        |
| Channel-to-Channel Crosstalk                                   |   |                    | 0.5        |                    |           | *   |     |           | *                  | *                  | LSB            |
| Digital Feedthrough  |   |                    | 2          |                    |           | *   |     |           | *                  | *                  | nV-s           |
| Output Noise Voltage   | $f = 10kHz$   |                    | 60         |                    |           | *   |     |           | *                  | *                  | $nV/\sqrt{Hz}$ |
| <b>DIGITAL INPUT</b>   |   |                    |            |                    |           |     |     |           |                    |                    |                |
| $V_{IH}$   |   | $0.7 \cdot V_{DD}$ |            | $V_{DD}$           | *         |     |     | *         |                    | *                  | V              |
| $V_{IL}$   |   | 0                  |            | $0.3 \cdot V_{DD}$ |           |     | *   |           | *                  | *                  | V              |
| $I_{IH}$   |   |                    |            | $\pm 10$           |           |     | *   |           | *                  | *                  | $\mu A$        |
| $I_{IL}$   |   |                    |            | $\pm 10$           |           |     | *   |           | *                  | *                  | $\mu A$        |
| <b>DIGITAL OUTPUT</b>  |   |                    |            |                    |           |     |     |           |                    |                    |                |
| $V_{OH}$   | $I_{OH} = -0.8mA$                                     | 3.6                | 4.5        |                    | *         | *   | *   | *         | *                  | *                  | V              |
| $V_{OL}$   | $I_{OL} = 1.6mA$                                      |                    | 0.3        | 0.4                |           | *   | *   | *         | *                  | *                  | V              |
| <b>POWER SUPPLY</b>  |   |                    |            |                    |           |     |     |           |                    |                    |                |
| $V_{DD}$   |   | +4.75              | +5.0       | +5.25              | *         | *   | *   | *         | *                  | *                  | V              |
| $V_{CC}$   |   | +14.25             | +15.0      | +15.75             | *         | *   | *   | *         | *                  | *                  | V              |
| $V_{SS}$   |   |                    | 0          |                    |           | *   | *   | *         | *                  | *                  | V              |
| $I_{DD}$   |   |                    | 50         |                    |           | *   | *   | *         | *                  | *                  | $\mu A$        |
| $I_{CC}$   |   |                    | 3.5        |                    |           | *   | *   | *         | *                  | *                  | mA             |
| Power  |   |                    | 50         | 70                 |           | *   | *   | *         | *                  | *                  | mW             |
| <b>TEMPERATURE RANGE</b>                                       |   |                    |            |                    |           |     |     |           |                    |                    |                |
| Specified Performance  |   | -40                |            | +85                | *         |     | *   | *         |                    | *                  | $^\circ C$     |

\* Specifications same as grade to the left.

NOTE: (1) If  $V_{SS} = 0V$ , the specification applies at code 0021<sub>H</sub> and above, due to possible negative zero scale error.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

|   |                          |
|---|--------------------------|
| $V_{CC}$ to $V_{SS}$ .....              | -0.3V to +32V            |
| $V_{CC}$ to AGND .....                  | -0.3V to +16V            |
| $V_{SS}$ to AGND .....                  | +0.3V to -16V            |
| AGND to DGND .....                      | -0.3V to +0.3V           |
| $V_{REFH}$ to AGND .....                | -9V to +11V              |
| $V_{REFL}$ to AGND .....                | -11V to +9V              |
| $V_{DD}$ to GND .....                   | -0.3V to +6V             |
| $V_{REFH}$ to $V_{REFL}$ .....          | -1V to 22V               |
| Digital Input Voltage to GND .....      | -0.3V to $V_{DD} + 0.3V$ |
| Digital Output Voltage to GND .....     | -0.3V to $V_{DD} + 0.3V$ |
| Maximum Junction Temperature .....      | +150°C                   |
| Operating Temperature Range .....       | -40°C to +85°C           |
| Storage Temperature Range .....         | -65°C to +150°C          |
| Lead Temperature (soldering, 10s) ..... | +300°C                   |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

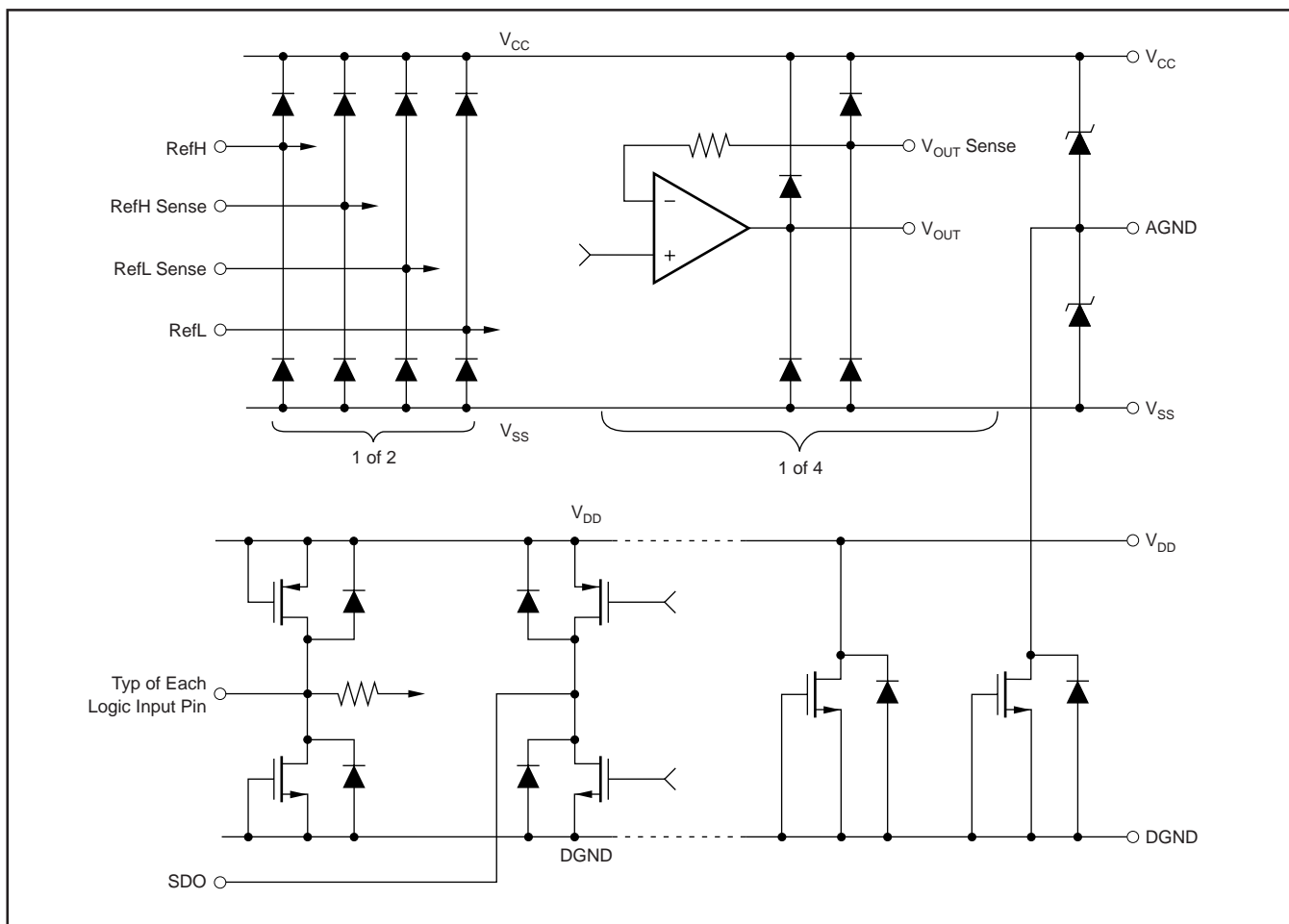
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

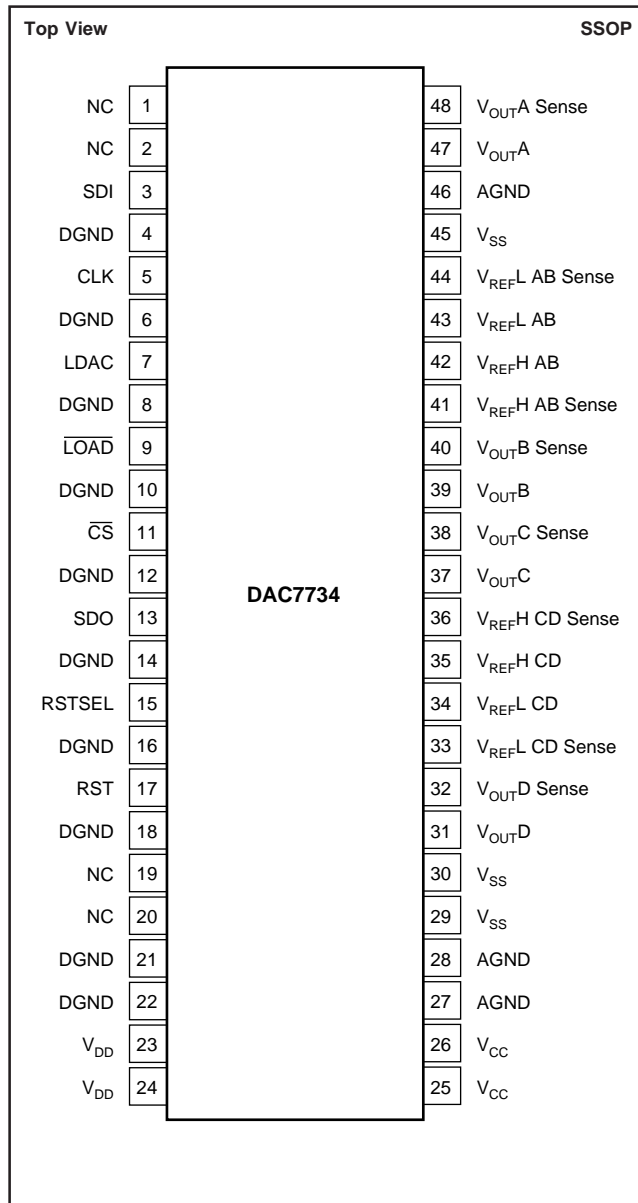
| PRODUCT        | LINEARITY ERROR (LSB) | DIFFERENTIAL NONLINEARITY (LSB) | PACKAGE      | PACKAGE DRAWING NUMBER | SPECIFICATION TEMPERATURE RANGE | ORDERING NUMBER <sup>(1)</sup> | TRANSPORT MEDIA        |
|----------------|-----------------------|---------------------------------|--------------|------------------------|---------------------------------|--------------------------------|------------------------|
| DAC7734E<br>"  | ±4<br>"               | ±3<br>"                         | SSOP-48      | 333<br>"               | -40°C to +85°C<br>"             | DAC7734E<br>DAC7734E/1K        | Rails<br>Tape and Reel |
| DAC7734EB<br>" | ±4<br>"               | ±2<br>"                         | SSOP-48<br>" | 333<br>"               | -40°C to +85°C<br>"             | DAC7734EB<br>DAC7734EB/1K      | Rails<br>Tape and Reel |
| DAC7734EC<br>" | ±3<br>"               | ±1<br>"                         | SSOP-48<br>" | 333<br>"               | -40°C to +85°C<br>"             | DAC7734EC<br>DAC7734EC/1K      | Rails<br>Tape and Reel |

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "DAC7734E/1K" will get a single 1000-piece Tape and Reel.

## ESD PROTECTION CIRCUITS



## PIN CONFIGURATION



## PIN DESCRIPTIONS

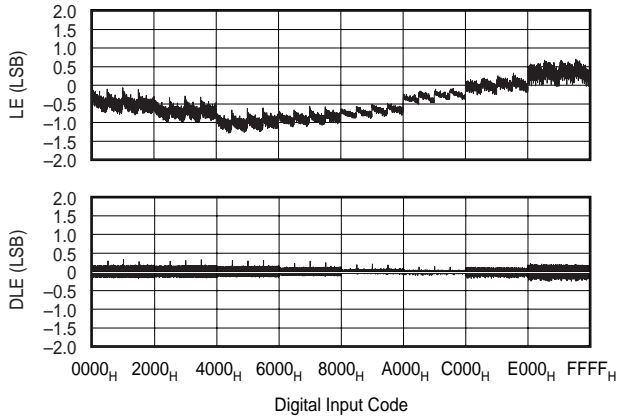
| PIN | NAME                       | DESCRIPTION  |
|-----|----------------------------|--|
| 1   | NC                         | No Connection  |
| 2   | NC                         | No Connection  |
| 3   | SDI                        | Serial Data Input  |
| 4   | DGND                       | Digital Ground   |
| 5   | CLK                        | Data Clock Input   |
| 6   | DGND                       | Digital Ground   |
| 7   | LDAC                       | DAC Register Load Control, Rising Edge Triggered   |
| 8   | DGND                       | Digital Ground   |
| 9   | LOAD                       | DAC Input Register Load Control, Active Low  |
| 10  | DGND                       | Digital Ground   |
| 11  | CS                         | Chip Select, Active Low  |
| 12  | DGND                       | Digital Ground   |
| 13  | SDO                        | Serial Data Output   |
| 14  | DGND                       | Digital Ground   |
| 15  | RSTSEL                     | Reset Select. Determines the action of RST. If HIGH, a RST common will set the DAC registers to mid-scale (8000H). If LOW, a RST command will set the DAC registers to zero (0000H). |
| 16  | DGND                       | Digital Ground   |
| 17  | RST                        | Reset, Rising Edge Triggered. Depending on the state of RSTSEL, the DAC registers are set to either mid-scale or zero.   |
| 18  | DGND                       | Digital Ground   |
| 19  | NC                         | No Connection  |
| 20  | NC                         | No Connection  |
| 21  | DGND                       | Digital Ground   |
| 22  | DGND                       | Digital Ground   |
| 23  | V <sub>DD</sub>            | Digital +5V Power Supply   |
| 24  | V <sub>DD</sub>            | Digital +5V Power Supply   |
| 25  | V <sub>CC</sub>            | Analog +15V Power Supply   |
| 26  | V <sub>CC</sub>            | Analog +15V Power Supply   |
| 27  | AGND                       | Analog Ground  |
| 28  | AGND                       | Analog Ground  |
| 29  | V <sub>SS</sub>            | Analog -15V Power Supply or 0V Single Supply   |
| 30  | V <sub>SS</sub>            | Analog -15V Power Supply or 0V Single Supply   |
| 31  | V <sub>OUTD</sub>          | DAC D Output Voltage   |
| 32  | V <sub>OUTD</sub> Sense    | DAC D's Output Amplifier Inverting Input. Used to close feedback loop at the load.   |
| 33  | V <sub>REFL</sub> CD Sense | DAC C and D Reference Low Sense Input  |
| 34  | V <sub>REFL</sub> CD       | DAC C and D Reference Low Input  |
| 35  | V <sub>REFH</sub> CD       | DAC C and D Reference High Input   |
| 36  | V <sub>REFH</sub> CD Sense | DAC C and D Reference High Sense Input   |
| 37  | V <sub>OUTC</sub>          | DAC C Output Voltage   |
| 38  | V <sub>OUTC</sub> Sense    | DAC C's Output Amplifier Inverting Input. Used to close the feedback loop at the load.   |
| 39  | V <sub>OUTB</sub>          | DAC B Output Voltage   |
| 40  | V <sub>OUTB</sub> Sense    | DAC B's Output Amplifier Inverting Input. Used to close the feedback loop at the load.   |
| 41  | V <sub>REFH</sub> AB Sense | DAC A and B Reference High Sense Input   |
| 42  | V <sub>REFH</sub> AB       | DAC A and B Reference High Input   |
| 43  | V <sub>OUTL</sub> AB       | DAC A and B Reference Low Input  |
| 44  | V <sub>REFL</sub> AB Sense | DAC A and B Reference Low Sense Input  |
| 45  | V <sub>SS</sub>            | Analog -15V Power Supply or 0V Single Supply   |
| 46  | AGND                       | Analog Ground  |
| 47  | V <sub>OUTA</sub>          | DAC A Output Voltage   |
| 48  | V <sub>OUTA</sub> Sense    | DAC A's Output Amplifier Inverting Input. Used to close the feedback loop at the load.   |

# TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$

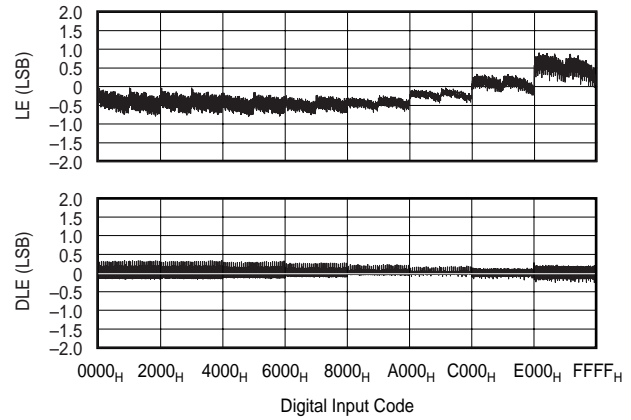
At  $T_A = +25^\circ C$ ,  $V_{DD} = +5V$ ,  $V_{CC} = +15V$ ,  $V_{SS} = 0$ ,  $V_{REFH} = +10V$ , and  $V_{REFL} = 0V$ , representative unit, unless otherwise specified.

## +25°C

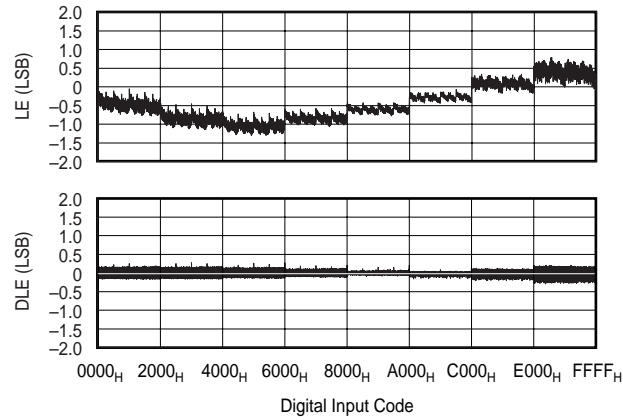
LINEARITY ERROR AND  
DIFFERENTIAL LINEARITY ERROR vs CODE  
(DAC A, +25°C)



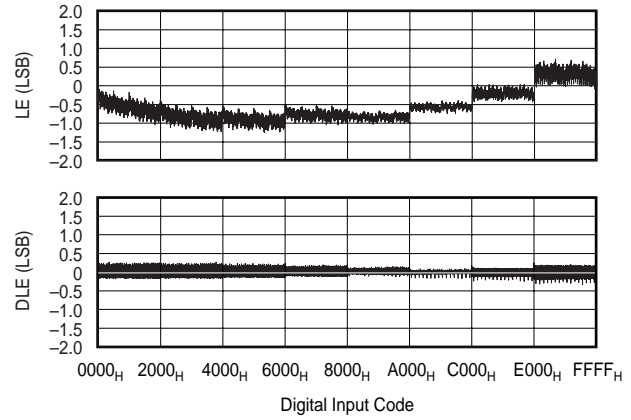
LINEARITY ERROR AND  
DIFFERENTIAL LINEARITY ERROR vs CODE  
(DAC B, +25°C)



LINEARITY ERROR AND  
DIFFERENTIAL LINEARITY ERROR vs CODE  
(DAC C, +25°C)

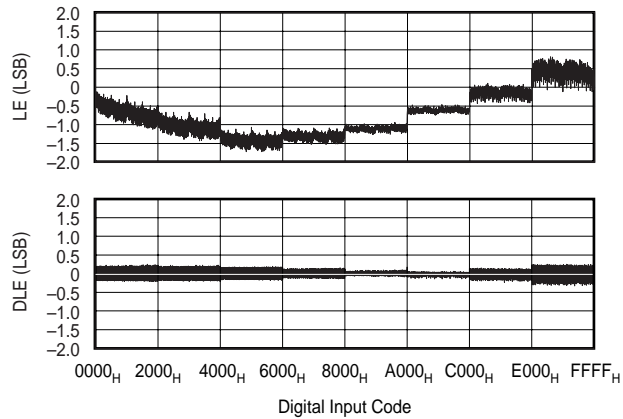


LINEARITY ERROR AND  
DIFFERENTIAL LINEARITY ERROR vs CODE  
(DAC D, +25°C)

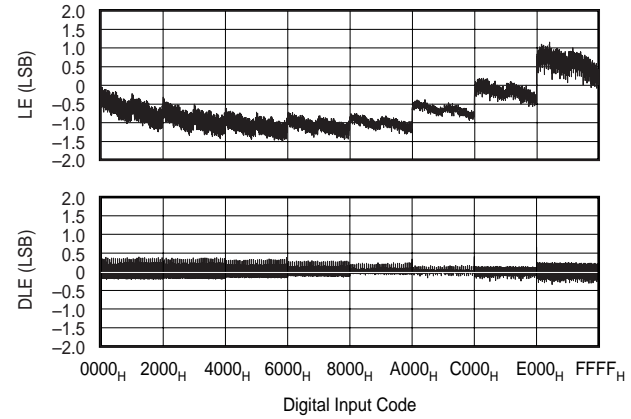


## +85°C

LINEARITY ERROR AND  
DIFFERENTIAL LINEARITY ERROR vs CODE  
(DAC A, +85°C)



LINEARITY ERROR AND  
DIFFERENTIAL LINEARITY ERROR vs CODE  
(DAC B, +85°C)

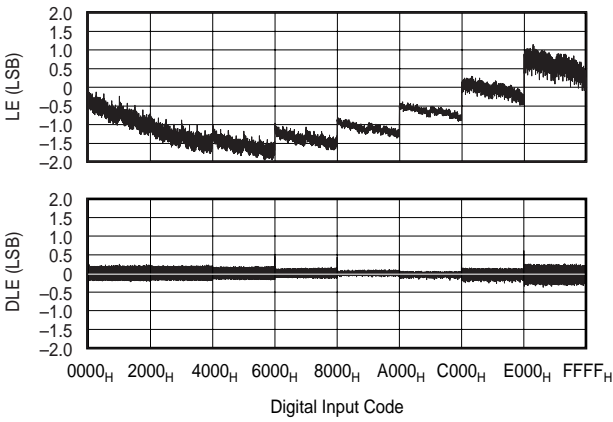


# TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (Cont.)

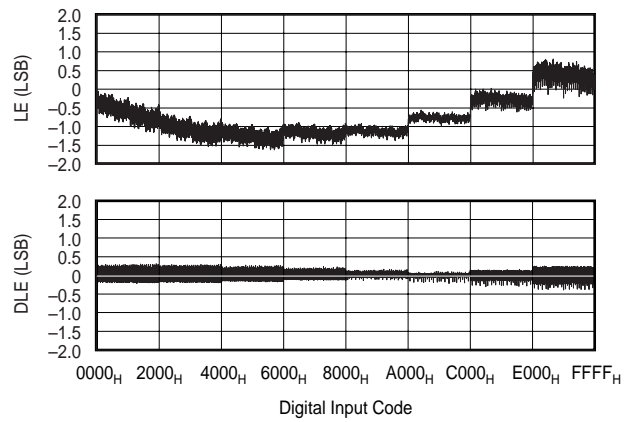
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## +85°C (cont.)

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC C, +85°C)

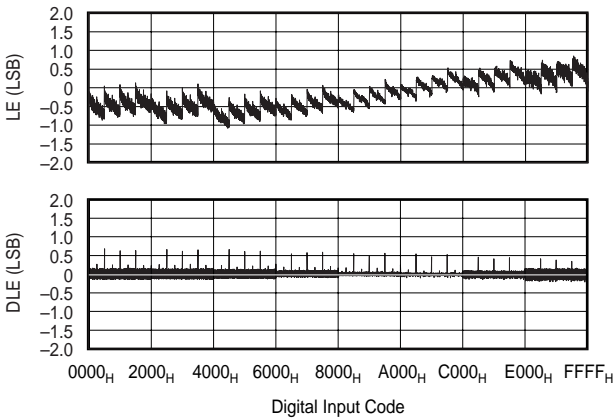


LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC D, +85°C)

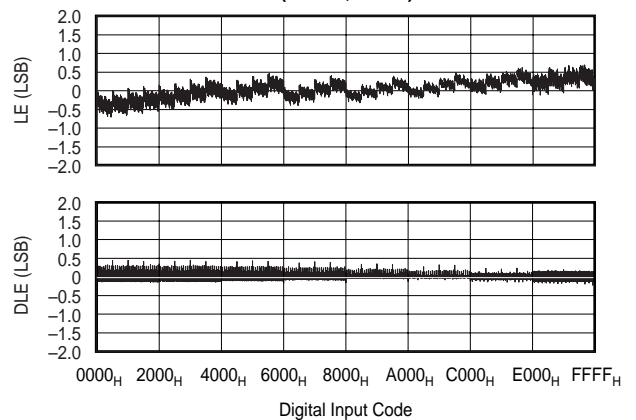


## -40°C

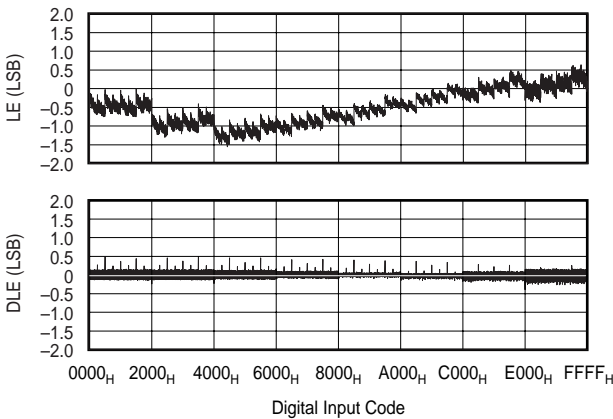
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC A, -40°C)



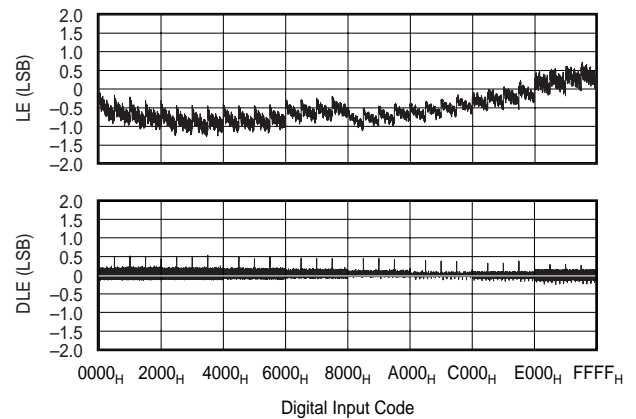
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC B, -40°C)



LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC C, -40°C)

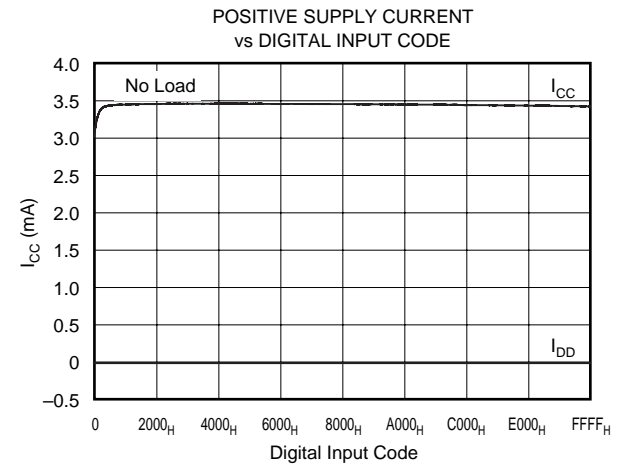
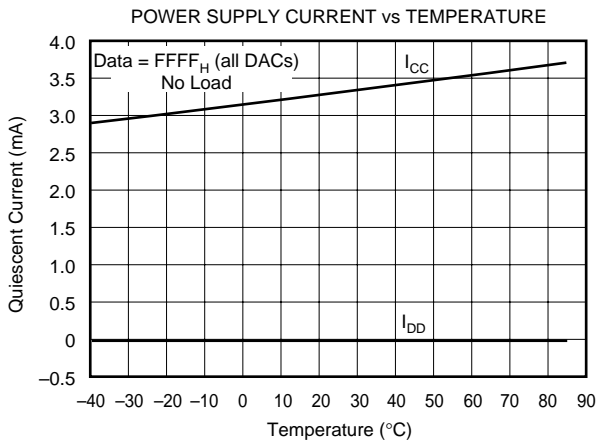
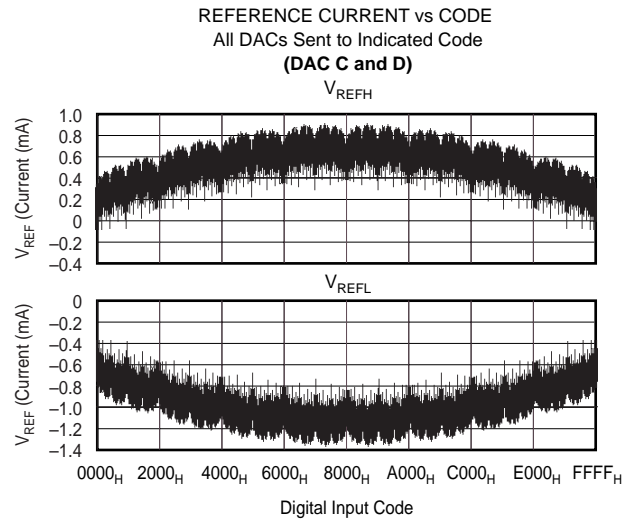
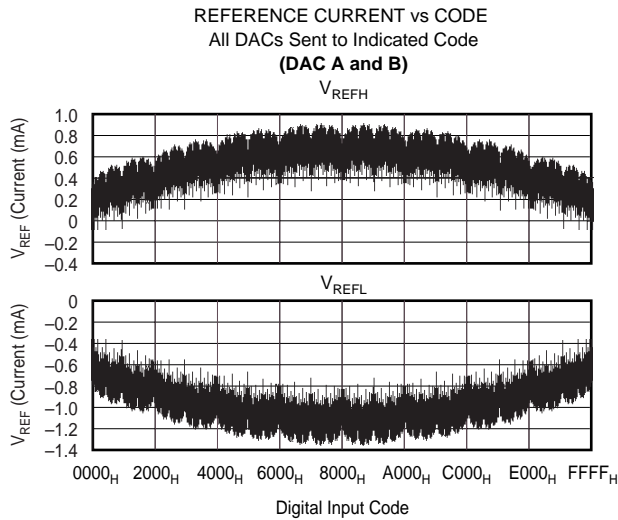
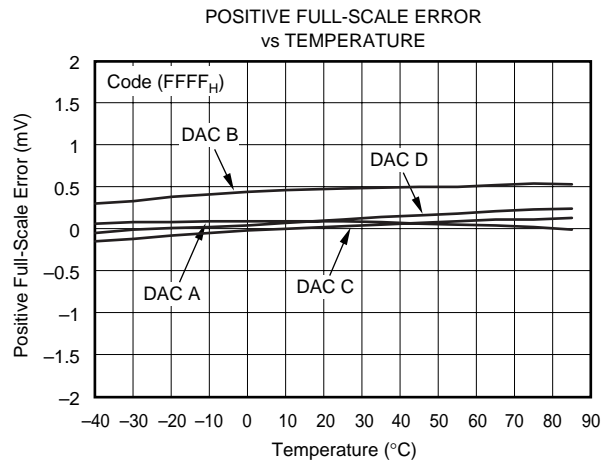
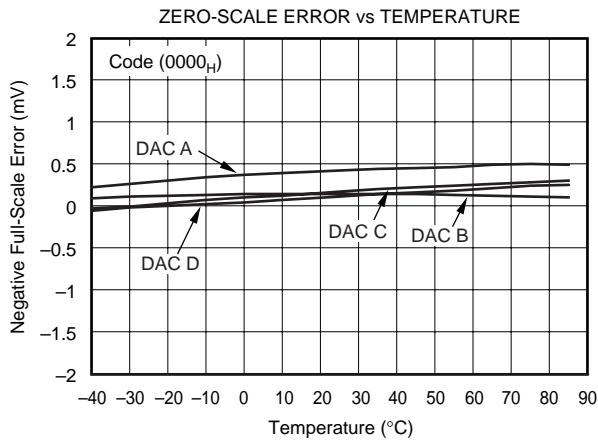


LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC D, -40°C)



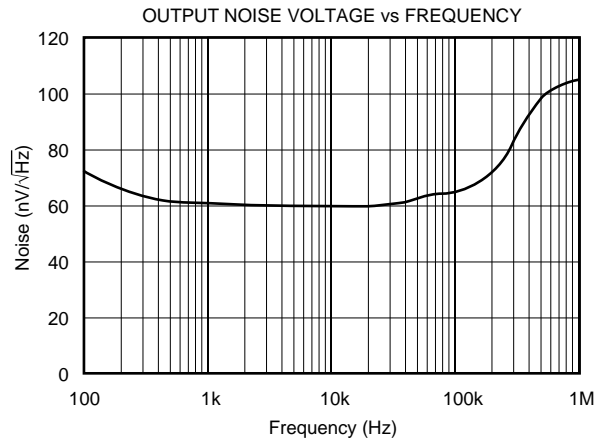
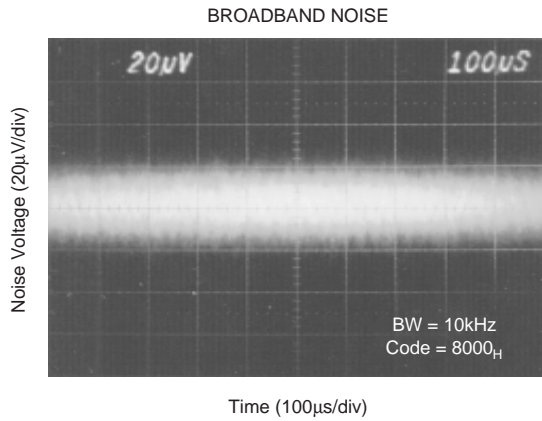
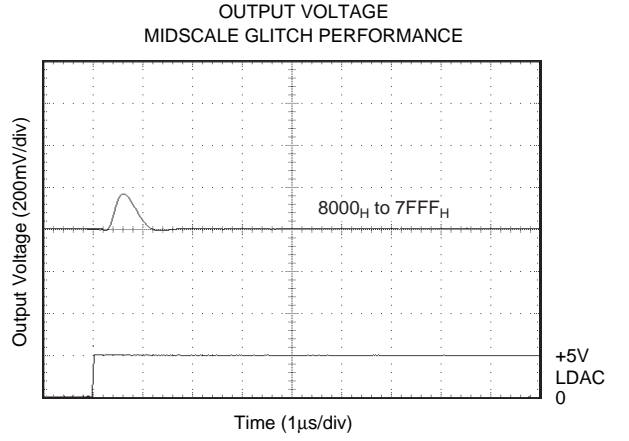
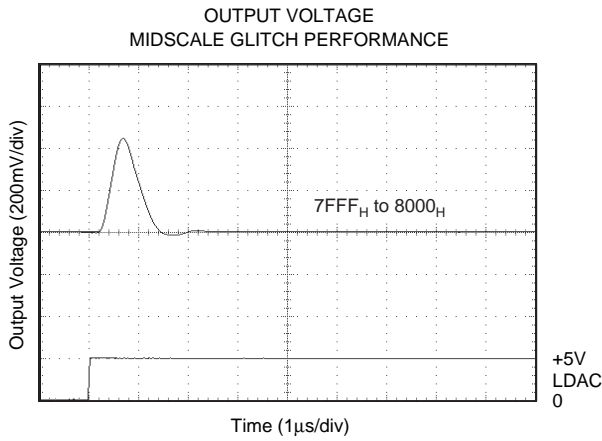
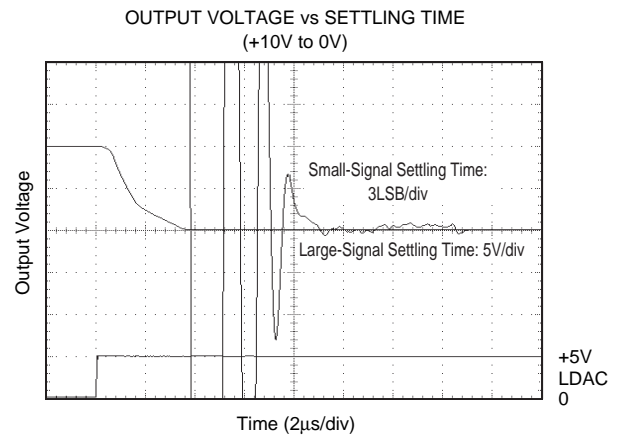
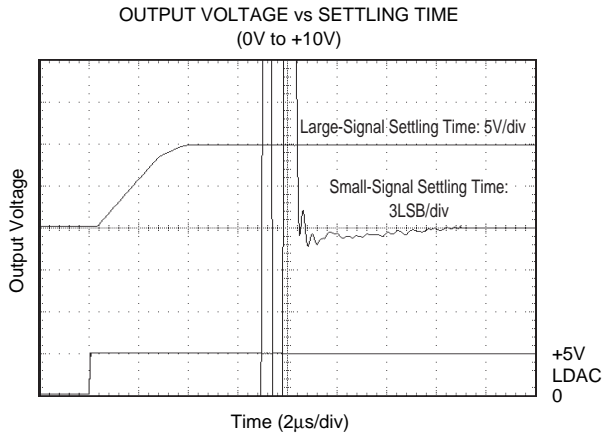
# TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (Cont.)

At  $T_A = +25^\circ C$ ,  $V_{DD} = +5V$ ,  $V_{CC} = +15V$ ,  $V_{SS} = 0$ ,  $V_{REFH} = +10V$ , and  $V_{REFL} = 0V$ , representative unit, unless otherwise specified.



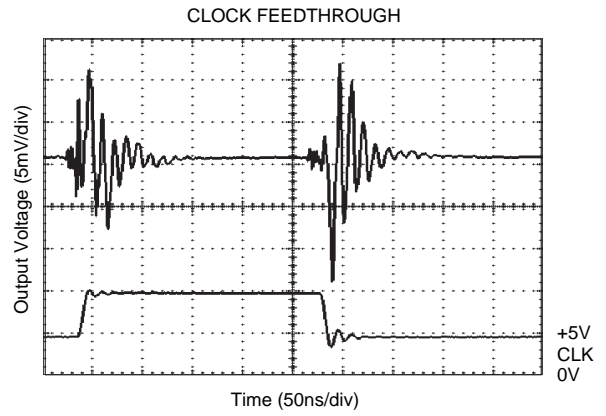
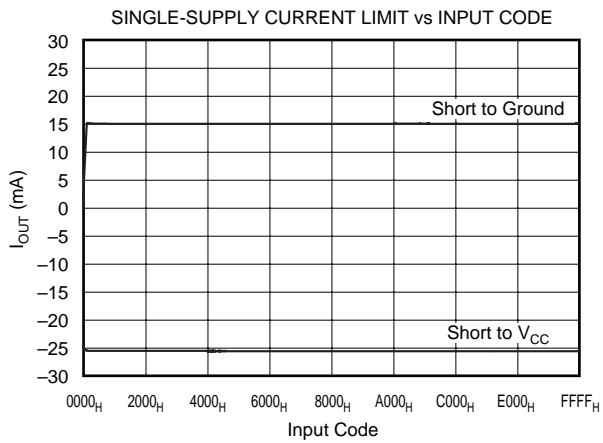
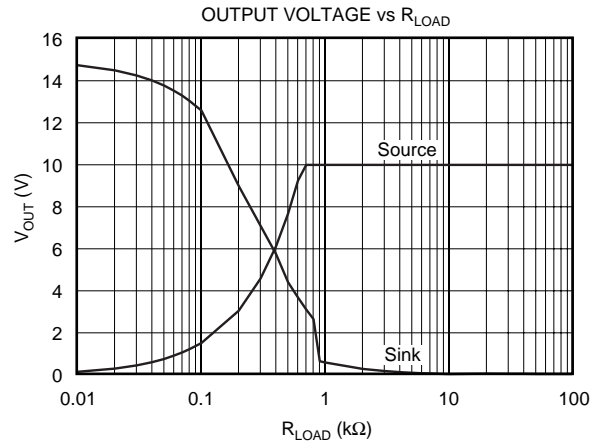
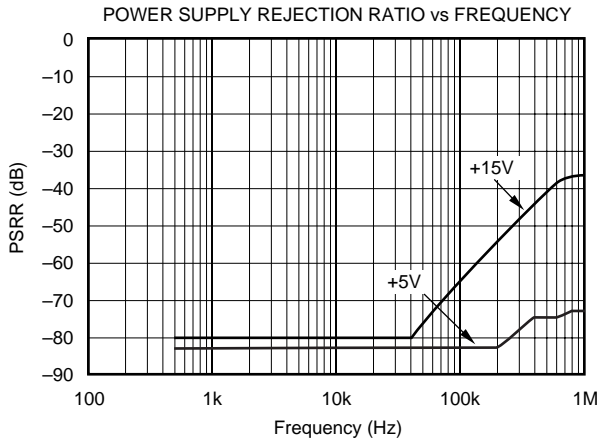
# TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (Cont.)

At  $T_A = +25^\circ C$ ,  $V_{DD} = +5V$ ,  $V_{CC} = +15V$ ,  $V_{SS} = 0$ ,  $V_{REFH} = +10V$ , and  $V_{REFL} = 0V$ , representative unit, unless otherwise specified.



# TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (Cont.)

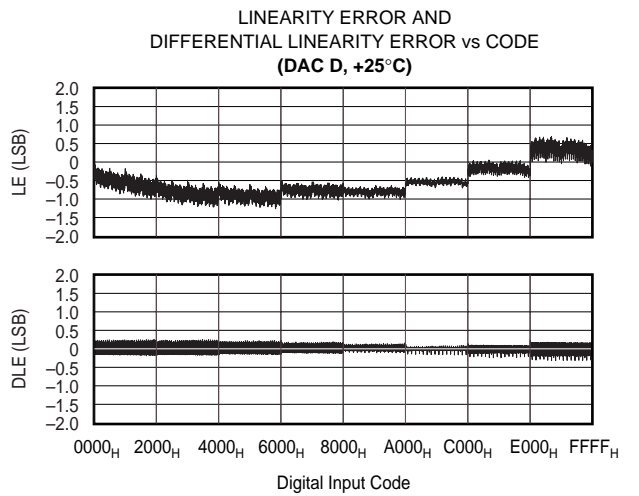
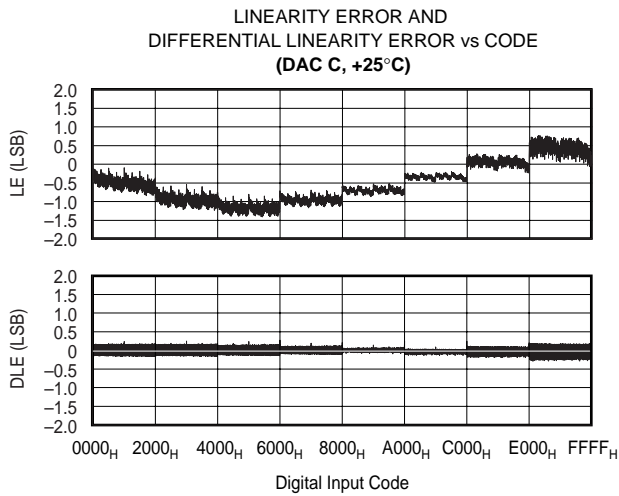
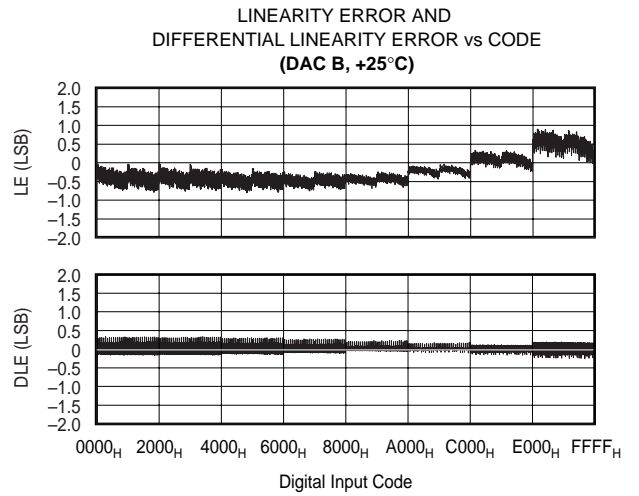
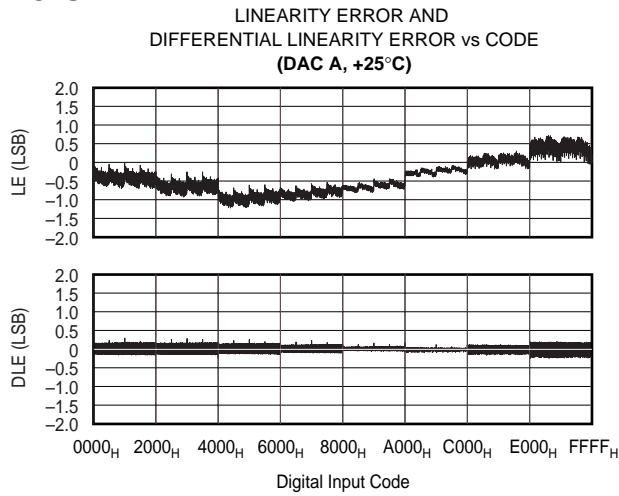
At  $T_A = +25^\circ C$ ,  $V_{DD} = +5V$ ,  $V_{CC} = +15V$ ,  $V_{SS} = 0$ ,  $V_{REFH} = +10V$ , and  $V_{REFL} = 0V$ , representative unit, unless otherwise specified.



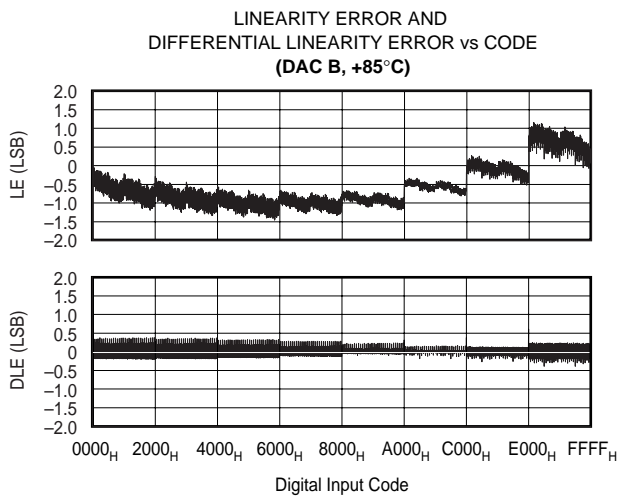
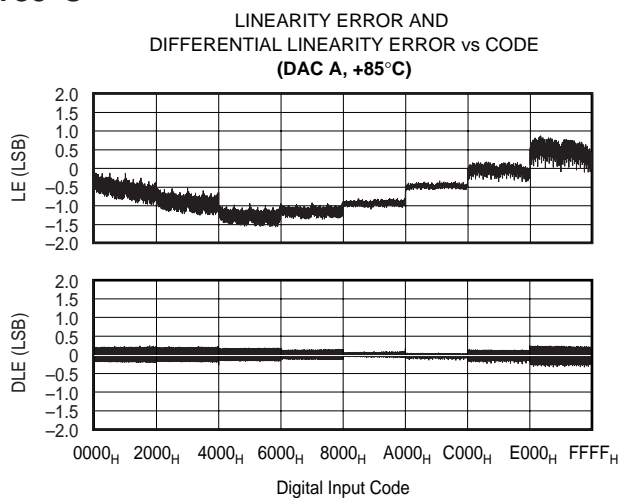
# TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$

At  $T_A = +25^\circ C$ ,  $V_{DD} = +5V$ ,  $V_{CC} = +15V$ ,  $V_{SS} = -15V$ ,  $V_{REFH} = +10V$ , and  $V_{REFL} = -10V$ , representative unit, unless otherwise specified.

## +25°C



## +85°C

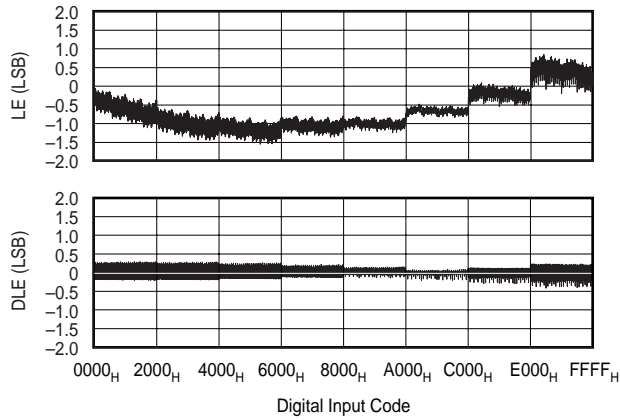


# TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$ (Cont.)

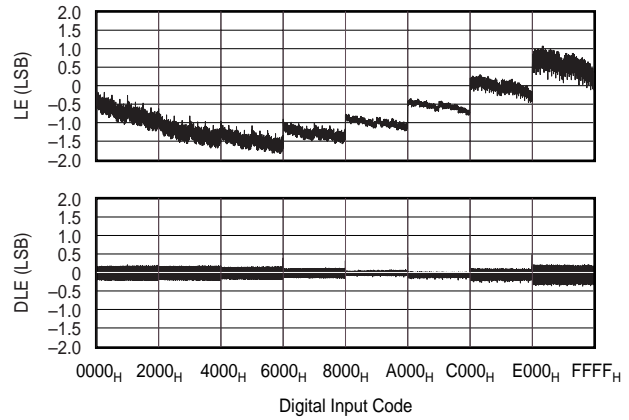
At  $T_A = +25^\circ C$ ,  $V_{DD} = +5V$ ,  $V_{CC} = +15V$ ,  $V_{SS} = -15V$ ,  $V_{REFH} = +10V$ , and  $V_{REFL} = -10V$ , representative unit, unless otherwise specified.

**+85°C (cont.)**

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC C, +85°C)

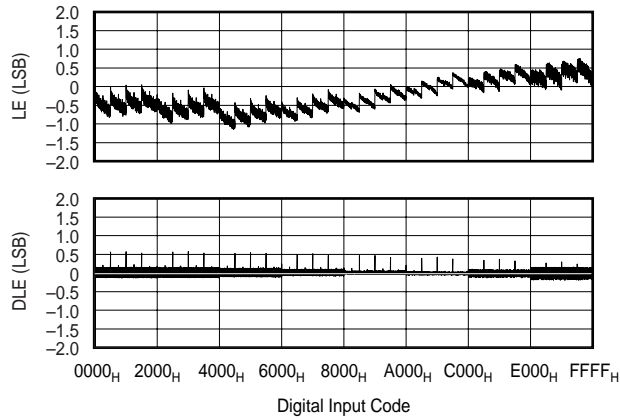


LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC D, +85°C)

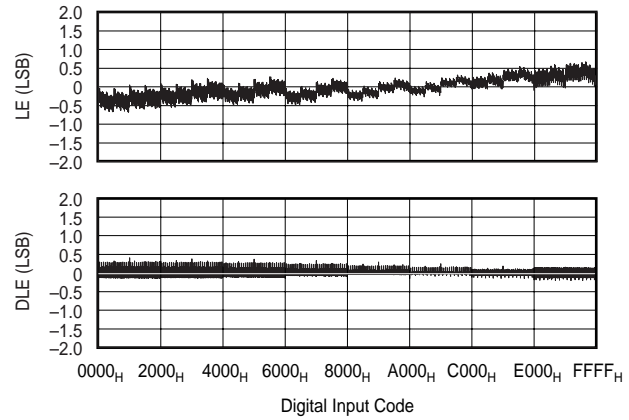


**-40°C**

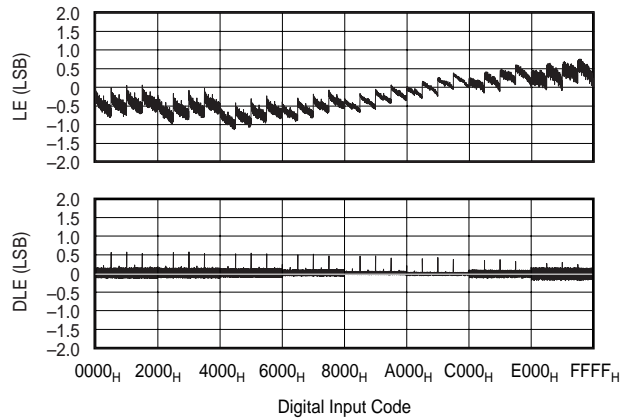
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC A, -40°C)



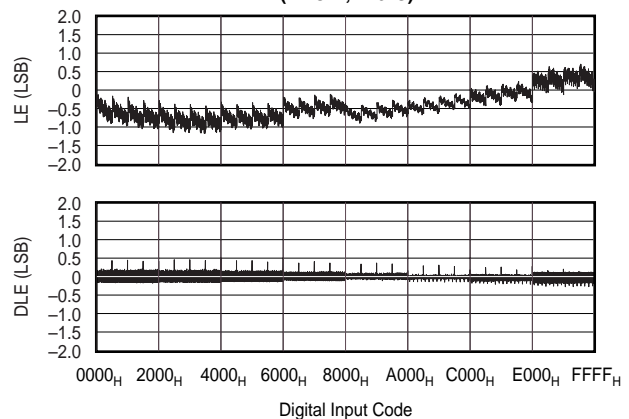
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC B, -40°C)



LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC C, -40°C)

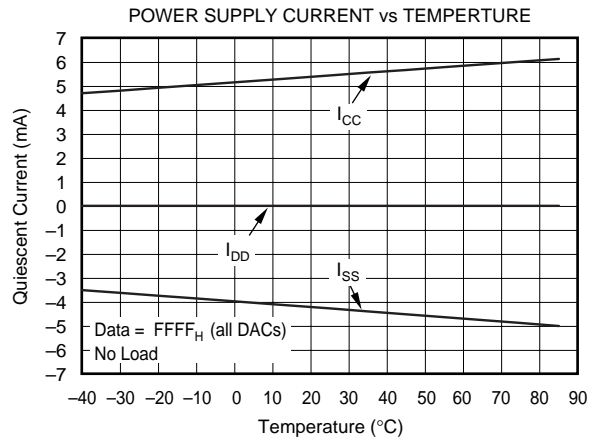
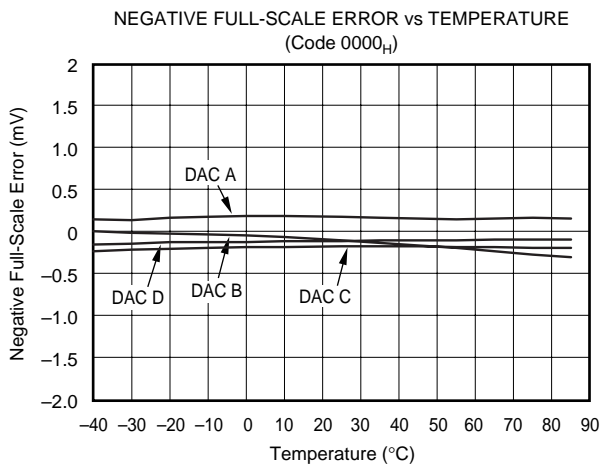
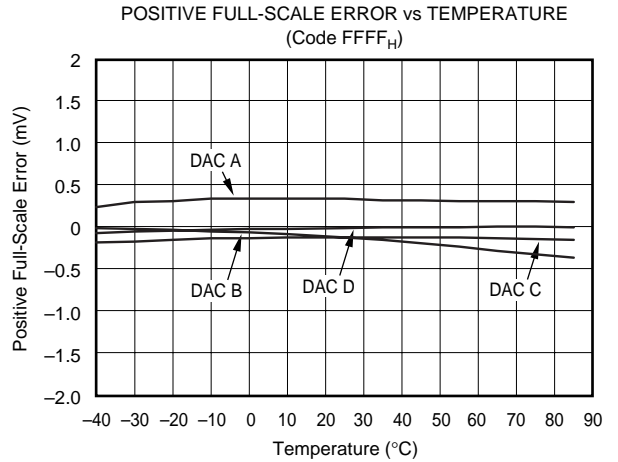
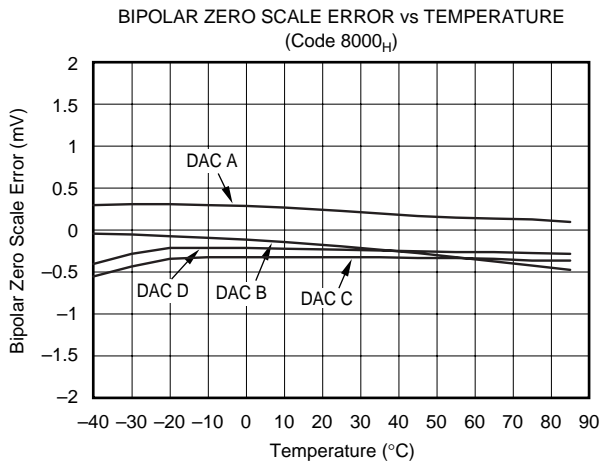
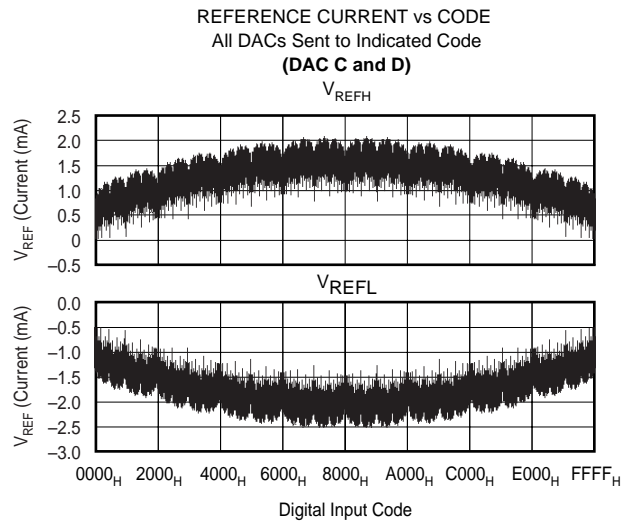
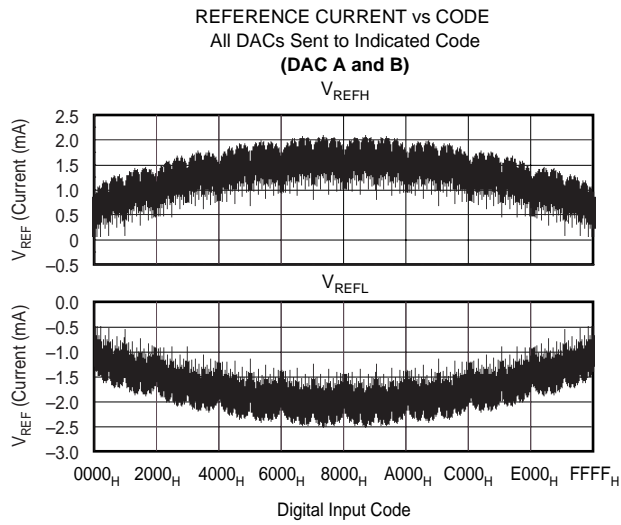


LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE (DAC D, -40°C)



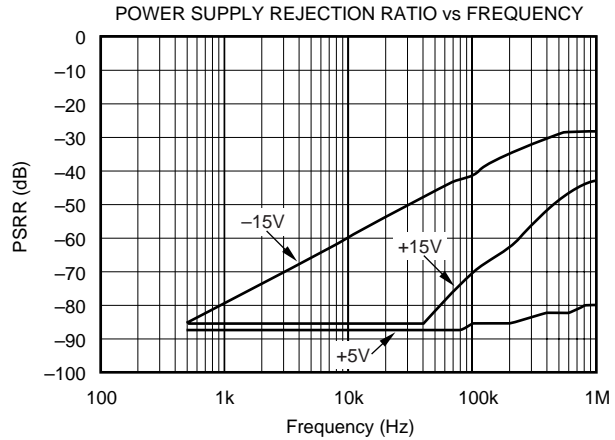
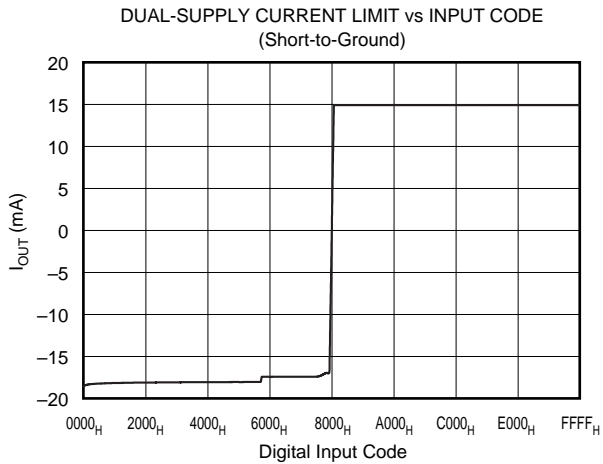
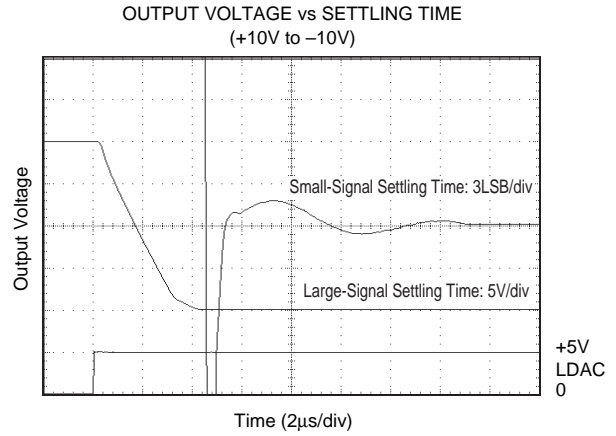
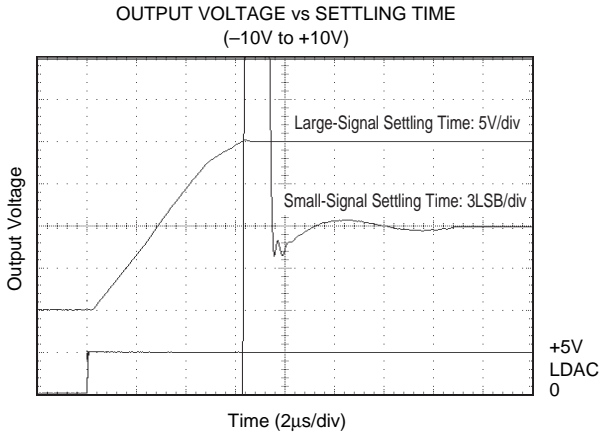
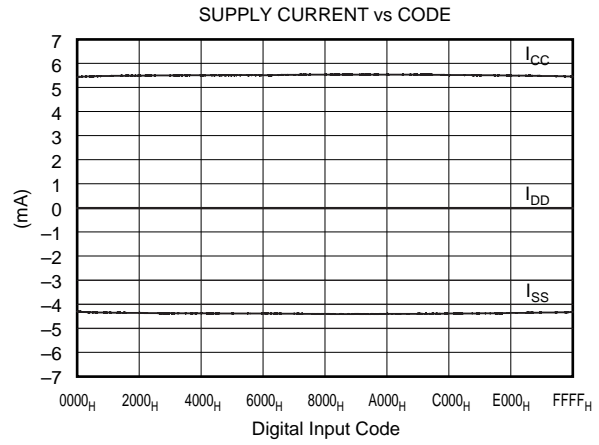
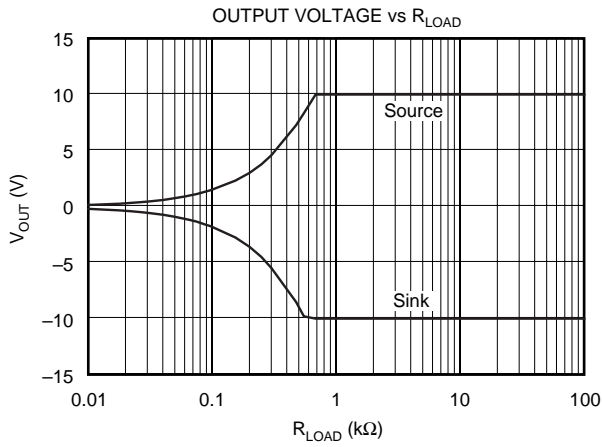
# TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$ (Cont.)

At  $T_A = +25^\circ C$ ,  $V_{DD} = +5V$ ,  $V_{CC} = +15V$ ,  $V_{SS} = -15V$ ,  $V_{REFH} = +10V$ , and  $V_{REFL} = -10V$ , representative unit, unless otherwise specified.



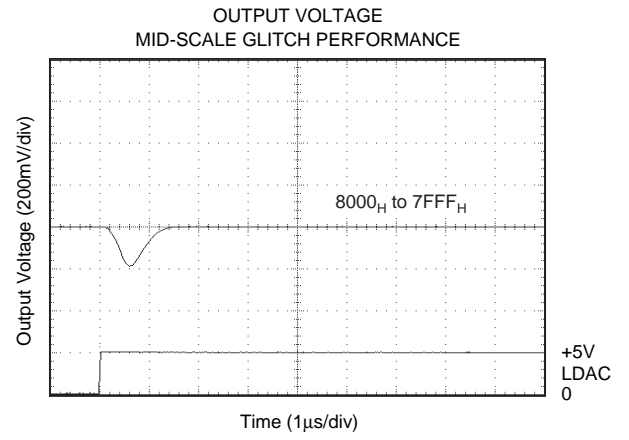
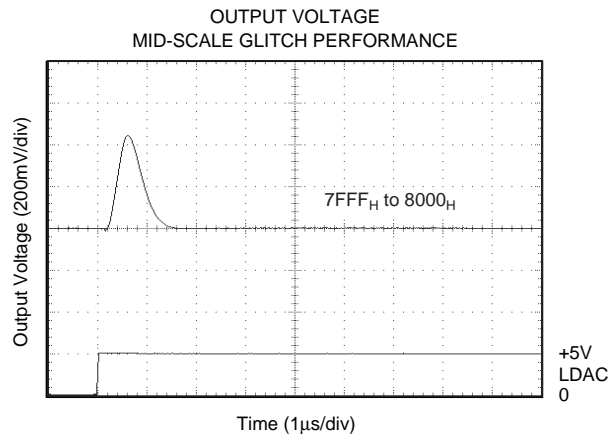
# TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$ (Cont.)

At  $T_A = +25^\circ C$ ,  $V_{DD} = +5V$ ,  $V_{CC} = +15V$ ,  $V_{SS} = -15V$ ,  $V_{REFH} = +10V$ , and  $V_{REFL} = -10V$ , representative unit, unless otherwise specified.



# TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$ (Cont.)

At  $T_A = +25^\circ C$ ,  $V_{DD} = +5V$ ,  $V_{CC} = +15V$ ,  $V_{SS} = -15V$ ,  $V_{REFH} = +10V$ , and  $V_{REFL} = -10V$ , representative unit, unless otherwise specified.



# THEORY OF OPERATION

The DAC7734 is a quad voltage output, 16-bit Digital-to-Analog Converter (DAC). The architecture is an R-2R ladder configuration with the three MSB's segmented, followed by an operational amplifier that serves as a buffer. Each DAC has its own R-2R ladder network, segmented MSBs, and output op amp, as shown in Figure 1. The minimum voltage output (zero-scale) and maximum voltage output (full-scale) are set by the external voltage references  $V_{REFL}$  and  $V_{REFH}$ .

The digital input is a 24-bit serial word that contains a 2-bit address code for selecting one of four DACs, a quick load bit, five unused bits and the 16-bit DAC code (MSB first). The converters can be powered from either a single +15V supply or a dual  $\pm 15V$  supply and a +5V logic supply. The device offers a reset function which immediately sets all DAC output voltages and DAC registers to mid-scale code  $8000_H$  or to zero-scale, code  $0000_H$ . See Figures 2 and 3 for the basic operation of the DAC7734.

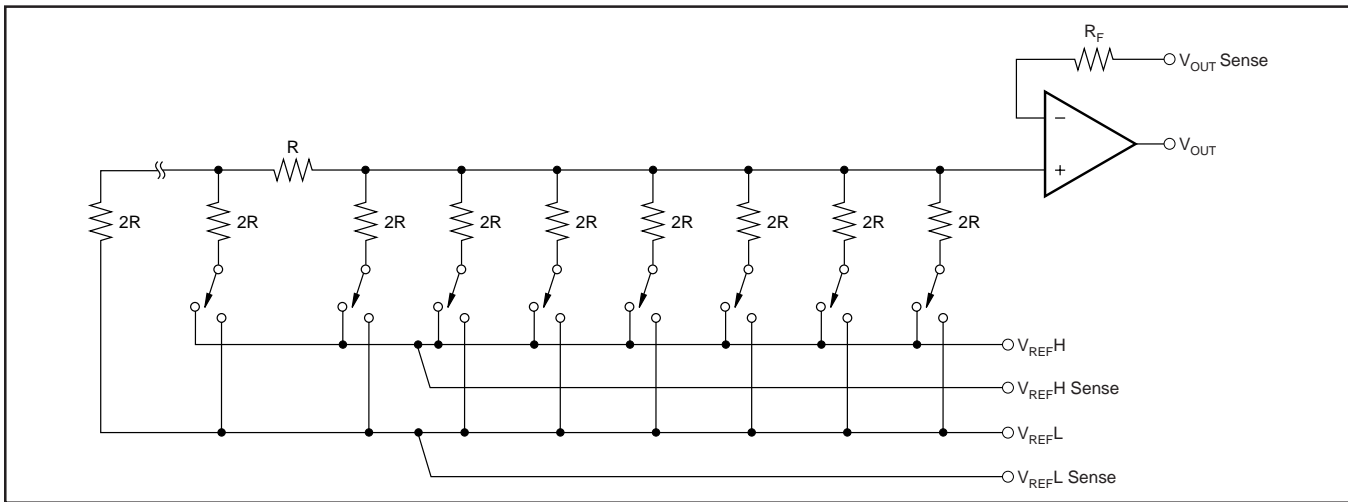


FIGURE 1. DAC7734 Architecture.

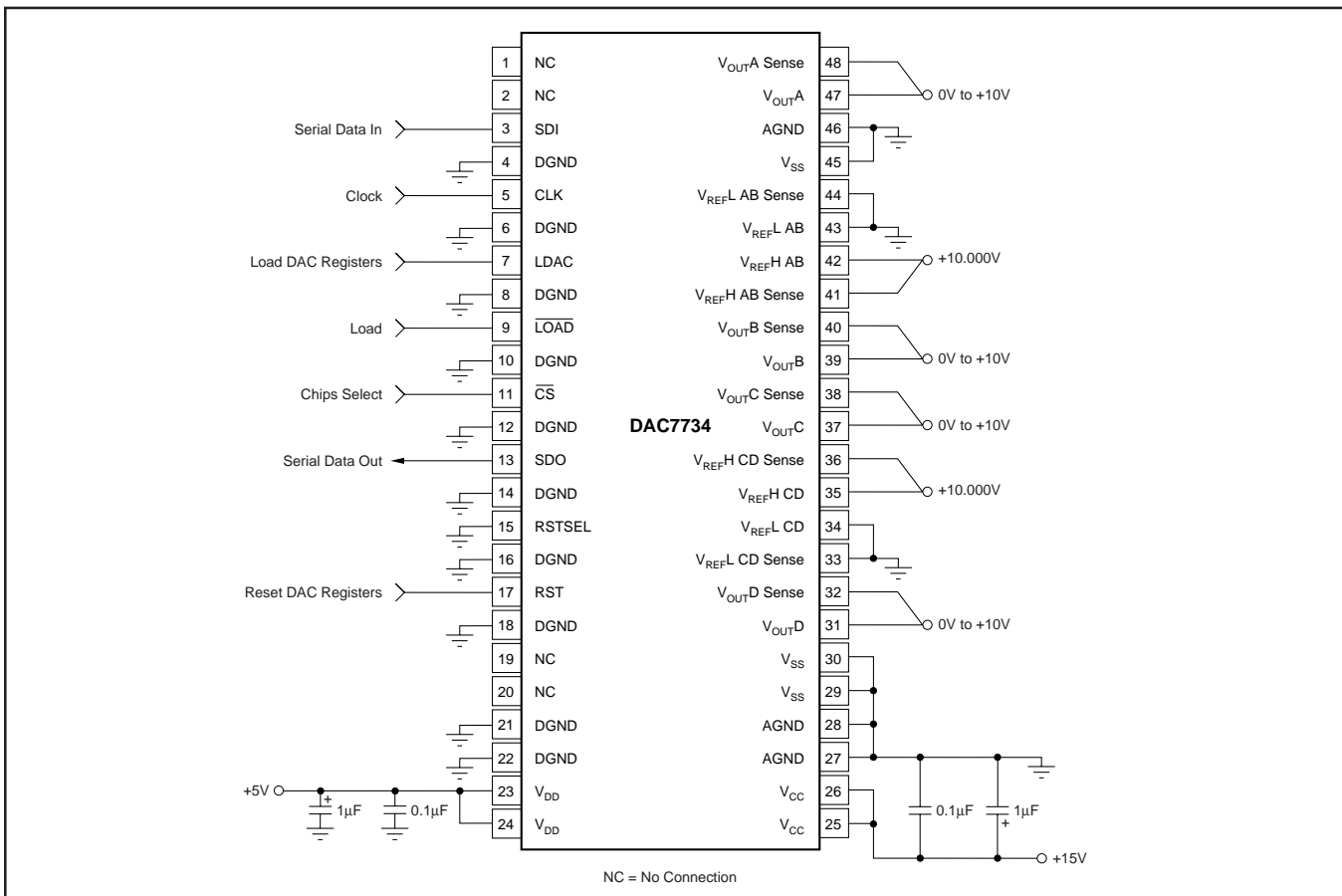


FIGURE 2. Basic Single-Supply Operation of the DAC7734.

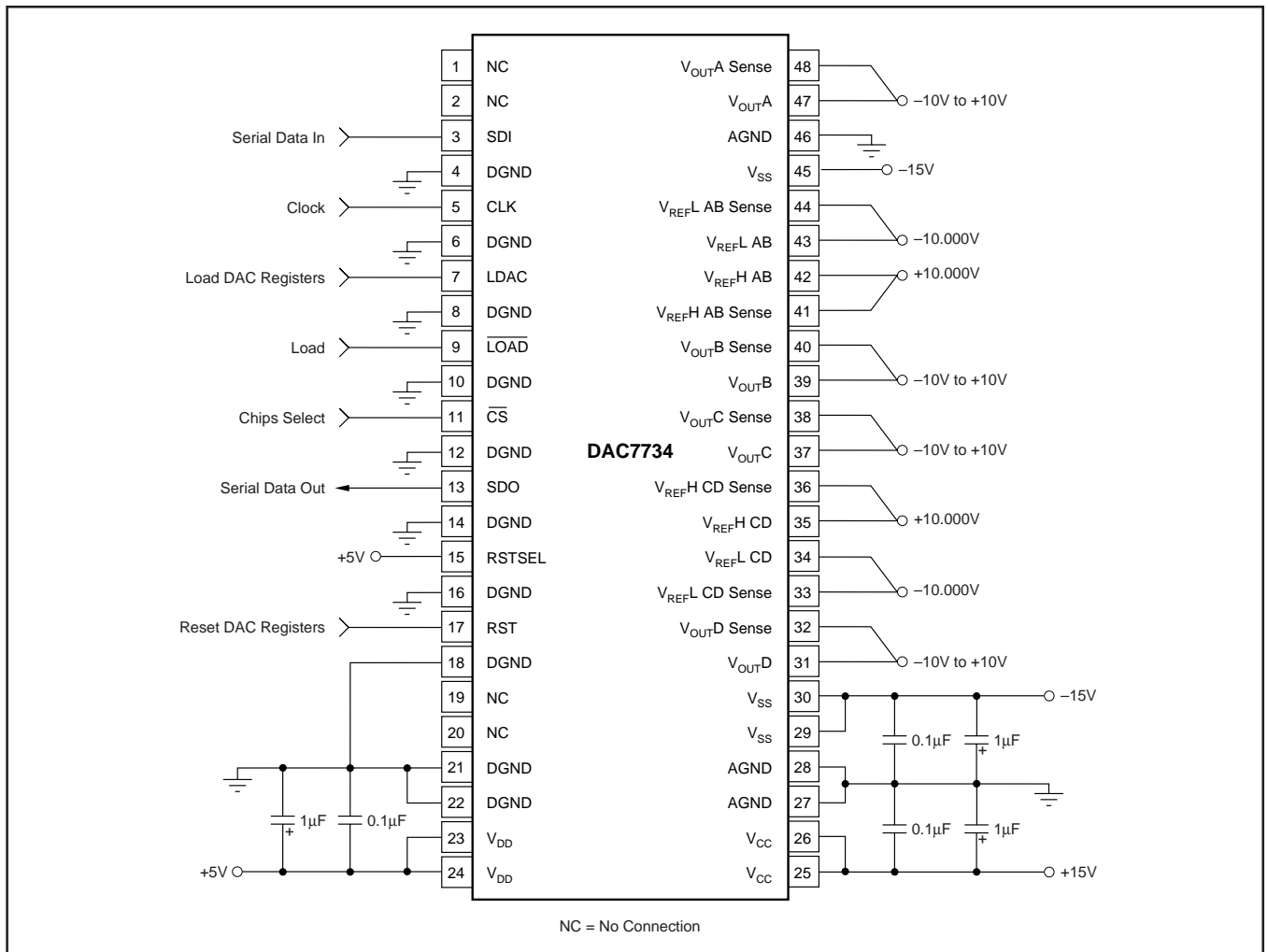


FIGURE 3. Basic Dual-Supply Operation of the DAC7734.

## ANALOG OUTPUTS

When  $V_{SS} = -15V$  (dual supply operation), the output amplifier can swing to within 4V of the supply rails, guaranteed over the  $-40^{\circ}C$  to  $+85^{\circ}C$  temperature range. When  $V_{SS} = 0V$  (single-supply operation), and with  $R_{LOAD}$  also connected to ground, the output can swing to ground. Care must also be taken when measuring the zero-scale error when  $V_{SS} = 0V$ . Since the output voltage cannot swing below ground, the output voltage may not change for the first few digital input codes ( $0000_H$ ,  $0001_H$ ,  $0002_H$ , etc.) if the output amplifier has a negative offset. At the negative limit of  $-5mV$ , the first specified output starts at code  $0021_H$ .

Due to the high accuracy of these D/A converters, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 10V full-scale range has a 1LSB value of  $152\mu V$ . With a load current of 1mA, series wiring and connector resistance of only  $150m\Omega$  ( $R_{W2}$ ) will cause a voltage drop of  $150\mu V$ , as shown in Figure 4. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is  $1/2 m\Omega$  per square. For a 1mA load, a 20 milli-inch wide printed circuit conductor 6 inches long will result in a voltage drop of  $150\mu V$ .

The DAC7734 offers a force and sense output configuration for the high open-loop gain output amplifier. This feature allows the loop around the output amplifier to be closed at the load (as shown in Figure 4), thus ensuring an accurate output voltage.

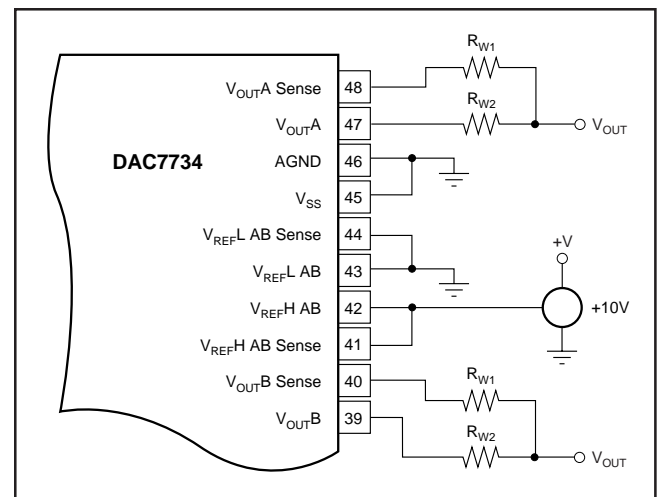


FIGURE 4. Analog Output Closed-Loop Configuration (1/2 DAC7734).  $R_W$  represents wiring resistances.

## REFERENCE INPUTS

The reference inputs,  $V_{REFL}$  and  $V_{REFH}$ , can be any voltage between  $V_{SS} + 4V$  and  $V_{CC} - 4V$ , provided that  $V_{REFH}$  is at least 1.25V greater than  $V_{REFL}$ . The minimum output of each DAC is equal to  $V_{REFL}$  plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to  $V_{REFH}$  plus a similar offset voltage. Note that  $V_{SS}$  (the negative power supply) must either be connected to ground or must be in the range of  $-14.25V$  to  $-15.75V$ . The voltage on  $V_{SS}$  sets several bias points within the converter. If  $V_{SS}$  is not in one of these two configurations, the bias values may be in error and proper operation of the device is not guaranteed.

The current into the  $V_{REFH}$  input and out of  $V_{REFL}$  depends on the DAC output voltages, and can vary from a few microamps to approximately 2.0mA. The reference input appears as a varying load to the reference. The DAC7734 features a reference drive and sense connection such that the internal errors caused by the changing reference current and the circuit impedances can be minimized. Figures 5 through 9 show different reference configurations, and the effect on the linearity and differential linearity.

The analog supplies have to come up first. If  $V_{CC}$  and  $V_{SS}$  don't come up together, then  $V_{SS}$  should come up first. If the power supplies for the reference come up first, then the  $V_{CC}$  and  $V_{SS}$  supplies will be "powered from the reference via the ESD protection diode", see page 4.

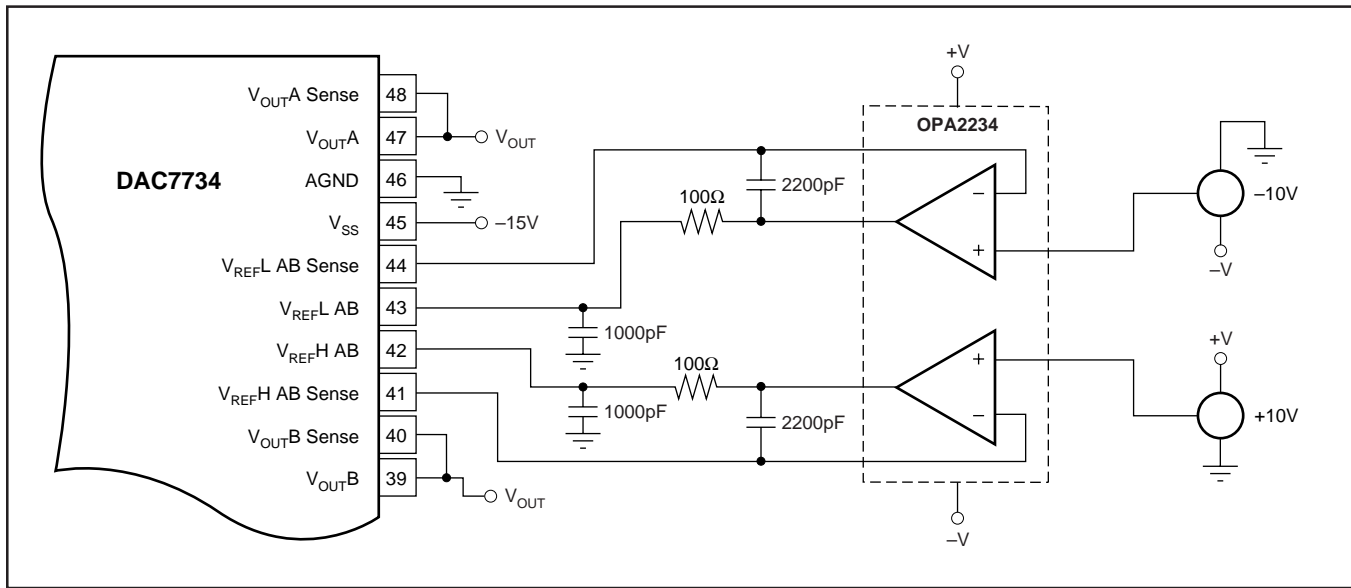


FIGURE 5. Dual Supply Configuration-Buffered References, used for Dual Supply Performance (1/2 DAC7734).

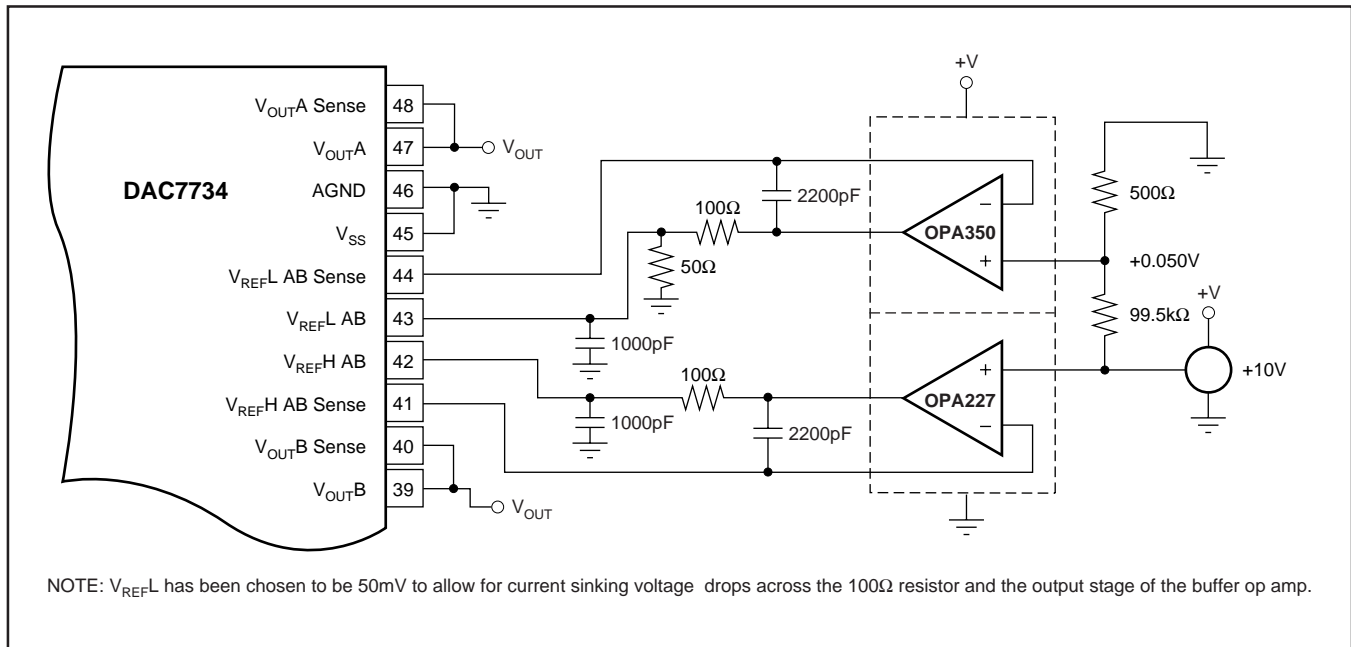


FIGURE 6. Single-Supply Buffered Reference with a Reference Low of 50mV used for Single-Supply Performance Curves (1/2 DAC7734).

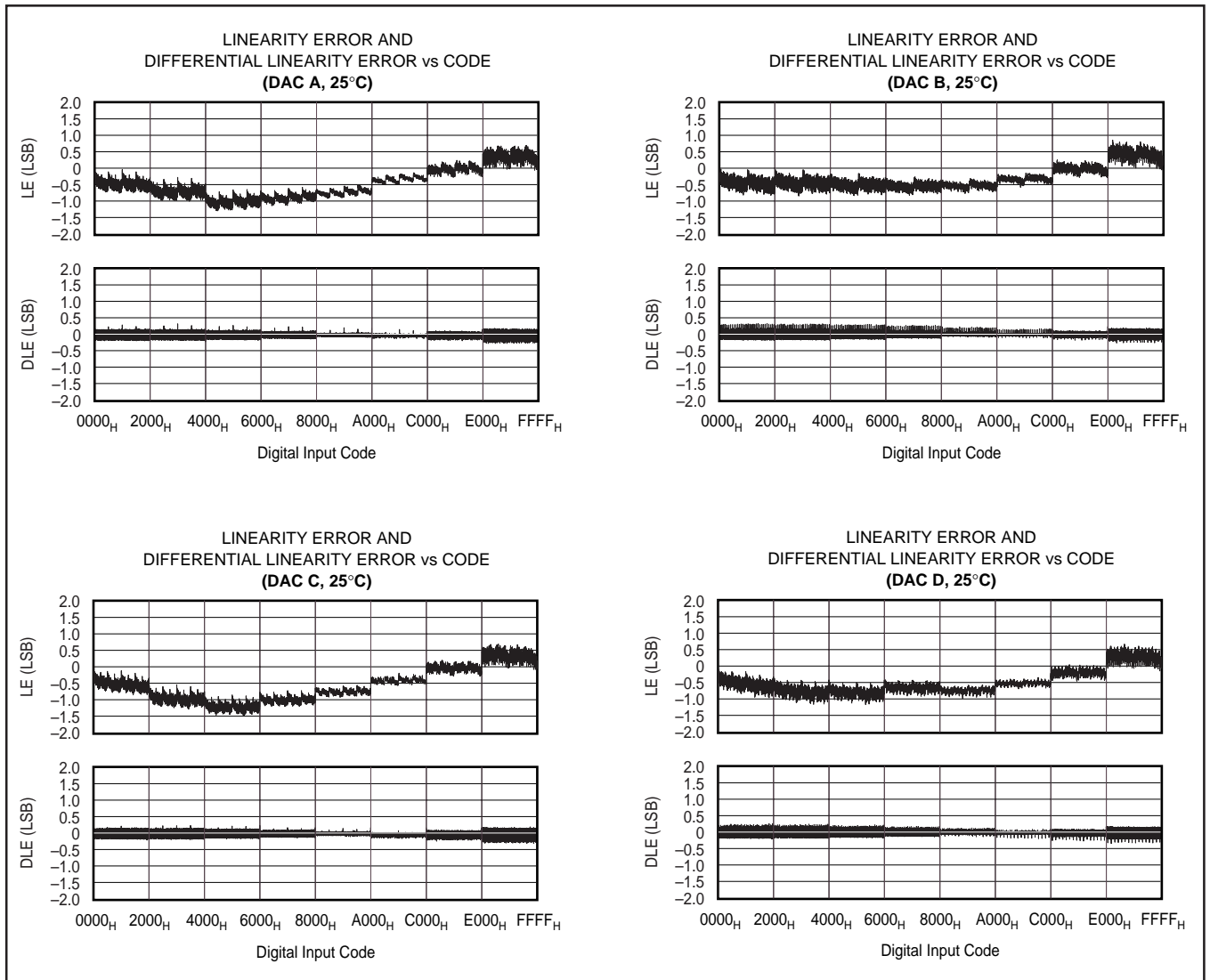


FIGURE 7. Integral Linearity and Differential Linearity Error Curves for Figure 8.

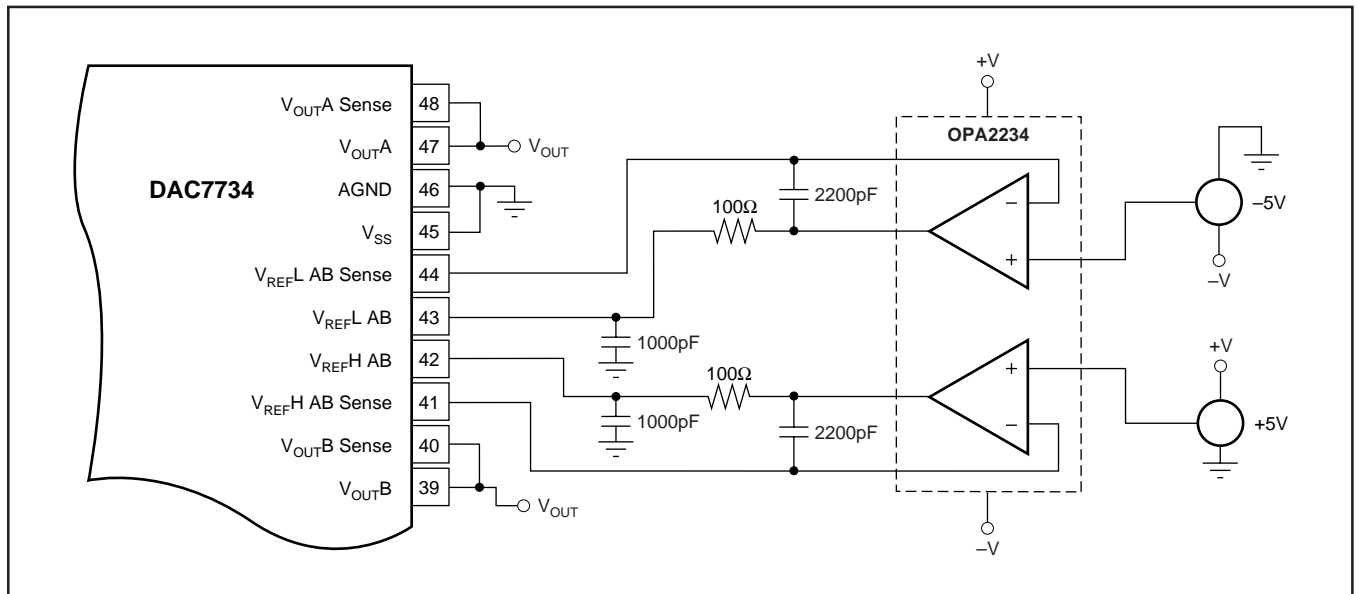


FIGURE 8. Dual-Supply Buffered Reference with  $V_{REFL} = -5V$  and  $V_{REFH} = +5V$  (1/2 DAC7734).

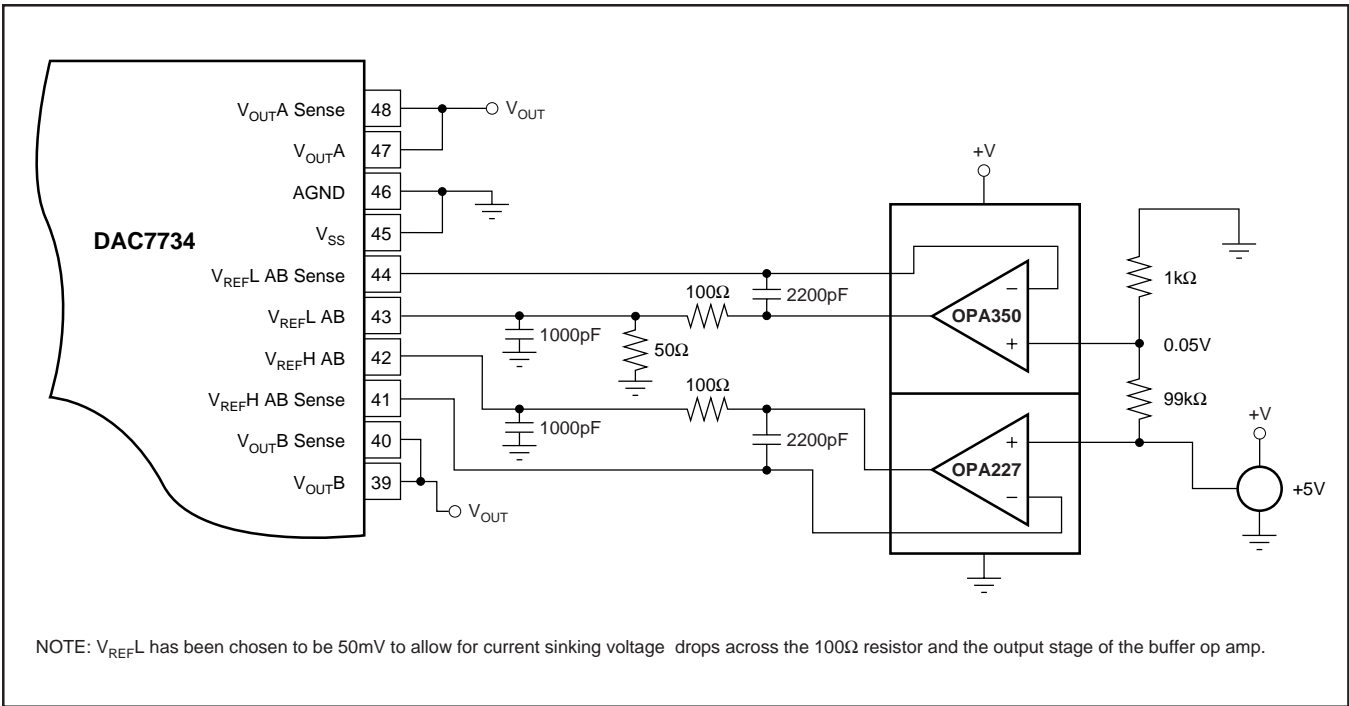


FIGURE 9. Single-Supply Buffered Reference with a Reference Low of 50mV and Reference High of +5V.

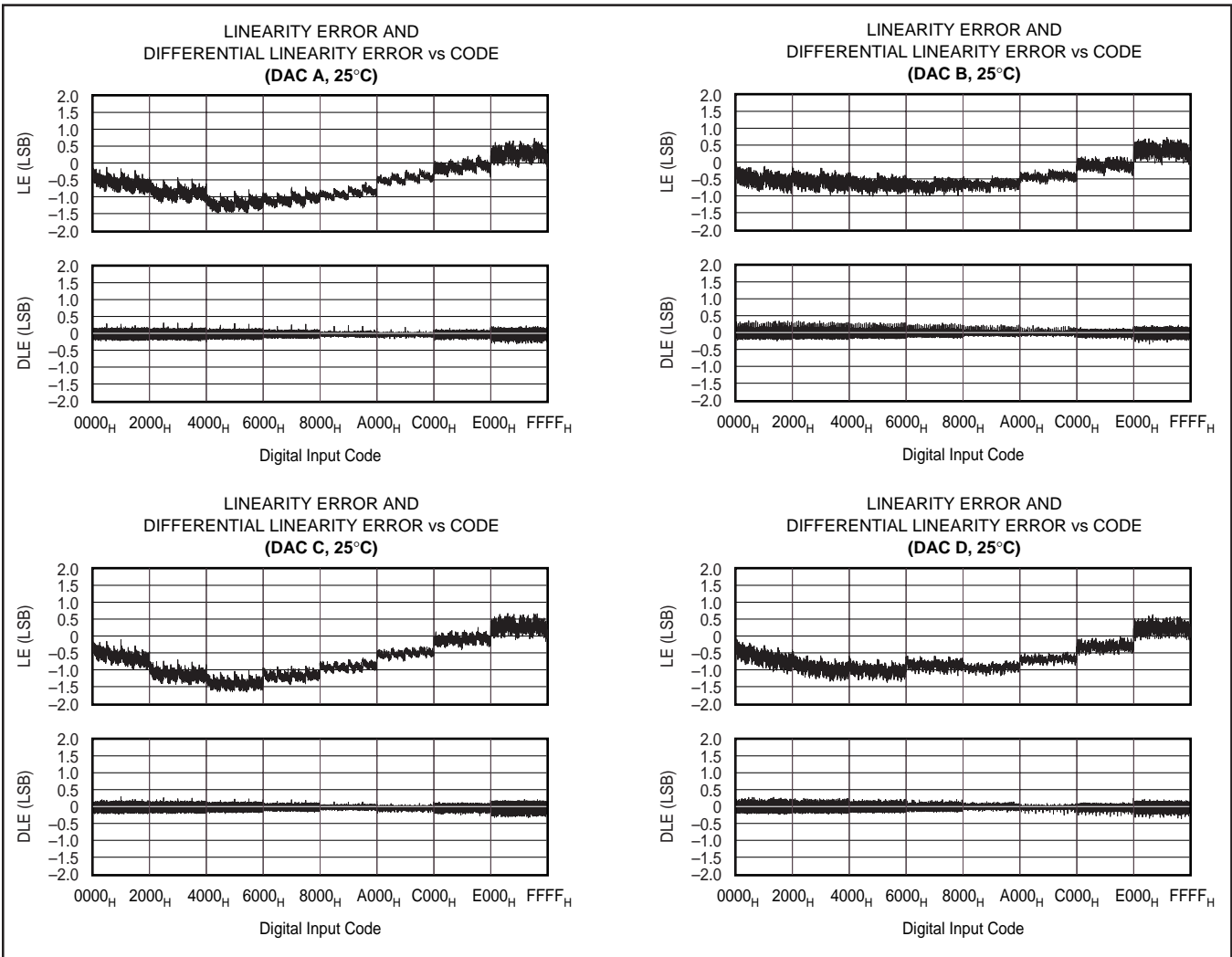


FIGURE 10. Integral Linearity and Differential Linearity Error Curves for Figure 9.

## DIGITAL INTERFACE

Table I shows the basic control logic for the DAC7734. The interface consists of a Signal Data Clock (CLK) input, Serial Data (SDI), DAC Input Register Load Control Signal ( $\overline{\text{LOAD}}$ ), and DAC Register Load Control Signal (LDAC). In addition, a Chip Select ( $\overline{\text{CS}}$ ) input is available to enable serial communication when there are multiple serial devices. An asynchronous Reset (RST) input, by the rising edge, is provided to simplify start-up conditions, periodic resets, or emergency resets to a known state, depending on the status of the reset select (RSTSEL) signal.

The DAC code, quick load control, and address are provided via a 24-bit serial interface (see Table I). The first two bits shifted into the shift register, B23 and B22, are the DAC register address. These bits select the input register that will be updated when  $\overline{\text{LOAD}}$  goes LOW. The third bit, B21, is a “Quick Load” bit such that if HIGH, the code in the shift register is loaded into ALL DAC input registers when the  $\overline{\text{LOAD}}$  signal goes LOW, independent of the state of the address bits, B23 and B22. If the “Quick Load” bit is LOW, the contents of the shift register is loaded only to the DAC register that is addressed. Bits B20 through B16 are not used and can assume any logical value. The last sixteen bits, B15 through B0, make up the DAC code to be loaded into the selected input register.

The internal DAC register is edge triggered and not level triggered. When the LDAC signal is transitioned from LOW to HIGH, the digital word currently in the DAC input register is latched. The first set of registers (the DAC input registers) are level triggered via the  $\overline{\text{LOAD}}$  signal. This double-buffered architecture has been designed so that new data can be entered for each DAC without disturbing the analog outputs. When the new data has been entered into the

device, all of the DAC outputs can be updated simultaneously by the rising edge of LDAC. Additionally, it allows the DAC input registers to be written to at any point, then the DAC output voltages can be synchronously changed via a trigger signal (LDAC).

Note that  $\overline{\text{CS}}$  and CLK are combined with an OR gate, which controls the serial-to-parallel shift register. These two inputs are completely interchangeable. In addition, care must be taken with the state of CLK when  $\overline{\text{CS}}$  rises at the end of a serial transfer. If CLK is LOW when  $\overline{\text{CS}}$  rises, the OR gate will provide a rising edge to the shift register, shifting the internal data one additional bit. The result will be incorrect data and possible selection of the wrong input register(s). If both  $\overline{\text{CS}}$  and CLK are used,  $\overline{\text{CS}}$  should rise only when CLK is HIGH. If not, then either  $\overline{\text{CS}}$  or CLK can be used to operate the shift register. See Table II for more information.

| $\overline{\text{CS}}^{(1)}$ | CLK <sup>(1)</sup>        | $\overline{\text{LOAD}}$ | RST                       | SERIAL SHIFT REGISTER |
|------------------------------|---------------------------|--------------------------|---------------------------|-----------------------|
| H <sup>(2)</sup>             | X <sup>(3)</sup>          | H                        | H                         | No Change             |
| L <sup>(4)</sup>             | L                         | H                        | H                         | No Change             |
| L                            | $\uparrow$ <sup>(5)</sup> | H                        | H                         | Advanced One Bit      |
| $\uparrow$                   | L                         | H                        | H                         | Advanced One Bit      |
| H <sup>(6)</sup>             | X                         | L <sup>(7)</sup>         | H                         | No Change             |
| H <sup>(6)</sup>             | X                         | H                        | $\uparrow$ <sup>(8)</sup> | No Change             |

NOTES: (1)  $\overline{\text{CS}}$  and CLK are interchangeable. (2) H = Logic HIGH. (3) X = Don't Care. (4) L = Logic LOW (5) = Positive Logic Transition. (6) A HIGH value is suggested in order to avoid a “false clock” from advancing the shift register and changing the shift register. (7) If data is clocked into the serial register while  $\overline{\text{LOAD}}$  is LOW, the selected DAC register will change as the shift register bits “flow” through A1 and A0. This will corrupt the data in each DAC register that has been erroneously selected. (8) Rising edge of RST causes no change in the contents of the serial shift register.

TABLE II. Serial Shift Register Truth Table.

## SERIAL DATA INPUT

| B23 | B22 | B21        | B20 | B19 | B18 | B17 | B16 | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----|-----|------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| A1  | A0  | QUICK LOAD | X   | X   | X   | X   | X   | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| A1 | A0 | $\overline{\text{CS}}$ | RST        | RSTSEL | LDAC       | $\overline{\text{LOAD}}$ | INPUT REGISTER    | DAC REGISTER      | MODE              | DAC |
|----|----|------------------------|------------|--------|------------|--------------------------|-------------------|-------------------|-------------------|-----|
| L  | L  | L                      | H          | X      | X          | L                        | Write             | Hold              | Write Input       | A   |
| L  | H  | L                      | H          | X      | X          | L                        | Write             | Hold              | Write Input       | B   |
| H  | L  | L                      | H          | X      | X          | L                        | Write             | Hold              | Write Input       | C   |
| H  | H  | L                      | H          | X      | X          | L                        | Write             | Hold              | Write Input       | D   |
| X  | X  | H                      | H          | X      | $\uparrow$ | H                        | Hold              | Write             | Update            | All |
| X  | X  | H                      | H          | X      | H          | H                        | Hold              | Hold              | Hold              | All |
| X  | X  | X                      | $\uparrow$ | L      | X          | X                        | Reset to Zero     | Reset to Zero     | Reset to Zero     | All |
| X  | X  | X                      | $\uparrow$ | H      | X          | X                        | Reset to Midscale | Reset to Midscale | Reset to Midscale | All |

TABLE I. DAC7734 Logic Truth Table.

## SERIAL-DATA OUTPUT

The Serial-Data Output (SDO) is the internal shift register's output. For DAC7734, the SDO is a driven output and does not require an external pull-up. Any number of DAC7734's can be daisy chained by connecting the SDO pin of one device to the SDI pin of the following device in the chain, as shown in Figure 11.

## DIGITAL TIMING

Figure 12 and Table III provide detailed timing for the digital interface of the DAC7734.

## DIGITAL INPUT CODING

The DAC7734 input data is in Straight Binary format. The output voltage is given by Equation 1.

where N is the digital input code. This equation does not

$$V_{OUT} = V_{REFL} + \frac{(V_{REFH} - V_{REFL}) \cdot N}{65,536} \quad (1)$$

include the effects of offset (zero-scale) or gain (full-scale) errors.

## DIGITALLY-PROGRAMMABLE CURRENT SOURCE

The DAC7734 offers a unique set of features that allows a wide range of flexibility in designing applications circuits such as programmable current sources. The DAC7734 offers both a differential reference input, as well as an open-loop configuration around the output amplifier. The open-loop configuration around the output amplifier allows a transistor to be placed within the loop to implement a digitally-programmable, unidirectional current source. The availability of a differential reference allows programmability for both the full-scale and zero-scale currents. The output current is calculated as:

$$I_{OUT} = \left( \left( \frac{V_{REFH} - V_{REFL}}{R_{SENSE}} \right) \cdot \left( \frac{N}{65,536} \right) \right) + (V_{REFL} / R_{SENSE}) \quad (2)$$

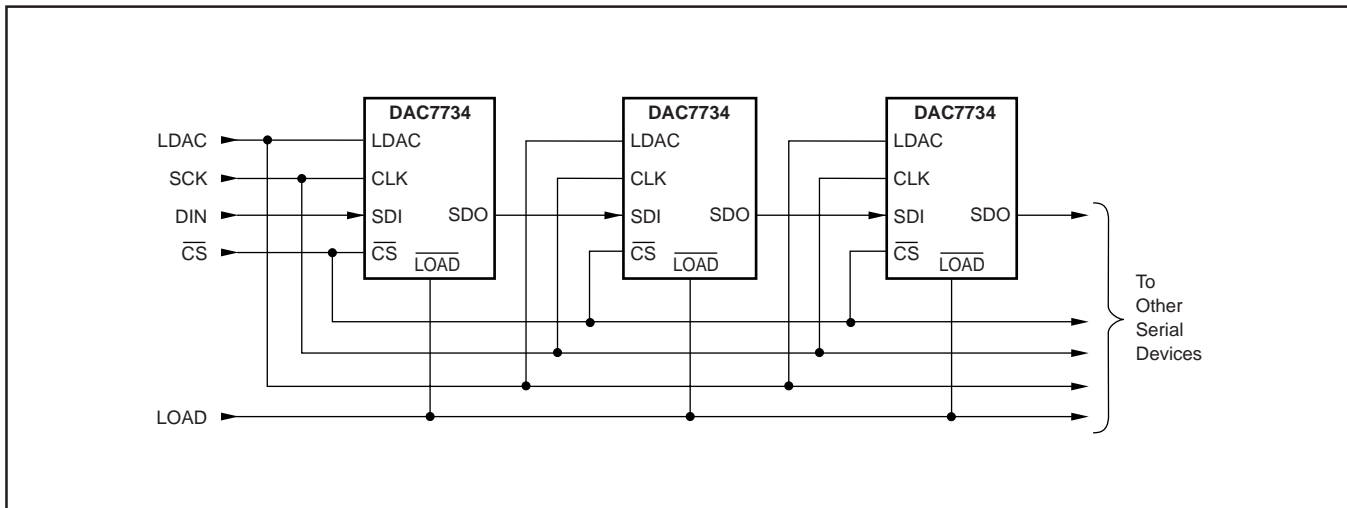


FIGURE 11. Daisy-Chaining DAC7734.

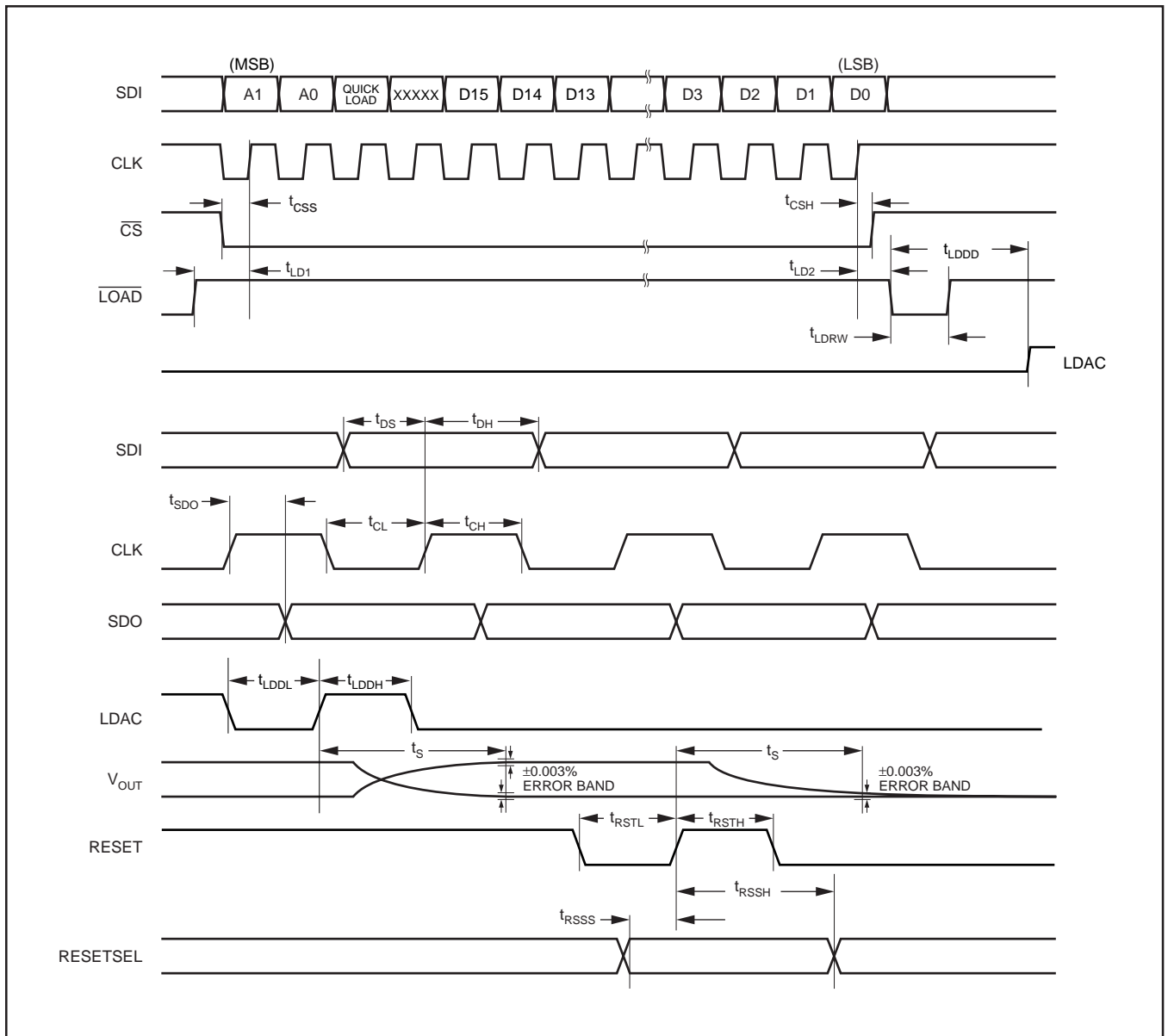


FIGURE 12. Digital Input and Output Timing.

| SYMBOL      | DESCRIPTION                        | MIN | MAX                   | UNITS   |
|-------------|------------------------------------|-----|-----------------------|---------|
| $t_{DS}$    | Data Valid to CLK Rising           | 10  |                       | ns      |
| $t_{DH}$    | Data Held Valid after CLK Rises    | 20  |                       | ns      |
| $t_{CH}$    | CLK HIGH                           | 25  |                       | ns      |
| $t_{CL}$    | CLK LOW                            | 25  |                       | ns      |
| $t_{CSS}$   | $\overline{CS}$ LOW to CLK Rising  | 15  |                       | ns      |
| $t_{CSH}$   | CLK HIGH to $\overline{CS}$ Rising | 0   |                       | ns      |
| $t_{LD1}$   | LOAD HIGH to CLK Rising            | 10  |                       | ns      |
| $t_{LD2}$   | CLK Rising to LOAD LOW             | 30  |                       | ns      |
| $t_{LDRW}$  | LOAD LOW Time                      | 30  |                       | ns      |
| $t_{LDDWL}$ | LDAC LOW Time                      | 40  |                       | ns      |
| $t_{LDDH}$  | LDAC HIGH Time                     | 40  |                       | ns      |
| $t_{SDO}$   | SDO Propagation Delay              | 10  | 45                    | ns      |
| $t_{RSSS}$  | RESETSEL Valid to RESET HIGH       | 0   |                       | ns      |
| $t_{RSSH}$  | RESET HIGH to RESETSEL Not Valid   | 100 |                       | ns      |
| $t_{RSTL}$  | RESET LOW Time                     | 10  |                       | ns      |
| $t_{RSTH}$  | RESET HIGH Time                    | 10  |                       | ns      |
| $t_{LDDD}$  | LOAD LOW to LDAC Rising Time       | 40  |                       | ns      |
| $t_S$       | Settling Time                      |     | 10 (dual)/11 (single) | $\mu$ s |

TABLE III. Timing Specifications ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ).

Figure 13 shows a DAC7734 in a 4mA to 20mA current output configuration. The output current can be determined by Equation 3:

$$I_{OUT} = \left( \left( \frac{5V - 1V}{250\Omega} \right) \cdot \left( \frac{N}{65,536} \right) \right) + \left( \frac{1V}{250\Omega} \right) \quad (3)$$

At full-scale, the output current is 16mA, plus the 4mA, for the zero current. At zero scale the output current is the offset current of 4mA (1V/250Ω).

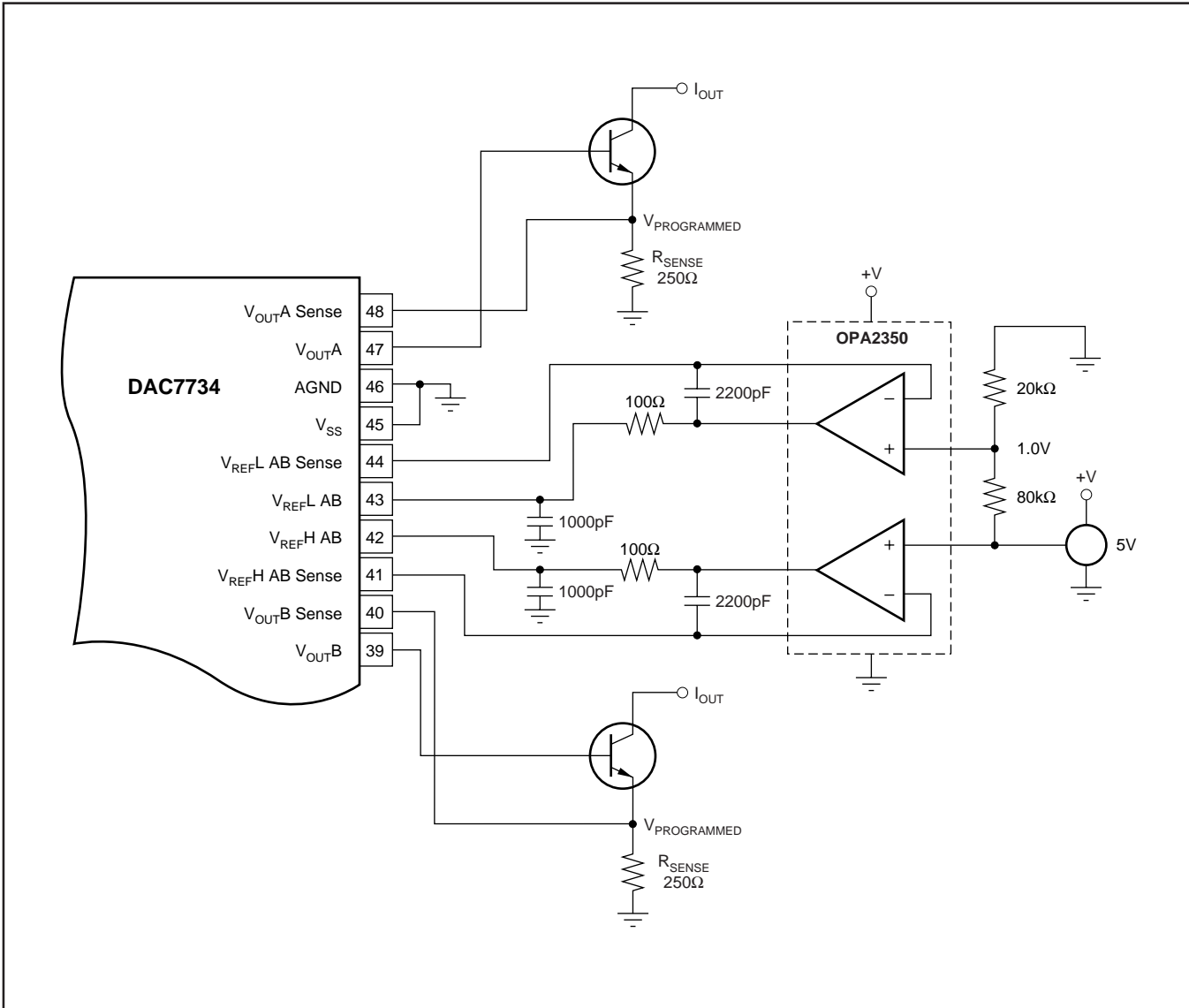


FIGURE 13. 4-to-20mA Digitally Controlled Current Source (1/2 DAC7734).

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| DAC7734E         | ACTIVE                | SSOP         | DL              | 48   | 30          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7734E/1K      | ACTIVE                | SSOP         | DL              | 48   | 1000        | TBD                     | CU NIPDAU        | Level-3-220C-168 HR          |
| DAC7734E/1KG4    | ACTIVE                | SSOP         | DL              | 48   | 1000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7734EB        | ACTIVE                | SSOP         | DL              | 48   | 30          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7734EB/1K     | ACTIVE                | SSOP         | DL              | 48   | 1000        | TBD                     | CU NIPDAU        | Level-3-220C-168 HR          |
| DAC7734EB/1KG4   | ACTIVE                | SSOP         | DL              | 48   |             | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7734EBG4      | ACTIVE                | SSOP         | DL              | 48   | 30          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7734EC        | ACTIVE                | SSOP         | DL              | 48   | 30          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7734EC/1K     | ACTIVE                | SSOP         | DL              | 48   | 1000        | TBD                     | CU NIPDAU        | Level-3-220C-168 HR          |
| DAC7734EC/1KG4   | ACTIVE                | SSOP         | DL              | 48   | 1000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7734ECG4      | ACTIVE                | SSOP         | DL              | 48   | 30          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| DAC7734EG4       | ACTIVE                | SSOP         | DL              | 48   | 30          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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