

CD4078B Types

CMOS 8-Input NOR/OR Gate

High-Voltage Types (20-Volt Rating)

■ **CD4078B NOR/OR Gate** provides the system designer with direct implementation of the positive-logic 8-input NOR and OR functions and supplements the existing family of CMOS gates.

The CD4078B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline package (NSR suffix), and in chip form (H suffix).

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to $V_{DD} + 0.5V$
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DC INPUT CURRENT, ANY ONE INPUT ±10mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ 500mW

For $T_A = +100^{\circ}\text{C}$ to $+125^{\circ}\text{C}$Derate Linearity at $12\text{mW}/^{\circ}\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)..... 100mW

OPERATING-TEMPERATURE RANGE (T_A).....-55°C to +125°C

STORAGE TEMPERATURE RANGE (T_{stg})	-65°C to +150°C
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LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10s max +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	Min.	Max.	Units
Supply-Voltage Range (For T_A Full Package Temperature Range)	3	18	V

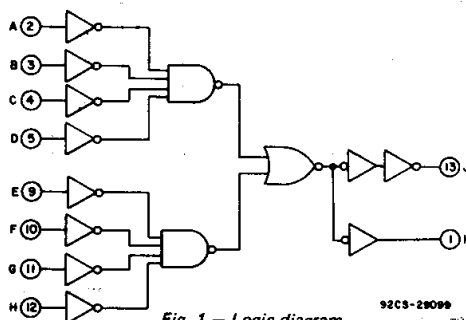


Fig. 1 — Logic diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_I = 50\text{ pF}$, $R_I = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		V _{DD} VOLTS	TYP.	MAX.	
Propagation Delay Time, t _{PHL} , t _{PLH}		5	150	300	ns
		10	75	150	
		15	55	110	
Transition Time, t _{THL} , t _{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C _{IN}	Any Input		5	7.5	pF

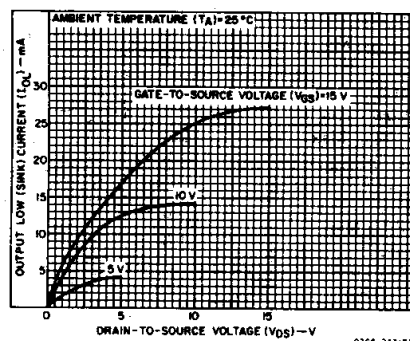
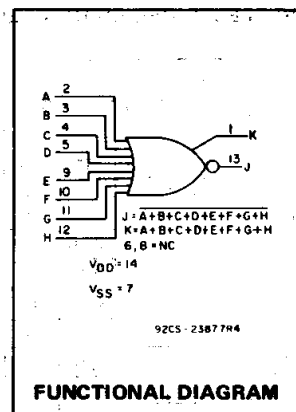


Fig. 2 — Typical output low (sink) current characteristics.

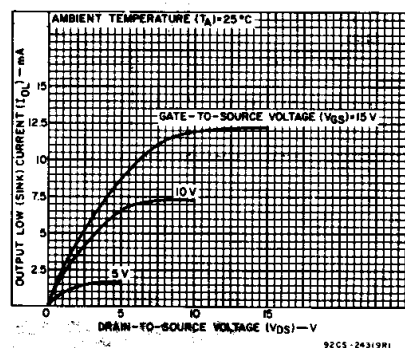


Fig. 3 — Minimum output low (sink) current characteristics.

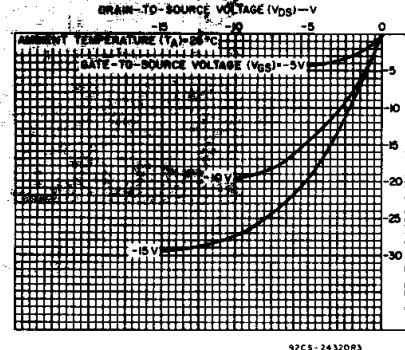


Fig. 4 — Typical output high (source) current characteristics.

**COMMERCIAL CMOS
HIGH VOLTAGE ICs**

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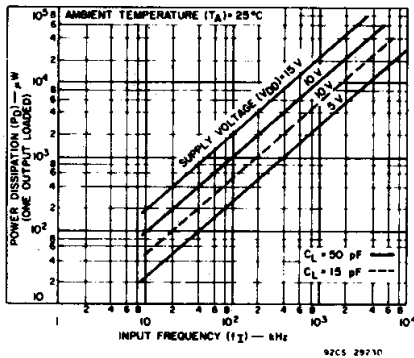


Fig. 10 - Typical dynamic power dissipation as a function of frequency.

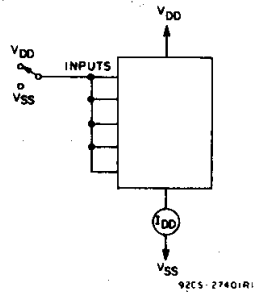


Fig. 11 - Quiescent-device-current test circuit.

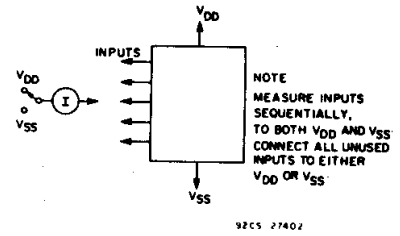


Fig. 12 - Input current test circuit.

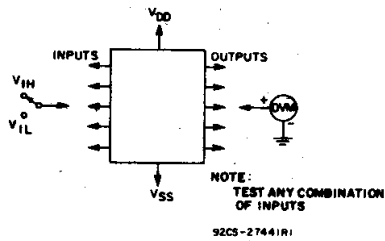


Fig. 13 - Input-voltage test circuit.

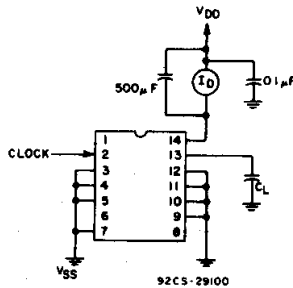
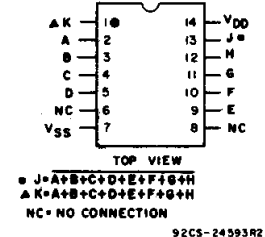
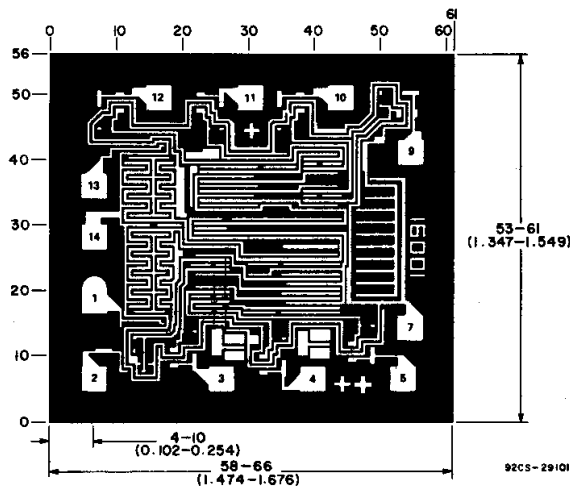


Fig. 14 - Dynamic power dissipation test circuit.



TERMINAL ASSIGNMENT



Dimensions and pad layout for CD4078BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

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