

CD40107B Types

CMOS Dual 2-Input NAND Buffer/Driver

High-Voltage Type (20-Volt Rating)

The CD40107B is a dual 2-input NAND buffer/driver containing two independent 2-input NAND buffers with open-drain single n-channel transistor outputs. This device features a wired-OR capability and high output sink current capability (136 mA typ. at $V_{DD} = 10\text{ V}$, $V_{DS} = 1\text{ V}$). The CD40107B is supplied in 8-lead hermetic dual-in-line ceramic packages (F3A suffix), 8-lead dual-in-line plastic packages (E suffix), 8-lead small-outline packages (M, M96, MT, and PSR suffixes), and 8-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- 32 times standard B-Series output current drive sinking capability – 136 mA typ. @ $V_{DD} = 10\text{ V}$, $V_{DS} = 1\text{ V}$
- 100% tested for quiescent current at 20 V
- Maximum input current of $1\ \mu\text{A}$ at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Noise margin, full package temperature range, R_L to $V_{DD} = 10\text{ k}\Omega$:
1 V at $V_{DD} = 5\text{ V}$
2 V at $V_{DD} = 10\text{ V}$
2.5 V at $V_{DD} = 15\text{ V}$
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

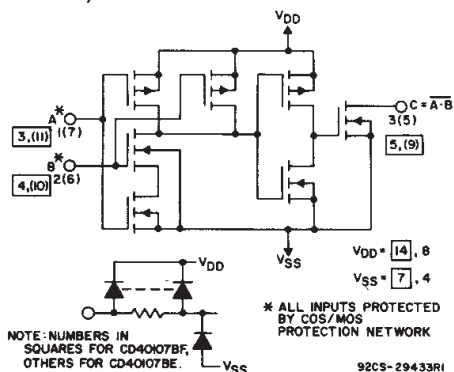
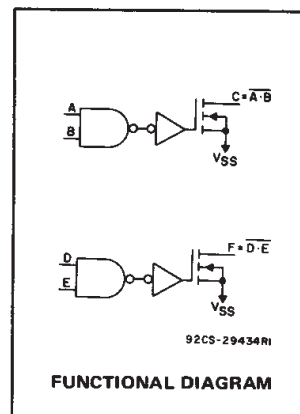


Fig.1 – Schematic diagram of CD40107B (one of 2 gates)

TRUTH TABLE			
A	B	C	
0	0	1*	Z#
1	0	1*	Z#
0	1	1*	Z#
1	1	0	

*Requires external pull-up resistor (R_L) to V_{DD} .

#Without pull-up resistor. (3-state).

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	-0.5V to +20V
Voltages referenced to V_{SS} Terminal	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to $V_{DD} + 0.5\text{V}$
DC INPUT CURRENT, ANY ONE INPUT	$\pm 10\text{ mA}$
POWER DISSIPATION PER PACKAGE (P_D):		
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$	500mW
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$	Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR		
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$	100mW
OPERATING-TEMPERATURE RANGE (T_A)	-55°C to $+125^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65°C to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):		
At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79mm) from case for 10s max	$+265^\circ\text{C}$

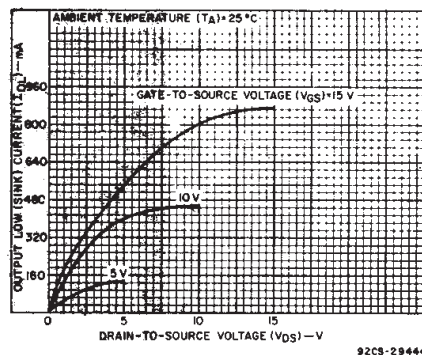


Fig.2 – Typical output low (sink) current characteristics.

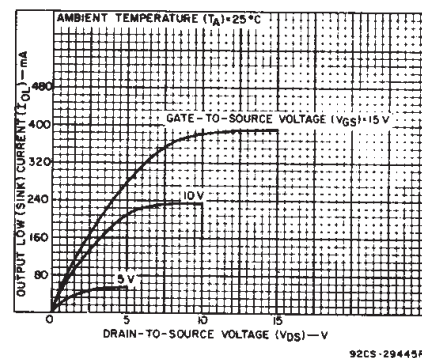


Fig.3 – Minimum output low (sink) current characteristics.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A = \text{Full Package-Temperature Range}$)	3	18	V

CD40107B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, Input $t_r, t_f = 20\text{ ns}$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		V _{DD} Volts	Typ.	Max.	
Propagation Delay: High-to-Low, t_{PHL}	$R_L^* = 120\ \Omega$	5	100	200	ns
		10	45	90	
		15	30	60	
Low-to-High, t_{PLH}	$R_L^* = 120\ \Omega$	5	100	200	ns
		10	60	120	
		15	50	100	
Transition Time: High-to-Low, t_{THL}	$R_L^* = 120\ \Omega$	5	50	100	ns
		10	20	40	
		15	10	20	
Low-to-High, t_{TLH}	$R_L^* = 120\ \Omega$	5	50	100	ns
		10	35	70	
		15	25	50	
Average Input Capacitance, C_{IN}	Any Input		5	7.5	pF
Average Output Capacitance, C_{OUT}	Any Output		30	—	pF

* R_L is external pull-up resistor to V_{DD} .

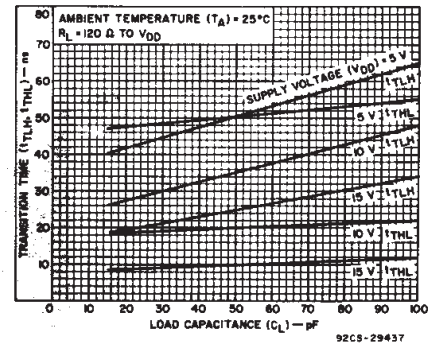


Fig. 4 — Typical transition time as a function of load capacitance.

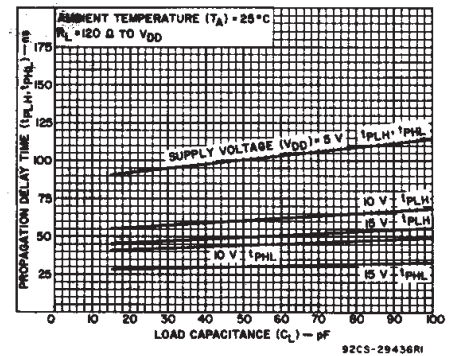


Fig. 5 — Typical propagation delay time as a function of load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES ($^\circ\text{C}$)							UNITS
				+25							
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current I_{DD} Max.	—	0,5	5	1	1	30	30	—	0.02	1	μA
	—	0,10	10	2	2	60	60	—	0.02	2	
	—	0,15	15	4	4	120	120	—	0.02	4	
	—	0,20	20	20	20	600	600	—	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0,4	0,5	5	21	20	14	12	16	32	—	mA
	1	0,5	5	44	42	30	25	34	68	—	
	0,5	0,10	10	49	46	32	28	37	74	—	
	1	0,10	10	89	85	60	51	68	136	—	
Output High (Source) Current I_{OH} Min.	0,5	0,15	15	66	63	44	38	50	100	—	
	No Internal Pull-Up Device										
Input Low Voltage V_{IL} Max.*	4,5	—	5	1,5				—	—	1,5	V
	9	—	10	3				—	—	3	
	13,5	—	15	4				—	—	4	
Input High Voltage V_{IH} Min.*	0,5,4,5	—	5	3,5				3,5	—	—	
	1,9	—	10	7				7	—	—	
	1,5,13,5	—	15	11				11	—	—	
Input Current I_{IN} Max.	—	0,18	18	$\pm 0,1$	$\pm 0,1$	± 1	± 1	—	$\pm 10^{-5}$	$\pm 0,1$	μA
Output Leakage Current I_{OZ} Max.	18	0,18	18	2	2	20	20	—	10^{-4}	2	μA

* Measured with external pull-up resistor, $R_L = 10\text{ k}\Omega$ to V_{DD} .

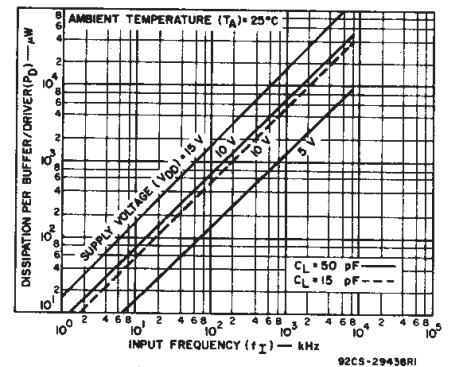


Fig. 6 — Typical power dissipation as a function of input frequency.

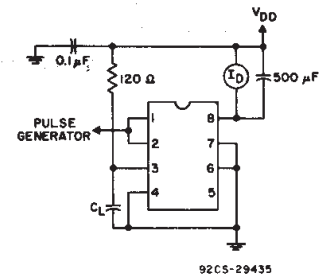
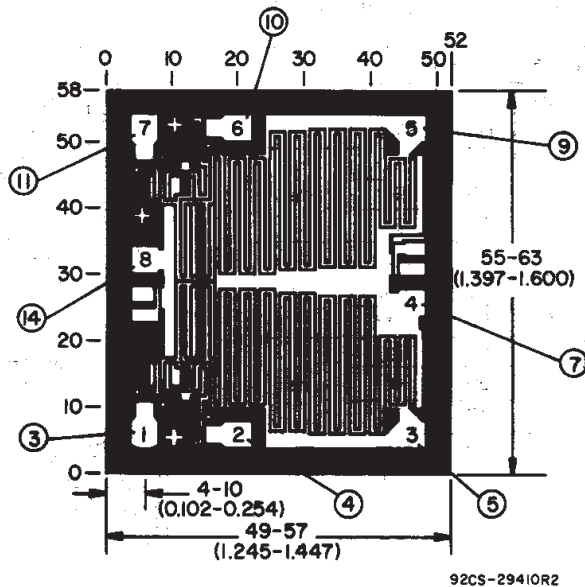


Fig. 7 — Power-dissipation test circuit for CD40107BE.

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD40107B Types



NOTE: NOS. IN PADS FOR CD40107BE
NOS. OUTSIDE CHIP FOR CD40107BF

Dimensions and Pad Layout for CD40107BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

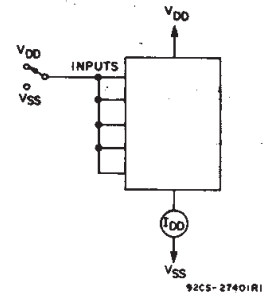


Fig. 8 - Quiescent-device current test circuit.

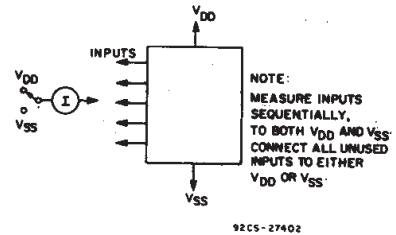
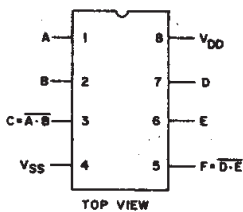
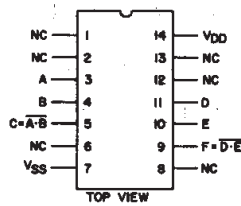


Fig. 9 - Input-current test circuit.

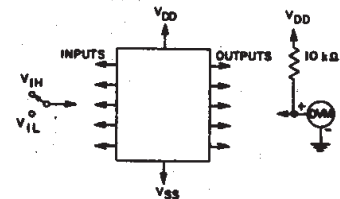


CD40107BE



CD40107BF

TERMINAL ASSIGNMENTS



NOTE: TEST ANY COMBINATION OF INPUTS

Fig. 10 - Input-voltage test circuit.

Special Considerations for CD40107B

1. Limiting Capacitive Currents for $C_L > 500$ pF, $V_{DD} > 15$ V.

For $V_{DD} > 15$ V, and load capacitance (C_L) from output to ground > 500 pF, an external 25Ω series limiting resistor should be inserted between the output terminal and C_L . No external resistor is necessary if $C_L < 500$ pF or $V_{DD} < 15$ V.

2. Driving Inductive Loads

When using the CD40107B to drive inductive loads, the load should be shunted with a diode to prevent high voltages from developing across the CD40107B output.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
Low Power Wireless	www.ti.com/lpw

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2007, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD40107BE	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD40107BEE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD40107BF	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD40107BF3A	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD40107BM	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40107BM96	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40107BM96E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40107BM96G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40107BME4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40107BMG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40107BMT	ACTIVE	SOIC	D	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40107BMTE4	ACTIVE	SOIC	D	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40107BMTG4	ACTIVE	SOIC	D	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40107BPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40107BPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40107BPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40107BPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40107BPWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40107BPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40107BPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40107BPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD40107BPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

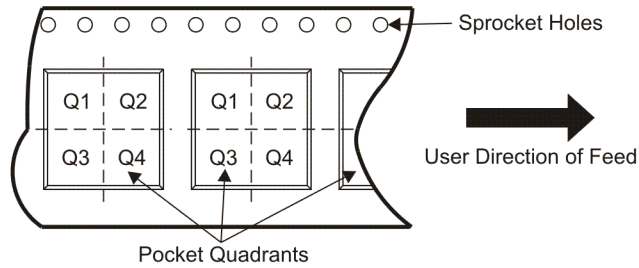
Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD40107BM96	SOIC	D	8	2500	330.0	12.0	6.0	5.0	2.0	8.0	12.0	Q1
CD40107BM96	SOIC	D	8	2500	330.0	12.0	6.0	5.0	2.0	8.0	12.0	Q1
CD40107BPSR	SO	PS	8	2000	330.0	16.0	8.0	7.0	3.0	12.0	16.0	Q1
CD40107BPWR	TSSOP	PW	8	2000	330.0	12.0	7.0	4.0	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD40107BM96	SOIC	D	8	2500	343.0	338.0	21.0
CD40107BM96	SOIC	D	8	2500	346.0	346.0	29.0
CD40107BPSR	SO	PS	8	2000	346.0	346.0	33.0
CD40107BPWR	TSSOP	PW	8	2000	346.0	346.0	29.0

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

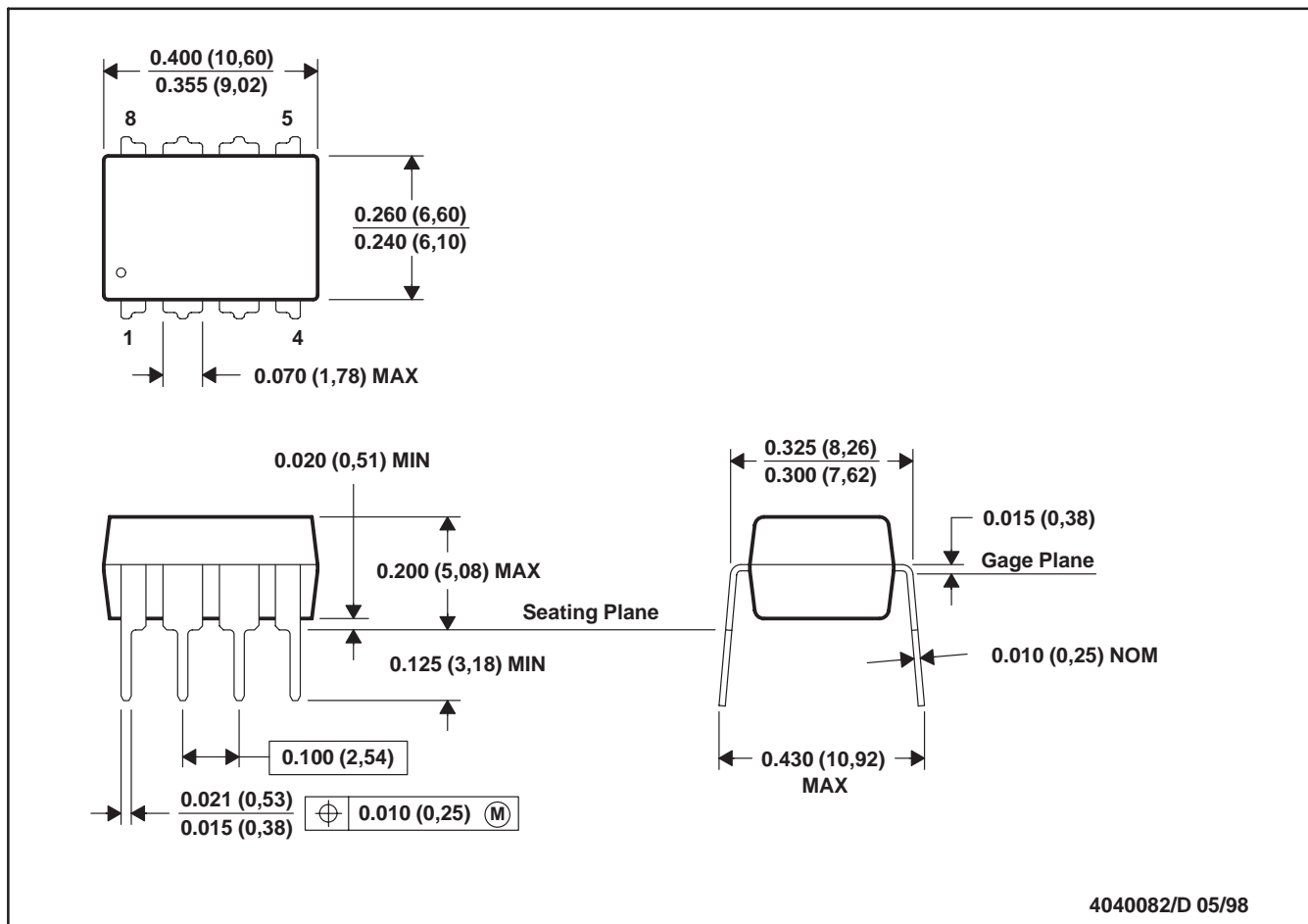


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



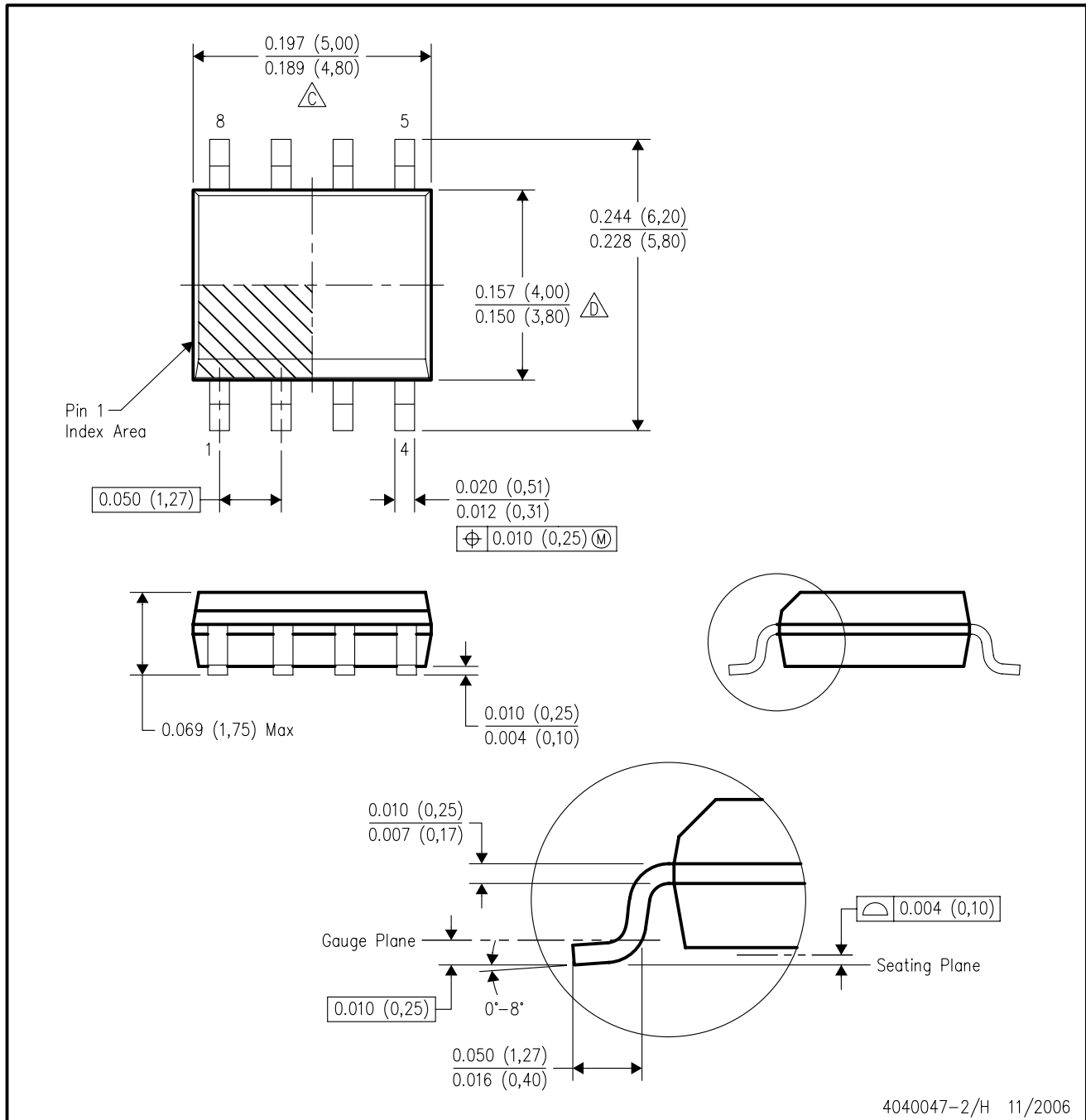
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm



D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

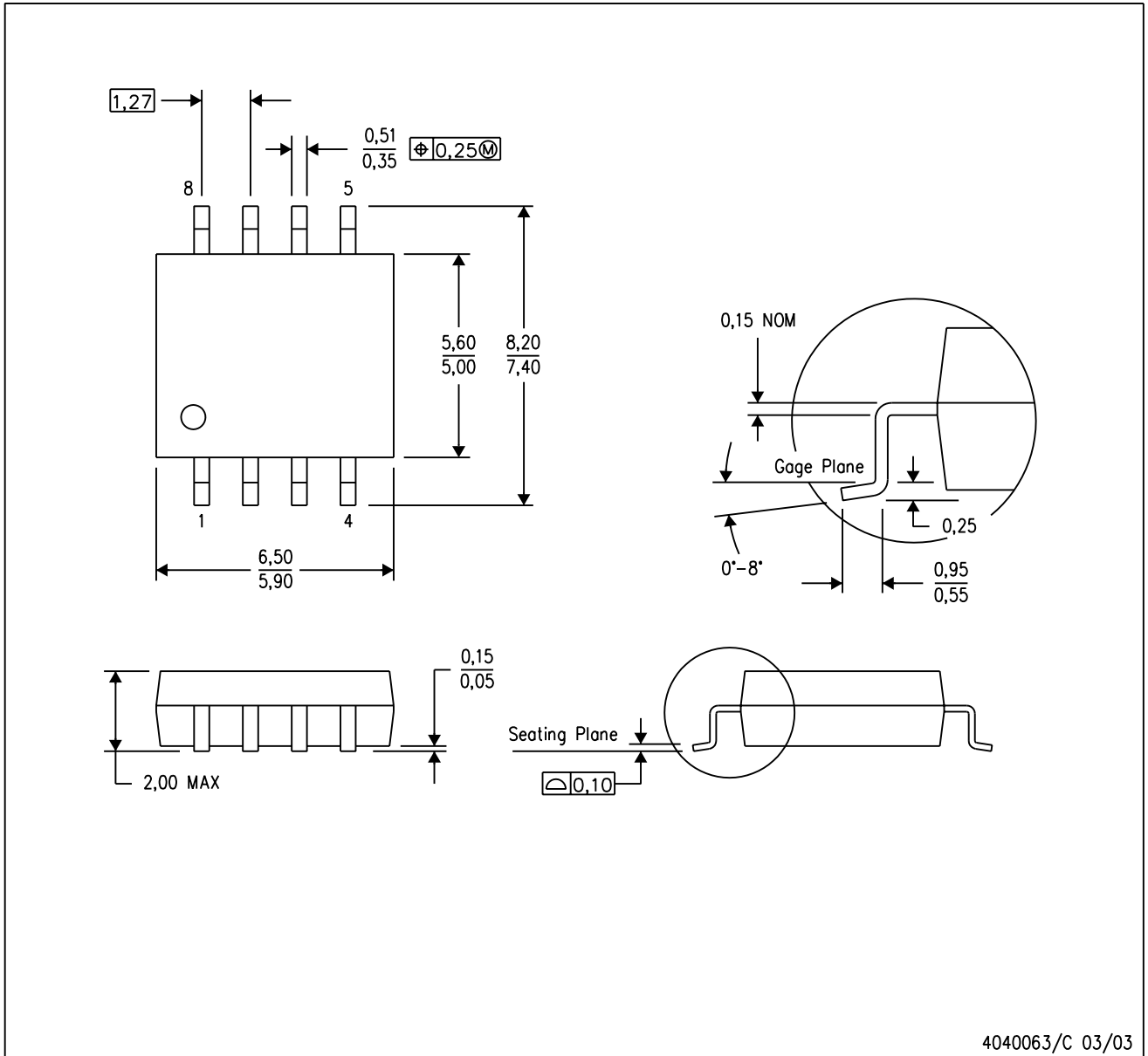


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153