SINGLE-CHIP LI-ION CHARGE AND SYSTEM POWER-PATH MANAGEMENT IC

Check for Samples: bq24070, bq24071

FEATURES

- **Small 3,5 mm × 4,5 mm QFN Package**
- **Designed for Single-Cell Li-Ion- or Li-Polymer-Based Portable Applications**
- **Integrated Dynamic Power-Path Management (DPPM) Feature Allowing the AC Adapter to Simultaneously Power the System and Charge the Battery**
- **Power Supplement Mode Allows Battery to Supplement the AC Input Current**
- **Autonomous Power Source Selection (AC Adapter or BAT)**
- **Supports Up to 2 Amps Total Current**
- **Thermal Regulation for Charge Control**
- **Charge Status Outputs for LED or System Interface Indicates Charge and Fault Conditions**
- **Reverse Current, Short-Circuit, and Thermal Protection**
- **Power Good Status Outputs**
- **4.4-V and 6-V Options for System Output Regulation Voltage**

APPLICATIONS

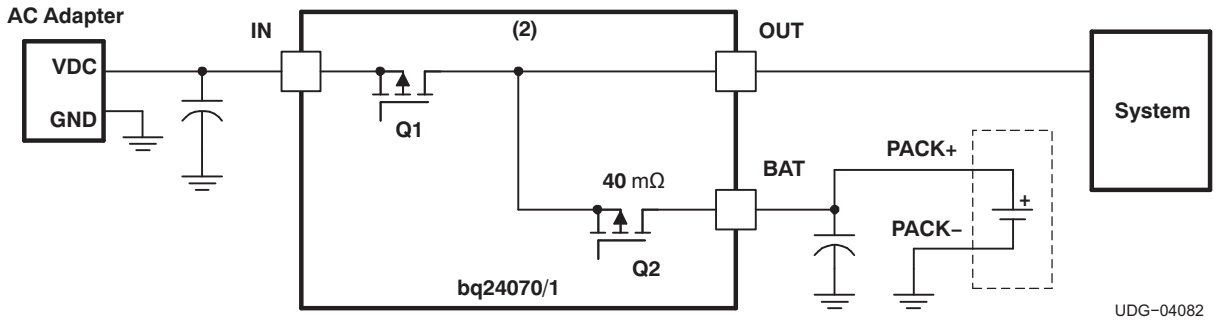
- **Smart Phones and PDA**
- **MP3 Players**
- **Digital Cameras and Handheld Devices**
- **Internet Appliances**

DESCRIPTION

The bq24070 and bq24071 are highly integrated Li-ion linear charger and system power-path management devices targeted at space-limited portable applications. The bq24070/1 offer DC supply (AC adapter) power-path management with autonomous power-source selection, power FETs and current sensors, high-accuracy current and voltage regulation, charge status, and charge termination, in a single monolithic device.

The bq24070/1 power the system while independently charging the battery. This feature reduces the charge and discharge cycles on the battery, allows for proper charge termination and allows the system to run with an absent or defective battery pack. This feature also allows for the system to instantaneously turn on from an external power source in the case of a deeply discharged battery pack. The IC design is focused on supplying continuous power to the system when available from the AC adapter or battery sources.

POWER FLOW DIAGRAM



(1) See Figure 2 and functional block diagram for more detailed feature information.

(2) P-FET back gate body diodes are disconnected to prevent body diode conduction.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

The MODE pin selects the priority of the input sources. If an input source is not available, then the battery is selected as the source. With the MODE pin high, the bq24070/1 attempts to charge from the input at the charge rate set by ISET1 pin. With the MODE pin low, the bq24070/1 defaults to USB charging at the charge rate. This feature allows the use of a single connector (mini-USB cable), where the host programs the MODE pin according to the source that is connected (AC adaptor or USB port). Table 1 summarizes the MODE pin function.

Table 1. Power Source Selection Function Summary

MODE STATE	AC ADAPTER	MAXIMUM CHARGE RATE(1)	SYSTEM POWER SOURCE	USB BOOT-UP FEATURE
Low	Present	ISET2	USB	Enabled
	Absent	N/A	Battery	Disabled
High	Present	ISET1	AC	Disabled
	Absent	N/A	Battery	Disabled

(1) Battery charge rate is always set by ISET1, but may be reduced by a limited input source (ISET2 USB mode) and I_{OUT} system load.

ORDERING INFORMATION(1)

T_A	BATTERY VOLTAGE (V)	OUT PIN	PART NUMBER(2) (3)	STATUS	PACKAGE MARKING
–40°C to 125°C	4.2	Regulated to 4.4 V(4)	bq24070RHLR	Production	BRQ
	4.2	Regulated to 4.4 V(4)	bq24070RHLT	Production	BRQ
	4.2	Regulated to 6 V	bq24071RHLR	Production	BTR
	4.2	Regulated to 6 V	bq24071RHLT	Production	BTR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) The RHL package is available in the following options:
R - taped and reeled in quantities of 3,000 devices per reel.
T - taped and reeled in quantities of 250 devices per reel.
(3) This product is RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and is suitable for use in specified lead-free soldering processes. In addition, this product uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.
(4) If AC < $V_{O(OUT-REG)}$, the AC is connected to the OUT pin by a P-FET, (Q1).

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		bq24070/1
Input voltage	IN (DC voltage with respect to VSS)	–0.3 V to 18 V
Input voltage	BAT, CE, DPPM, $\overline{PG}$, Mode, OUT, ISET1, ISET2, STAT1, STAT2, TS, (all DC voltages wrt VSS)	–0.3 V to 7 V
	V_{REF} (DC voltage wrt VSS)	–0.3 V to $V_{O(OUT)}$ + 0.3 V
	TMR	–0.3 V to V_O + 0.3 V
Input current		3.5 A
Output current	OUT	4 A
	BAT(2)	–4 A to 3.5 A
Output source current (in regulation at 3.3 V V_{REF})	V_{REF}	30 mA
Output sink current	$\overline{PG}$, STAT1, STAT2,	15 mA
Storage temperature range, T_{stg}		–65°C to 150°C
Junction temperature range, T_J		–40°C to 150°C
Lead temperature (soldering, 10 seconds)		300°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.
(2) Negative current is defined as current flowing into the BAT pin.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CC}	Supply voltage (V_{IN}) (1)		4.35	16	V
I_{AC}	Input current			2	A
T_J	Operating junction temperature range		–40	125	°C

(1) Verify that power dissipation and junction temperatures are within limits at maximum V_{CC} .

DISSIPATION RATINGS

PACKAGE	$T_A \le 40°C$ POWER RATING	DERATING FACTOR $T_A > 40°C$	θ_{JA}
20-pin RHL(1)	1.81 W	21 mW/°C	46.87 °C/W

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. This is connected to the ground plane by a 2×3 via matrix.

ELECTRICAL CHARACTERISTICS

over junction temperature range (0°C ≤ T_J ≤ 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT BIAS CURRENTS							
$I_{CC(SPLY)}$	Active supply current, VCC		$V_{VCC} > V_{VCC(min)}$		1	2	mA
$I_{CC(SLP)}$	Sleep current (current into BAT pin)		$V_{IN} < V_{(BAT)}$ 2.6 V ≤ $V_{I(BAT)}$ ≤ $V_{O(BAT-REG)}$, Excludes load on OUT pin		2	5	μA
$I_{CC(IN-STDBY)}$	Input standby current		$V_{I(AC)}$ ≤ 6V, Total current into IN pin with chip disabled, Excludes all loads, CE=LOW, after $t_{(CE-HOLDOFF)}$ delay			200	
$I_{CC(BAT-STDBY)}$	BAT standby current		Total current into BAT pin with input present and chip disabled; Excludes all loads, CE=LOW, after $t_{(CE-HOLDOFF)}$ delay, 0°C ≤ T_J ≤ 85°C(1)		45	65	
$I_{IB(BAT)}$	Charge done current, BAT		Charge DONE, input supplying the load		1	5	
OUT PIN-VOLTAGE REGULATION							
$V_{O(OUT-REG)}$	Output regulation voltage	bq24070	$V_{I(AC)}$ ≥ 4.4 V + V_{DO}		4.4	4.5	V
		bq24071	$V_{I(AC)}$ ≥ 6 V + V_{DO}		6.0	6.3	
OUT PIN – DPPM REGULATION							
$V_{(DPPM-SET)}$	DPPM set point(2)		$V_{DPPM-SET} < V_{OUT}$	2.6		3.8	V
$I_{(DPPM-SET)}$	DPPM current source		Input present	95	100	105	μA
SF	DPPM scale factor		$V_{(DPPM-REG)} = V_{(DPPM-SET)} \times SF$	1.139	1.150	1.162	
OUT PIN – FET (Q1, Q2) DROP-OUT VOLTAGE $R_{DS(on)}$)							
$V_{(ACDO)}$	AC to OUT dropout voltage(3)		$V_{I(AC)}$ ≥ $V_{CC(min)}$, Mode = High, $I_{I(AC)}$ = 1 A, ($I_{O(OUT)}$+ $I_{O(BAT)}$), or no input		300	475	mV
$V_{(BATDO)}$	BAT to OUT dropout voltage (discharging)		$V_{I\ (BAT)}$ ≥ 3 V, $I_{I(BAT)}$= 1.0 A, $V_{CC} < V_{I(BAT)}$		40	100	
OUT PIN - BATTERY SUPPLEMENT MODE							
V_{BSUP1}	Enter battery supplement mode (battery supplements OUT current in the presence of input source		$V_{I(BAT)}$> 2 V	$V_{I(OUT)}$ ≤ $V_{I(BAT)}$ – 60 mV			V
V_{BSUP2}	Exit battery supplement mode		$V_{I(BAT)}$> 2 V			$V_{I(OUT)}$ ≥ $V_{I(BAT)}$ – 20 mV	
OUT PIN - SHORT CIRCUIT							
I_{OSH1}	BAT to OUT short-circuit recovery		Current source between BAT to OUT for short-circuit recovery to $V_{I(OUT)}$ ≤ $V_{I(BAT)}$ –200 mV		10		mA
R_{SHAC}	AC to OUT short-circuit limit		$V_{I(OUT)}$ ≤ 1 V		500		Ω
BAT PIN CHARGING – PRECHARGE							
$V_{(LOWV)}$	Precharge to fast-charge transition threshold		Voltage on BAT	2.9	3	3.1	V
$T_{DGL(F)}$	De-glitch time for fast-charge to precharge transition(4)		t_{FALL} = 100 ns, 10 mV overdrive, $V_{I(BAT)}$ decreasing below threshold		22.5		ms
$I_{O(PRECHG)}$	Precharge range		1 V < $V_{I(BAT)}$ < $V_{(LOWV)}$, t < $t_{(PRECHG)}$, $I_{O(PRECHG)}$ = ($K_{(SET)}$ × $V_{(PRECHG)}$)/ R_{SET}	10		150	mA
$V_{(PRECHG)}$	Precharge set voltage		1 V < $V_{I(BAT)}$ < $V_{(LOWV)}$, t < $t_{(PRECHG)}$	225	250	275	mV
BAT PIN CHARGING - CURRENT REGULATION							
$I_{O(BAT)}$	Battery charge current range (5)		$V_{I\ (BAT)}$ > $V_{(LOWV)}$, Mode = High $I_{OUT(BAT)}$ = ($K_{(SET)}$ × $V_{(SET)}$ / R_{SET}), V_I(OUT) > V_O(OUT-REG) + $V_{(DO-MAX)}$	100	1000	1500	mA
R_{PBAT}	BAT to OUT pullup		$V_{I\ (BAT)}$< 1 V		1000		Ω

(1) This includes the quiescent current for the integrated LDO.
(2) $V_{(DPPM-SET)}$ is scaled up by the scale factor for controlling the output voltage $V_{(DPPM-REG)}$.
(3) $V_{DO(max)}$, dropout voltage is a function of the FET, $R_{DS(on)}$, and drain current. The dropout voltage increases proportionally to the increase in current.
(4) All de-glitch periods are a function of the timer setting and is modified in DPPM or thermal regulation modes by the percentages that the program current is reduced.
(5) When input current remains below 2 A, the battery charging current may be raised until the thermal regulation limits the charge current.

ELECTRICAL CHARACTERISTICS (continued)

over junction temperature range (0°C ≤ T_J ≤ 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SET)}$	Battery charge current set voltage(6)	Voltage on ISET1, V_{VCC} ≥ 4.35 V, $V_{I(OUT)}$- $V_{I(BAT)}$ > $V_{(DO-MAX)}$, $V_{I(BAT)}$ > $V_{(LOWV)}$	2.47	2.50	2.53	V
$K_{(SET)}$	Charge current set factor, BAT	100 mA ≤ $I_{O(BAT)}$ ≤ 1.5 A	375	425	450	
		10 mA ≤ $I_{O(BAT)}$ ≤ 100 mA(7)	300	450	600	
USB MODE INPUT CURRENT LIMIT						
$I_{(USB)}$	USB input port current range	ISET2 = Low	80	90	100	mA
		ISET2 = High	400		500	
BAT PIN CHARGING VOLTAGE REGULATION, $V_{O\ (BAT-REG)}$ + $V_{(DO-MAX)}$ < V_{CC}, I_{TERM} < $I_{BAT(OUT)}$ ≤ 1 A						
$V_{O(BAT-REG)}$	Battery charge voltage			4.2		V
	Battery charge voltage regulation accuracy	T_A = 25°C	–0.5%		0.5%	
			–1%		1%	
CHARGE TERMINATION DETECTION						
$I_{(TERM)}$	Charge termination detection range	$V_{I(BAT)}$ > $V_{(RCH)}$, $I_{(TERM)}$ = ($K_{(SET)}$ × $V_{(TERM)}$)/ R_{SET}	10		150	mA
$V_{(TERM)}$	Charge termination set voltage, measured on ISET1	$V_{I(BAT)}$ > $V_{(RCH)}$, Mode = High	230	250	270	mV
		$V_{I(BAT)}$ > $V_{(RCH)}$, Mode = Low	95	100	130	
$T_{DGL(TERM)}$	De-glitch time for termination detection	t_{FALL} = 100 ns, 10 mV overdrive, I_{CHG} increasing above or decreasing below threshold		22.5		ms
TEMPERATURE SENSE COMPARATORS						
V_{LTF}	High voltage threshold	Temp fault at V(TS) > V_{LTF}	2.465	2.500	2.535	V
V_{HTF}	Low voltage threshold	Temp fault at V(TS) < V_{HTF}	0.485	0.500	0.515	V
I_{TS}	Temperature sense current source		94	100	106	µA
$T_{DGL(TF)}$	De-glitch time for temperature fault detection(8)	$R_{(TMR)}$ = 50 kΩ, $V_{I(BAT)}$ increasing or decreasing above and below; 100-ns fall time, 10-mv overdrive		22.5		ms
BATTERY RECHARGE THRESHOLD						
V_{RCH}	Recharge threshold voltage		$V_{O(BAT-REG)}$ –0.075	$V_{O(BAT-REG)}$ –0.100	$V_{O(BAT-REG)}$ –0.125	V
$T_{DGL(RCH)}$	De-glitch time for recharge detection(8)	$R_{(TMR)}$ = 50 kΩ, $V_{I(BAT)}$ increasing or decreasing below threshold, 100-ns fall time, 10-mv overdrive		22.5		ms
STAT1, STAT2, AND $\overline{PG}$, OPEN DRAIN (OD) OUTPUTS(9)						
V_{OL}	Low-level output saturation voltage	I_{OL} = 5 mA, An external pullup resistor ≥ 1 K required.			0.25	V
I_{LKG}	Input leakage current			1	5	µA
ISET2, CE INPUTS						
V_{IL}	Low-level input voltage		0		0.4	V
V_{IH}	High-level input voltage		1.4			
I_{IL}	Low-level input current, CE		–1			µA
I_{IH}	High-level input current, CE				1	
I_{IL}	Low-level input current, ISET2	V_{ISET2} = 0.4 V	–20			
I_{IH}	High-level input current, ISET2	V_{ISET2} = V_{CC}			40	
$t_{(CE-HLDOFF)}$	Holdoff time, CE	CE going low only	3.3		6.2	ms

(6) For half-charge rate, $V_{(SET)}$ is 1.25 V ± 25 mV.
(7) Specification is for monitoring charge current via the ISET1 pin during voltage regulation mode, not for a reduced fast-charge level.
(8) All de-glitch periods are a function of the timer setting and is modified in DPPM or thermal regulation modes by the percentages that the program current is reduced.
(9) See Charger Sleep mode for $\overline{PG}$ (V_{CC} = V_{IN}) specifications.

ELECTRICAL CHARACTERISTICS (continued)

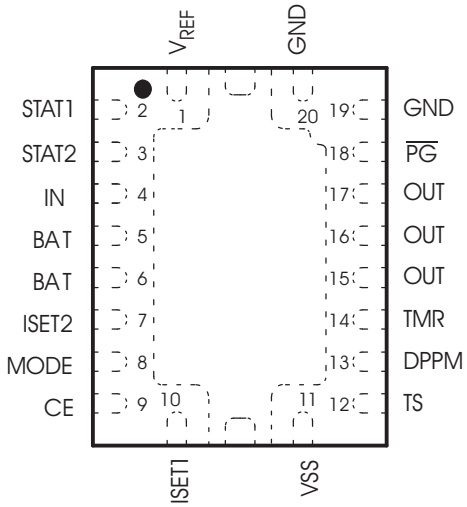
over junction temperature range (0°C ≤ T_J ≤ 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MODE INPUT						
V_{IL}	Low-level input voltage	Falling Hi→Low; 280 K ± 10% applied when low.	0.975	1	1.025	V
V_{IH}	High-level input voltage	Input R_{Mode} sets external hysteresis	V_{IL} + .01		V_{IL} + .024	V
I_{IL}	Low-level input current, Mode		–1			µA
TIMERS						
$K_{(TMR)}$	Timer set factor	$t_{(CHG)} = K_{(TMR)} \times R_{(TMR)}$	0.313	0.360	0.414	s/Ω
$R_{(TMR)}$ (10)	External resistor limits		30		100	kΩ
$t_{(PRECHG)}$	Precharge timer		0.09 × $t_{(CHG)}$	0.10 × $t_{(CHG)}$	0.11 × $t_{(CHG)}$	s
$I_{(FAULT)}$	Timer fault recovery pullup from OUT to BAT			1		kΩ
CHARGER SLEEP THRESHOLDS ($\overline{PG}$ THRESHOLDS, LOW → POWER GOOD)						
$V_{(SLPENT)}$ (11)	Sleep-mode entry threshold	$V_{(UVLO)} \le V_{I(BAT)} \le V_{O(BAT-REG)}$, No $t_{(BOOT-UP)}$ delay			$V_{VCC} \le V_{I(BAT)}$ +125 mV	V
$V_{(SLPEXIT)}$ (11)	Sleep-mode exit threshold	$V_{(UVLO)} \le V_{I(BAT)} \le V_{O(BAT-REG)}$, No $t_{(BOOT-UP)}$ delay	$V_{VCC} \ge V_{I(BAT)}$ +190 mV			
$t_{(DEGL)}$	De-glitch time for sleep mode (12)	$R_{(TMR)}$ = 50 kΩ, $V_{(IN)}$ decreasing below threshold, 100-ns fall time, 10-mv overdrive		22.5		ms
START-UP CONTROL BOOT-UP						
$t_{(BOOT-UP)}$	Boot-up time	On the first application of input with Mode Low	120	150	180	ms
SWITCHING POWER SOURCE TIMING						
t_{SW-BAT}	Switching power source from input to battery	When input applied. Measure from: [$\overline{PG}$: Lo → Hi to $I_{(IN)}$ > 5 mA], $I_{(OUT)}$ = 100 mA, R_{TRM} = 50 K			50	µs
THERMAL SHUTDOWN REGULATION (13)						
$T_{(SHTDWN)}$	Temperature trip	T_J (Q1 and Q3 only)		155		°C
	Thermal hysteresis	T_J (Q1 and Q3 only)		30		
$T_{J(REG)}$	Temperature regulation limit	T_J (Q2)	115		135	
UVLO						
$V_{(UVLO)}$	Undervoltage lockout	Decreasing V_{CC}	2.45	2.50	2.65	V
	Hysteresis			27		mV
V_{REF} OUTPUT						
$V_{O(VREF)}$	Output regulation voltage	Active only if AC or USB is present, $V_{I(OUT)} \ge V_{O(VREF)} + (I_{O(VREF)} \times R_{DS(on)})$		3.3		V
	Regulation accuracy (14)		–5%		5%	
$I_{O(VREF)}$	Output current				20	mA
$R_{DS(on)}$	On resistance	OUT to V_{REF}			50	Ω
$C_{(OUT)}$ (15)	Output capacitance				1	µF

(10) To disable the fast-charge safety timer and charge termination, tie TMR to the V_{REF} pin. Tying the TMR pin high changes the timing resistor from the external value to an internal 50 kΩ ±25%, which can add an additional tolerance to any timed specification. The TMR pin normally regulates to 2.5 V when the charge current is not restricted by the DPPM or thermal feedback loops. If these loops become active, the TMR pin voltage will be reduced proportionally to the reduction in charge current and the clock frequency will be reduced by the same percentage (timed durations will count down slower, extending their time). The TMR pin is clamped at 0.80 V, for a maximum time extension of 2.5 V ÷ 0.8 V × 100 = 310%.
(11) The IC is considered in sleep mode when IN is absent ($\overline{PG}$ = OPEN DRAIN).
(12) Does not declare sleep mode until after the de-glitch time and implement the needed power transfer immediately according to the switching specification.
(13) Reaching thermal regulation reduces the charging current. Battery supplement current is not restricted by either thermal regulation or shutdown. Input power FETs turn off during thermal shutdown. The battery FET is only protected by a short-circuit limit which typically does not cause a thermal shutdown (input FETs turning off) by itself.
(14) In standby mode (CE low) the accuracy is ±10%.
(15) V_{REF} output capacitor not required, but one with a value of 0.1 µF is recommended.

DEVICE INFORMATION

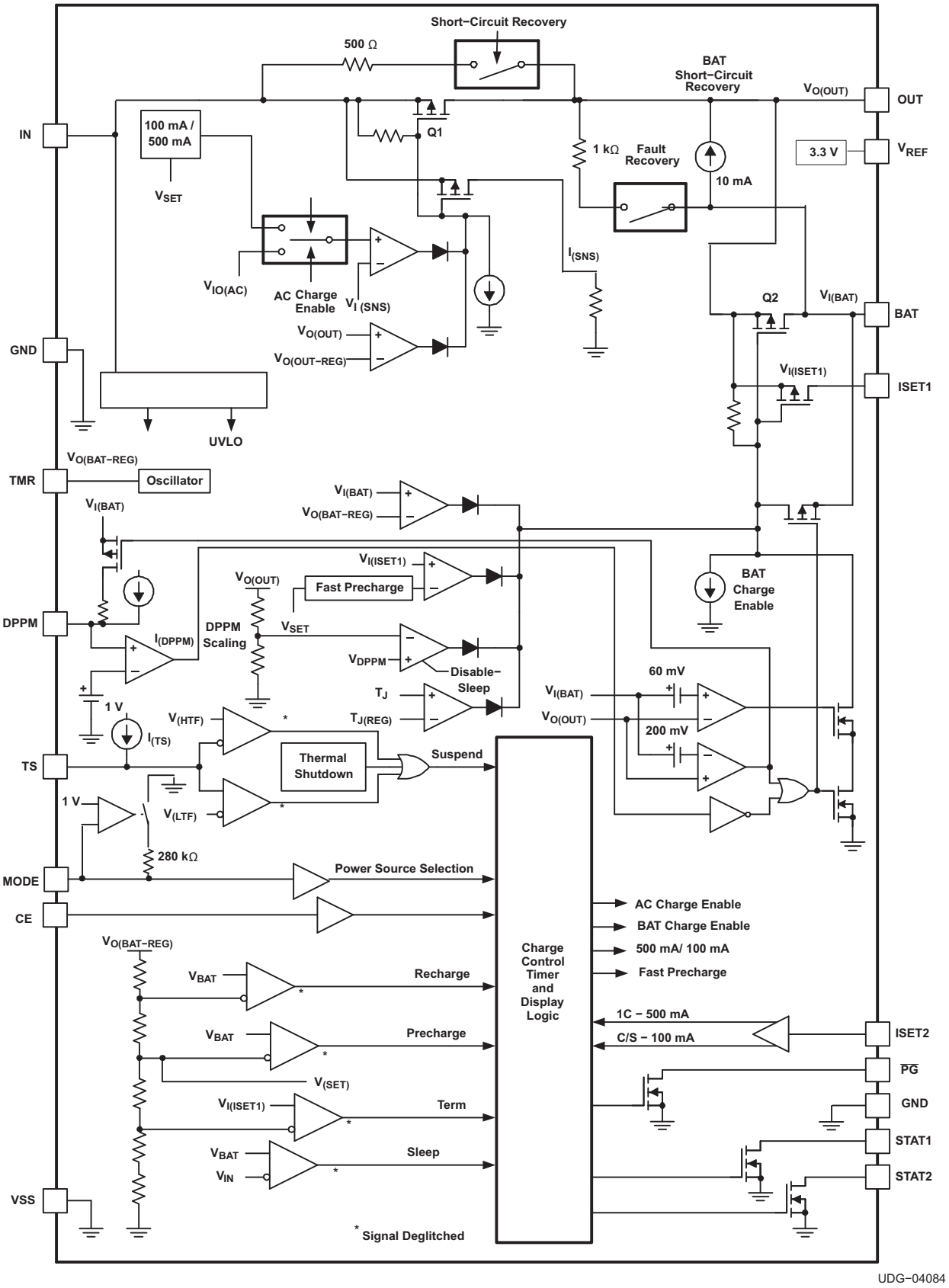
bq24070/1RHL
RHL PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
IN	4	I	Charge input voltage
$\overline{PG}$	18	O	Power-good status output (open-drain)
BAT	5, 6	I/O	Battery input and output.
CE	9	I	Chip enable input (active high)
DPPM	13	I	Dynamic power-path management set point (account for scale factor)
ISET1	10	I/O	Charge current set point and precharge and termination set point
ISET2	7	I	Charge current set point for USB port. (High = 500 mA, Low = 100 mA) See half-charge current mode using ISET2.
OUT	15, 16, 17	O	Output terminal to the system
MODE	8	I	Power source selection input (Low for USB mode current limit)
STAT1	2	O	Charge status output 1 (open-drain)
STAT2	3	O	Charge status output 2 (open-drain)
TMR	14	I/O	Timer program input programmed by resistor. Disable fast-charge safety timer and termination by tying TMR to V_{REF}.
TS	12	I/O	Temperature sense input
GND	19, 20	I	Ground input
VREF	1	O	Internal reference signal
VSS	11	–	Ground input (the thermal pad on the underside of the package) There is an internal electrical connection between the exposed thermal pad and VSS pin of the device. The exposed thermal pad must be connected to the same potential as the VSS pin on the printed-circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

FUNCTIONAL BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTIONS

SIGMA

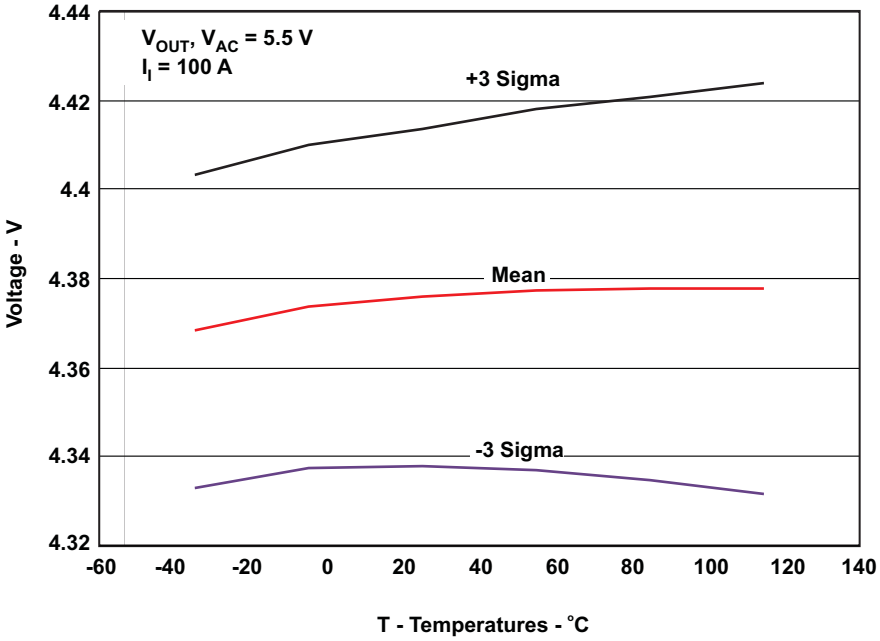


Figure 1. Typical OUT Voltage Regulation, bq24070

CHARGE CONTROL

The bq24070/1 supports a precision Li-ion or Li-polymer charging system suitable for single-cell portable devices. See a typical charge profile, application circuit, and an operational flow chart in Figure 2 through Figure 4, respectively.

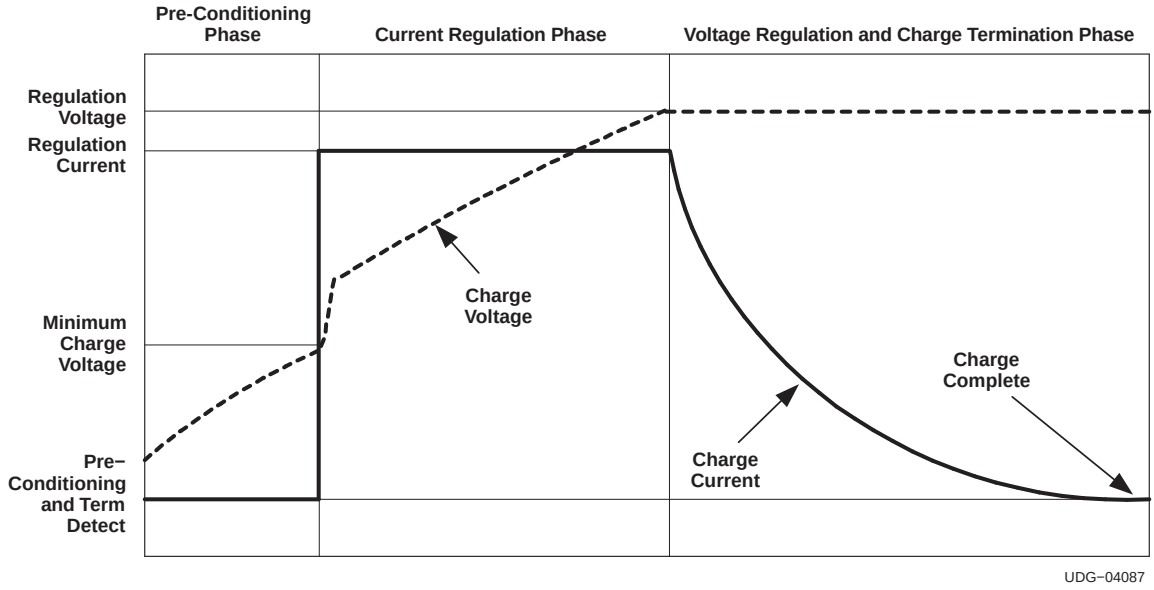


Figure 2. Charge Profile

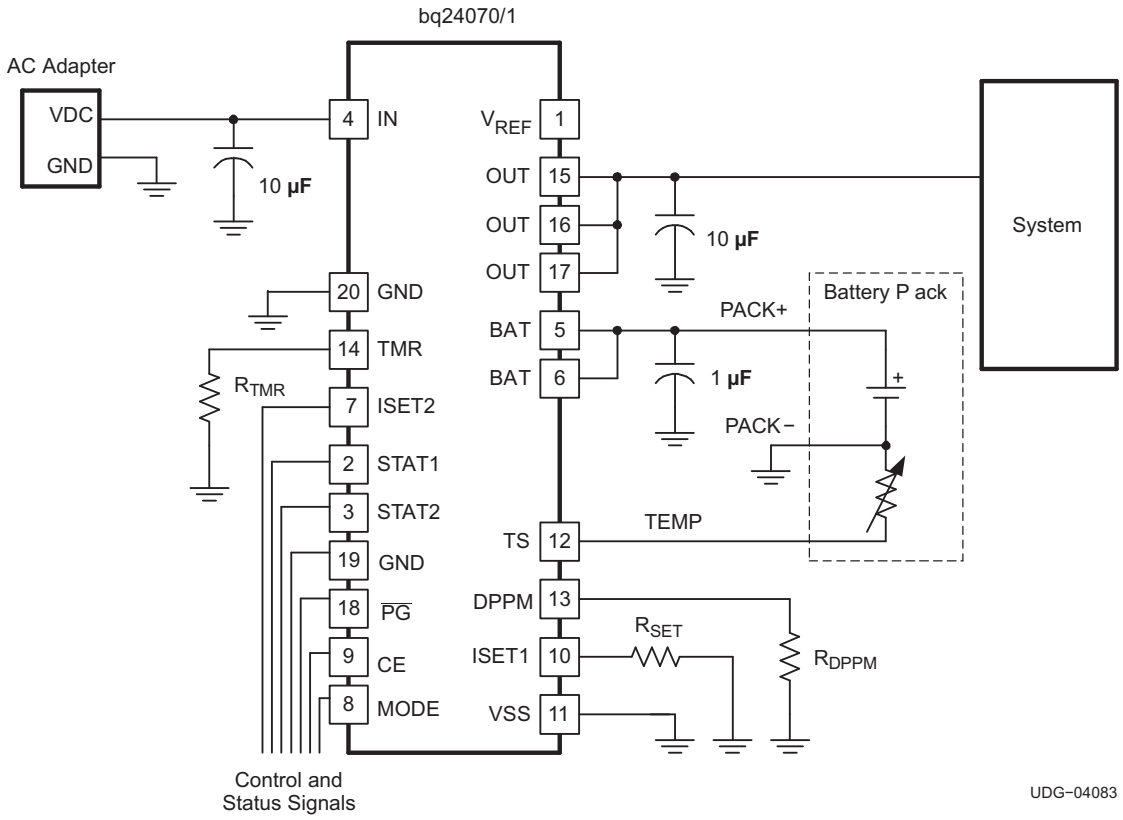


Figure 3. Typical Application Circuit

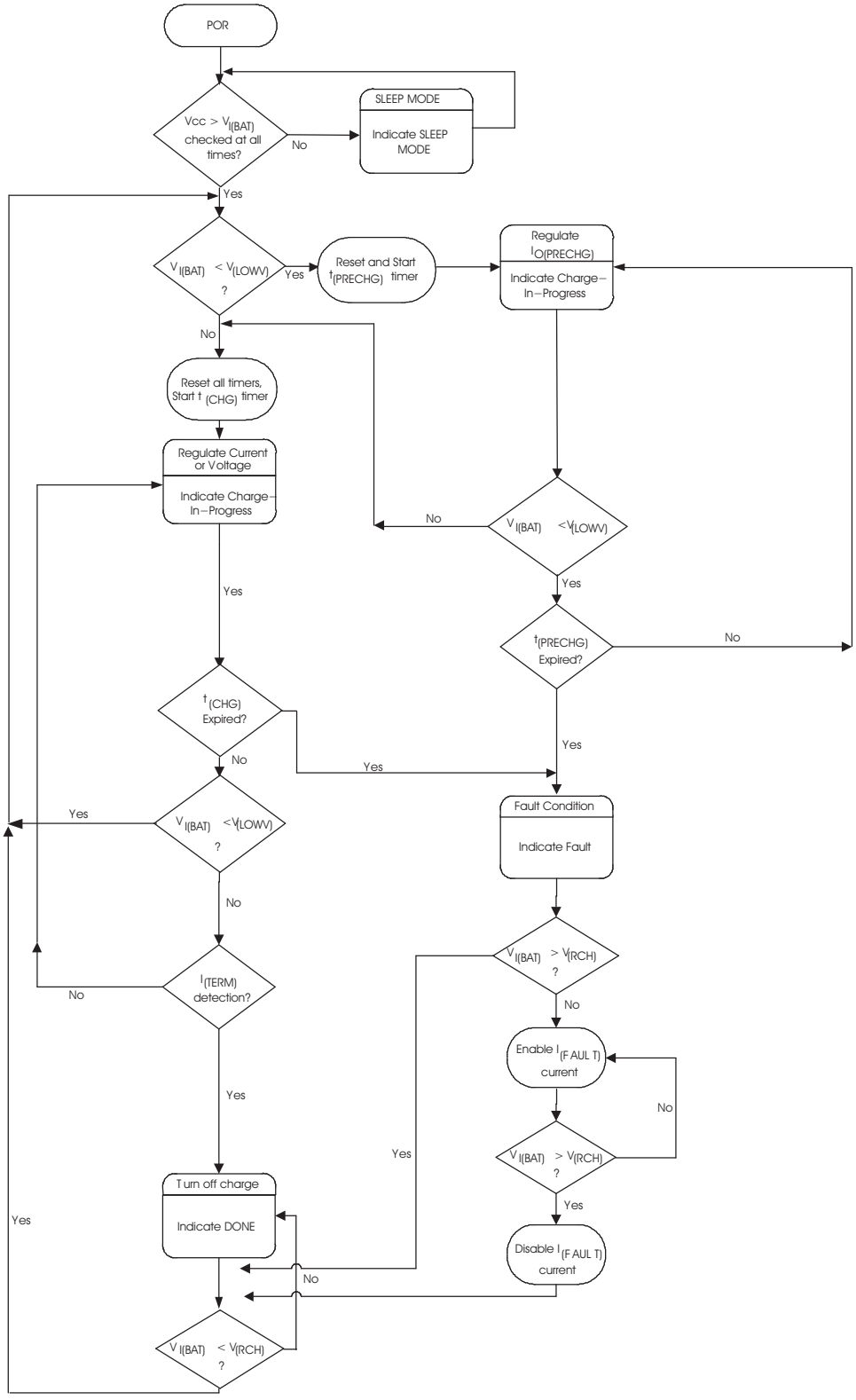


Figure 4. Charge Control Operational Flow Chart

Autonomous Power Source Selection, Mode Control Pin

With the MODE input low, the bq24070/1 defaults to USB-mode charging, and the supply current is limited by the ISET2 pin (100 mA for ISET2 = Low, 500 mA for ISET2 = High). If an input source is not available, then the battery is selected as the source.

Boot-Up Sequence

In order to facilitate the system start-up and USB enumeration, the bq24070/1 offers a proprietary boot-up sequence. On the first application of power to the bq24070/1, this feature enables the 100-mA USB charge rate for a period of approximately 150 ms, ($t_{(BOOT-UP)}$), ignoring the ISET2 and CE inputs setting. At the end of this period, the bq24070/1 implement CE and ISET2 input settings. Table 1 indicates when this feature is enabled. See Figure 9.

Power-Path Management

The bq24070/1 powers the system while independently charging the battery. This feature reduces the charge and discharge cycles on the battery, allows for proper charge termination, and allows the system to run with an absent or defective battery pack. This feature gives the system priority on input power, allowing the system to power up with a deeply discharged battery pack. This feature works as follows:

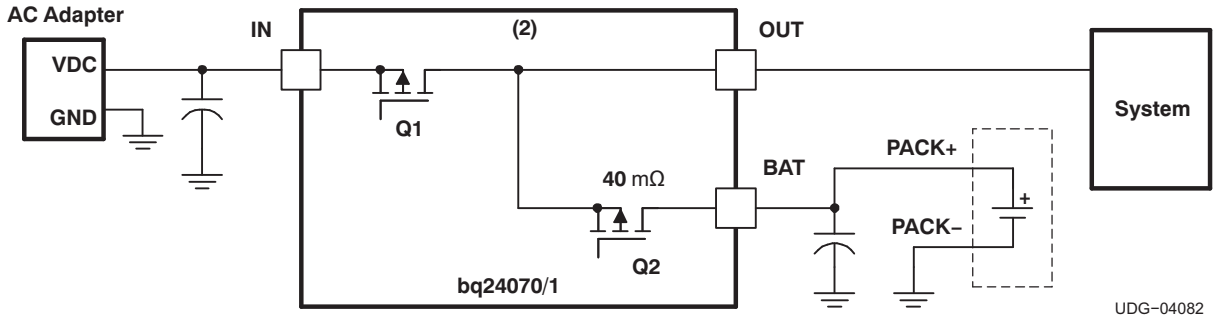


Figure 5. Power-Path Management

Case 1: AC Mode (Mode = High)

System Power

In this case, the system load is powered directly from the AC adapter through the internal transistor Q1 (see Figure 5). The output is regulated at 4.4 V (bq24070). If the system load exceeds the capacity of the supply, the output voltage drops down to the battery's voltage.

Charge Control

When in AC mode the battery is charged through switch Q2 based on the charge rate set on the ISET1 input.

Dynamic Power-Path Management (DPPM)

This feature monitors the output voltage (system voltage) for input power loss due to brown outs, current limiting, or removal of the input supply. If the voltage on the OUT pin drops to a preset value, $V_{(DPPM)}$ × SF, due to a limited amount of input current, then the battery charging current is reduced until the output voltage stops dropping. The DPPM control tries to reach a steady-state condition where the system gets its needed current and the battery is charged with the remaining current. No active control limits the current to the system; therefore, if the system demands more current than the input can provide, the output voltage drops just below the battery voltage and Q2 turns on which supplements the input current to the system. DPPM has three main advantages.

1. This feature allows the designer to select a lower power wall adapter, if the average system load is moderate compared to its peak power. For example, if the peak system load is 1.75 A, average system load is 0.5 A and battery fast-charge current is 1.25 A, the total peak demand could be 3 A. With DPPM, a 2-A adaptor could be selected instead of a 3.25-A supply. During the system peak load of 1.75 A and charge load of 1.25 A, the smaller adaptor's voltage drops until the output voltage reaches the DPPM regulation voltage threshold. The charge current is reduced until there is no further drop on the output voltage. The system gets

its 1.75-A charge and the battery charge current is reduced from 1.25 A to 0.25 A. When the peak system load drops to 0.5 A, the charge current returns to 1 A and the output voltage returns to its normal value.

2. Using DPPM provides a power savings compared to configurations without DPPM. Without DPPM, if the system current plus charge current exceed the supply's current limit, then the output is pulled down to the battery. Linear chargers dissipate the unused power $(V_{IN}\text{-}V_{OUT}) \times I_{LOAD}$. The current remains high (at current limit) and the voltage drop is large for maximum power dissipation. With DPPM, the voltage drop is less $(V_{IN}\text{-}V_{(DPPM\text{-}REG)})$ to the system which means better efficiency. The efficiency for charging the battery is the same for both cases. The advantages include less power dissipation, lower system temperature, and better overall efficiency.
3. The DPPM sustains the system voltage no matter what causes it to drop, if at all possible. It does this by reducing the noncritical charging load while maintaining the maximum power output of the adaptor.

Note that the DPPM voltage, $V_{(DPPM)}$, is programmed as follows:

$$V_{(DPPM-REG)} = I_{(DPPM)} \times R_{(DPPM)} \times SF \quad (1)$$

where

$R_{(DPPM)}$ is the external resistor connected between the DPPM and VSS pins.

$I_{(DPPM)}$ is the internal current source.

SF is the scale factor as specified in the specification table.

The safety timer is dynamically adjusted while in DPPM mode. The voltage on the ISET1 pin is directly proportional to the programmed charging current. When the programmed charging current is reduced, due to DPPM, the ISET1 and TMR voltages are reduced and the timer's clock is proportionally slowed, extending the safety time. In normal operation V(TMR) = 2.5 V; and, when the clock is slowed, V(TMR) is reduced. When V(TMR) = 1.25 V, the safety timer has a value close to 2 times the normal operation timer value. See Figure 6 through Figure 7.

Case 2: USB Mode (Mode = L)

System Power

In this case, the system load is powered from a USB port through the internal switch Q1 (see Figure 5). Note that in this case, Q1 regulates the total current to the 100-mA or 500-mA level, as selected on the ISET2 input. The output, V_{OUT}, is regulated to 4.4 V (bq24070). The system's power management is responsible for keeping its system load below the USB current level selected (if the battery is critically low or missing). Otherwise, the output drops to the battery voltage; therefore, the system should have a low-power mode for USB power application. The DPPM feature keeps the output from dropping below its programmed threshold, due to the battery charging current, by reducing the charging current.

Charge Control

When in USB mode, Q1 regulates the input current to the value selected by the ISET2 pin (0.1/0.5 A). The charge current to the battery is set by the ISET1 resistor (typically > 0.5 A). Because the charge current typically is programmed for more current than the USB current limit allows, the output voltage drops to the battery voltage or DPPM voltage, whichever is higher. If the DPPM threshold is reached first, the charge current is reduced until V_{OUT} stops dropping. If V_{OUT} drops to the battery voltage, the battery is able to supplement the input current to the system.

Dynamic Power-Path Management (DPPM)

The theory of operation is the same as described in CASE 1, except that Q1 is restricted to the USB current level selected by the ISET2 pin.

Note that the DPPM voltage, $V_{(DPPM)}$, is programmed as follows:

$$V_{(DPPM-REG)} = I_{(DPPM)} \times R_{(DPPM)} \times SF \quad (2)$$

where

$R_{(DPPM)}$ is the external resistor connected between the DPPM and VSS pins.

$I_{(DPPM)}$ is the internal current source.

SF is the scale factor as specified in the specification table.

Feature Plots

Figure 6 illustrates DPPM and battery supplement modes as the output current (I_{OUT}) is increased; channel 1 (CH1) VAC = 5.4 V; channel 2 (CH2) V_{OUT}; channel 3 (CH3) I_{OUT} = 0 to 2.2 A to 0 A; channel 4 (CH4) V_{BAT} = 3.5 V; $I_{(PGM-CHG)}$ = 1 A. In typical operation, bq24070/1 (V_{OUT} = 4.4 V_{reg}), through an AC adaptor overload condition and recovery. The AC input is set for ~5.1 V (1.5 A current limit), $I_{(CHG)}$ = 1 A, $V_{(DPPM-SET)}$ = 3.7 V, $V_{(DPPM-OUT)}$ = 1.15 × $V_{(DPPM-SET)}$ = 4.26 V, V_{BAT} = 3.5 V, Mode = H, and USB input is not connected. The output load is increased from 0 A to ~2.2 A and back to 0 A as shown in the bottom waveform. As the I_{OUT} load reaches 0.5 A, along with the 1-A charge current, the adaptor starts to current limit, the output voltage drops to the DPPM-OUT threshold of 4.26 V. This is DPPM mode. The AC input tracks the output voltage by the dropout voltage of the AC FET. The battery charge current is then adjusted back as necessary to keep the output voltage from falling any further. Once the output load current exceeds the input current, the battery has to supplement the excess current and the output voltage falls just below the battery voltage by the dropout voltage of the battery FET. This is the battery supplement mode. When the output load current is reduced, the operation described is reversed as shown. If the DPPM-OUT voltage was set below the battery voltage, during input current limiting, the output falls directly to the battery's voltage.

Under USB operation, when the loads exceeds the programmed input current thresholds a similar pattern is observed. If the output load exceeds the available USB current, the output instantly goes into the battery supplement mode.

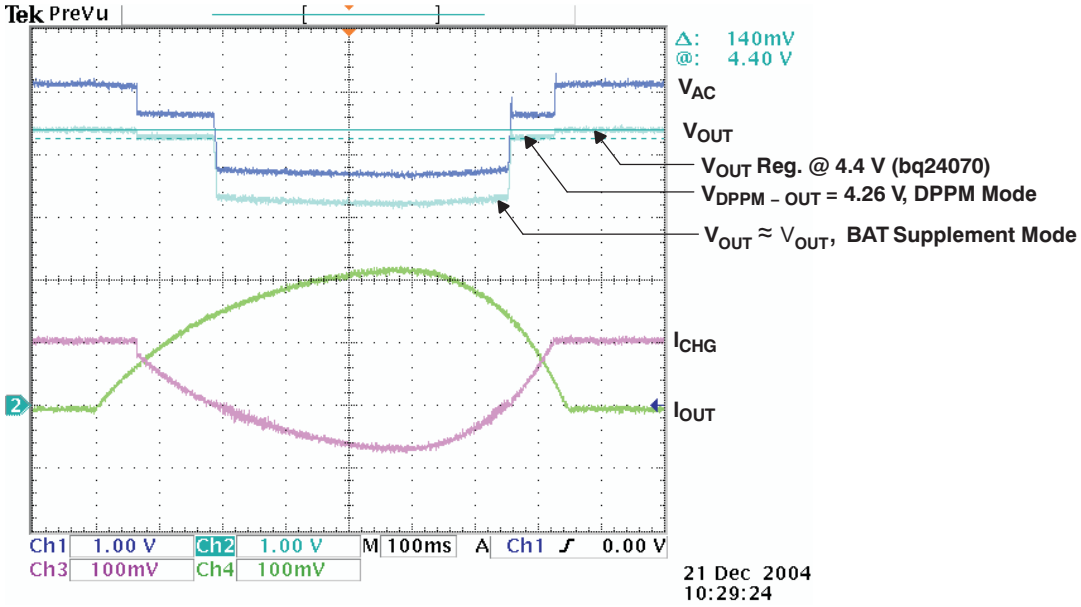


Figure 6. DPPM and Battery Supplement Modes

Figure 7 illustrates when Mode is toggled low for 500 µs. Power transfers from AC to USB to AC; channel 1 (CH1) VAC = 5.4 V; channel 2 (CH2) $V_{(USB)}$ = 5 V; channel 3 (CH3) V_{OUT}; output current, I_{OUT} = 0.25 A; channel 4 (CH4) V_{BAT} = 3.5 V; and $I_{(PGM-CHG)}$ = 1 A. When the Mode went low (1st div), the AC FET opened, and the output fell until the USB FET turned on. Turning off the active source before turning on the replacement source is referred to as *break-before-make* switching. The rate of discharge on the output is a function of system capacitance and load. Note the cable IR drop in the AC and USB inputs when they are under load. At the 4th division, the output has reached steady-state operation at the DPPM voltage level (charge current has been reduced due to the limited USB input current). At the 6th division, the Mode goes high and the USB FET turns off followed by the AC FET turning on. The output returns to its regulated value, and the battery returns to its programmed current level.

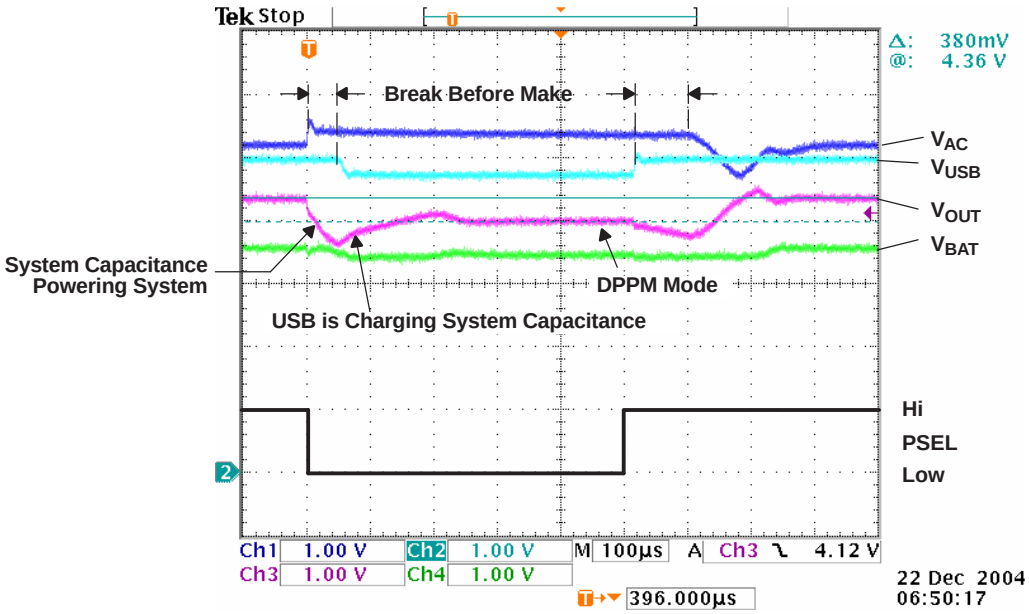


Figure 7. Toggle Mode Low

Figure 8 illustrates when a battery is inserted for power up; channel 1 (CH1) VAC = 0 V; channel 2 (CH2) V_{USB} = 0 V; channel 3 (CH3) V_{OUT}; output current, I_{OUT} = 0.25 A for V_{OUT} > 2 V; channel 4 (CH4) V_{BAT} = 3.5 V; $C_{(DPPM)}$ = 0 pF. When there are no power sources and the battery is inserted, the output tracks the battery voltage if there is no load (<10 mA of load) on the output, as shown. If a load is present that keeps the output more than 200 mV below the battery, a short-circuit condition is declared. At this time, the load has to be removed to recover. A capacitor can be placed on the DPPM pin to delay implementing the short-circuit mode and get unrestricted (not limited) current.

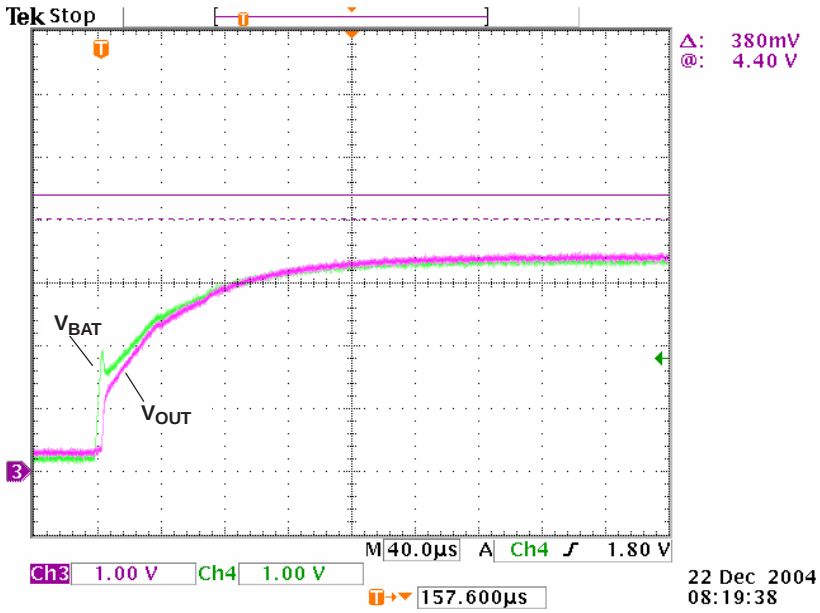


Figure 8. Insert Battery – Power-Up Output via BAT

Figure 9 illustrates USB boot up and power-up via USB; channel 1 (CH1) $V_{(USH)}$ = 0 to 5 V; channel 2 (CH2) USB

input current (0.2 A/div); Mode = Low; CE = High; ISET2 = High; V_{BAT} = 3.85 V; $V_{(DPPM)}$ = 3.0 V ($V_{(DPPM)}$ × 1.15 < V_{BAT}, otherwise DPPM mode increases time duration). When a USB source is applied (if AC is not present), the CE pin and ISET2 pin are ignored during the boot-up time and a maximum input current of 100 mA is made available to the OUT or BAT pins. After the boot-up time, the IC implements the CE and ISET2 pins as programmed.

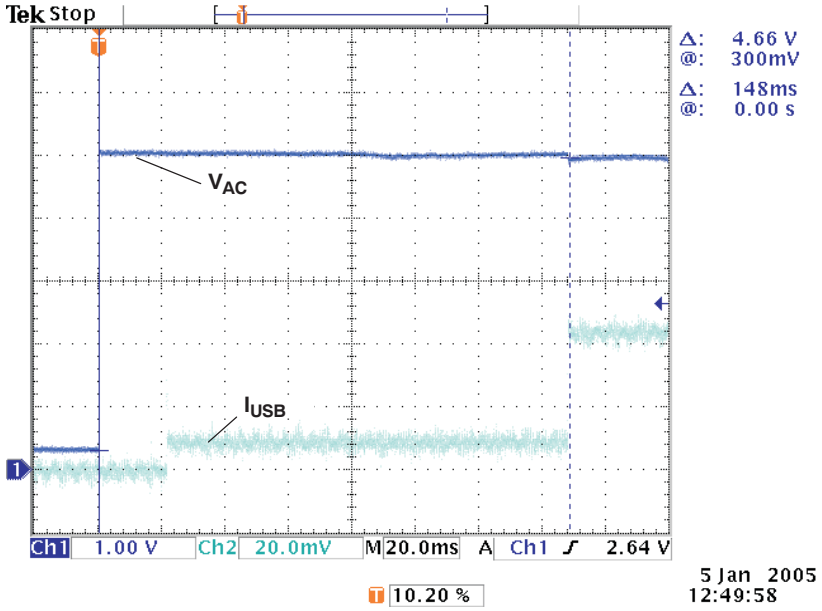


Figure 9. USB Boot-Up Power-Up

Battery Temperature Monitoring

The bq24070/1 continuously monitors battery temperature by measuring the voltage between the TS and VSS pins. An internal current source provides the bias for most-common 10 kΩ negative-temperature coefficient thermistors (NTC) (see Figure 10). The device compares the voltage on the TS pin against the internal $V_{(LTF)}$ and $V_{(HTF)}$ thresholds to determine if charging is allowed. Once a temperature outside the $V_{(LTF)}$ and $V_{(HTF)}$ thresholds is detected, the device immediately suspends the charge. The device suspends charge by turning off the power FET and holding the timer value (i.e., timers are not reset). Charge is resumed when the temperature returns to the normal range. The allowed temperature range for 103AT-type thermistor is 0°C to 45°C. However, the user may increase the range by adding two external resistors. See Figure 11.

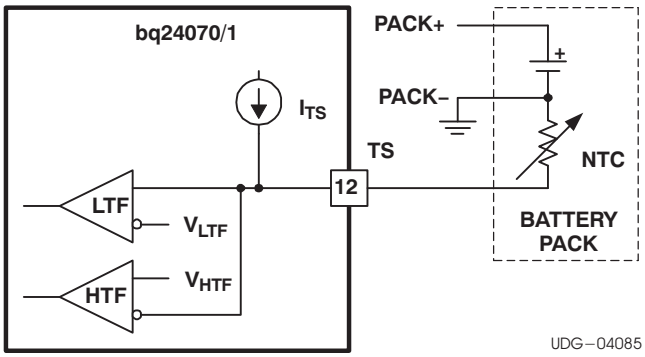


Figure 10. TS Pin Configuration

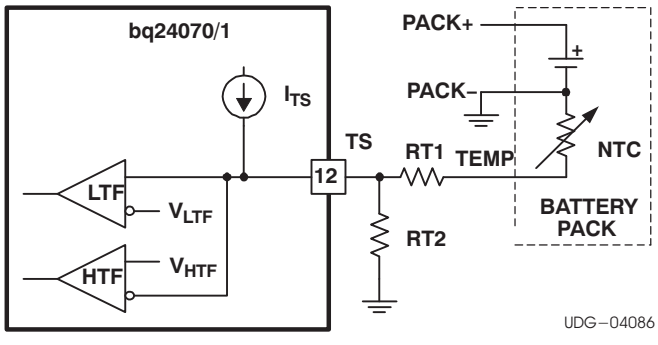


Figure 11. TS Pin Thresholds

Battery Pre-Conditioning

During a charge cycle, if the battery voltage is below the $V_{(LOWV)}$ threshold, the bq24070/1 applies a precharge current, $I_{O(PRECHG)}$, to the battery. This feature revives deeply discharged cells. The R_{SET} resistor, connected between the ISET1 and VSS pins, determines the precharge rate. The $V_{(PRECHG)}$ and $K_{(SET)}$ parameters are specified in the specifications table. Note that this applies to both AC-mode and USB-mode charging.

$$I_{O\ (PRECHG)} = \frac{V_{(PRECHG)} \times K_{(SET)}}{R_{SET}} \quad (3)$$

The bq24070/1 activates a safety timer, $t_{(PRECHG)}$, during the conditioning phase. If $V_{(LOWV)}$ threshold is not reached within the timer period, the bq24070/1 turns off the charger and enunciates FAULT on the STAT1 and STAT2 pins. The timeout is extended if the charge current is reduced by DPPM or thermal regulation. See the *Timer Fault Recovery* section for additional details.

Battery Charge Current

The bq24070/1 offers on-chip current regulation with programmable set point. The R_{SET} resistor, connected between the ISET1 and VSS pins, determines the charge level. The charge level may be reduced to give the system priority on input current (see DPPM). The $V_{(SET)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{O\ (OUT)} = \frac{V_{(SET)} \times K_{(SET)}}{R_{SET}} \quad (4)$$

When powered from a USB port, the input current available (0.1 A/0.5 A) is typically less than the programmed (ISET1) charging current, and therefore, the DPPM feature attempts to keep the output from being pulled down by reducing the charging current.

The charge level, during AC mode operation only (Mode = High), can be changed by a factor of 2 by setting the ISET2 pin high (full charge) or low (half charge). The voltage on the ISET1 pin, VSET1, is divided by 2 when in the half constant current charge mode. Note that with Mode low, the ISET2 pin controls only the 0.1 A/0.5 A USB current level.

See the section titled *Power-Path Management* for additional details.

Battery Voltage Regulation

The voltage regulation feedback is through the BAT pin. This input is tied directly to the positive side of the battery pack. The bq24070/1 monitors the battery-pack voltage between the BAT and VSS pins. When the battery voltage rises to the $V_{O(REG)}$ threshold, the voltage regulation phase begins and the charging current begins to taper down.

If the battery is absent, the BAT pin cycles between charge done ($V_{O(REG)}$) and charging (battery recharge threshold, ~4.1 V).

See Figure 8 for power up by battery insertion.

As a safety backup, the bq24070/1 also monitors the charge time in the charge mode. If charge is not terminated within this time period, $t_{(CHG)}$, the bq24070/1 turns off the charger and enunciates FAULT on the STAT1 and STAT2 pins. See the DPPM operation under Case 1 for information on extending the safety timer during DPPM operation. See the*Timer Fault Recovery* section for additional details.

Temperature Regulation and Thermal Protection

In order to maximize charge rate, the bq24070/1 features a junction temperature regulation loop. If the power dissipation of the IC results in a junction temperature greater than the $T_{J(REG)}$ threshold, the bq24070/1 throttles back on the charge current in order to maintain a junction temperature around the $T_{J(REG)}$ threshold. To avoid false termination, the termination detect function is disabled while in this mode.

The bq24070/1 also monitors the junction temperature, T_J, of the die and disconnects the OUT pin from the IN input if T_J exceeds $T_{(SHTDWN)}$. This operation continues until T_J falls below $T_{(SHTDWN)}$ by the hysteresis level specified in the specification table.

The battery supplement mode has no thermal protection. The Q2 FET continues to connect the battery to the output (system), if input power is not sufficient; however, a short-circuit protection circuit limits the battery discharge current such that the maximum power dissipation of the part is not exceeded under typical design conditions.

Charge Timer Operation

As a safety backup, the bq24070/1 monitors the charge time in the charge mode. If the termination threshold is not detected within the time period, $t_{(CHG)}$, the bq24070/1 turns off the charger and enunciates FAULT on the STAT1 and STAT2 pins. The resistor connected between the TMR and VSS, R_{TMR}, determines the timer period. The $K_{(TMR)}$ parameter is specified in the specifications table. In order to disable the charge timer, eliminate R_{TMR}, connect the TMR pin directly to the V_{REF} pin. Note that this action eliminates the fast-charge safety timer (it does not disable or reset the pre-charge safety timer), and also clears any timer fault. TMR pin should not be left floating.

$$t_{(CHG)} = K_{(TMR)} \times R_{(TMR)} \quad (5)$$

While in the thermal regulation mode or DPPM mode, the bq24070/1 dynamically adjusts the timer period in order to provide the additional time needed to fully charge the battery. This proprietary feature is designed to prevent against early or false termination. The maximum charge time in this mode, $t_{(CHG-TREG)}$, is calculated by Equation 6.

$$t_{(CHG-TREG)} = \frac{t_{(CHG)} \times V_{(SET)}}{V_{(SET-REG)}} \quad (6)$$

Note that because this adjustment is dynamic and changes as the ambient temperature changes and the charge level changes, the timer clock is adjusted. It is difficult to estimate a total safety time without integrating the above equation over the charge cycle. Therefore, understanding the theory that the safety time is adjusted inversely proportionately with the charge current and the battery is a current-hour rating, the safety time dynamically adjusts appropriately.

The $V_{(SET)}$ parameter is specified in the specifications table. $V_{(SET-TREG)}$ is the voltage on the ISET pin during the thermal regulation or DPPM mode and is a function of charge current. (Note that charge current is dynamically adjusted during the thermal regulation or DPPM mode.)

$$V_{(SET-TREG)} = \frac{I_{(OUT)} \times R_{(SET)}}{K_{(SET)}} \quad (7)$$

All de-glitch times also adjusted proportionally to $t_{(CHG-TREG)}$.

Charge Termination and Recharge

The bq24070/1 monitors the voltage on the ISET1 pin, during voltage regulation, to determine when termination should occur. Termination occurs when the charge current tapers down to either $1/10^{th}$ of the programmed fast charge rate (when the MODE pin is high) or $1/25^{th}$ of the programmed fast charge rate (when the MODE pin is low). Once the termination threshold, $I_{(TERM)}$, is detected the bq24070/1 terminates charge. The R_{SET} resistor, connected between the ISET1 and VSS pins, programs the fast charge current level and thus the current termination threshold level. The $V_{(TERM)}$ and $K_{(SET)}$ parameters are specified in the specifications table. Note that this applies to both AC and USB charging.

$$I_{(TERM)} = \frac{V_{(TERM)} \times K_{(SET)}}{R_{SET}} \quad (8)$$

After charge termination, the bq24070/1 re-starts the charge once the voltage on the BAT pin falls below the $V_{(RCH)}$ threshold. This feature keeps the battery at full capacity at all times.

Sleep and Standby Modes

The bq24070/1 charger circuitry enters the low-power sleep mode if the input is removed from the circuit. This feature prevents draining the battery into the bq24070/1 during the absence of input supply. Note that in sleep mode, Q2 remains on (i.e., battery connected to the OUT pin) in order for the battery to continue supplying power to the system.

The bq24070/1 enters the low-power standby mode if while input power is present, the CE input is low. In this suspend mode, internal power FET Q1 (see Figure 5) is turned off, the BAT input is used to power the system through the OUT pin. This feature is designed to limit the power drawn from the input supply (such as USB suspend mode).

Charge Status Outputs

The open-drain (OD) STAT1 and STAT2 outputs indicate various charger operations as shown in Table 2. These status pins can be used to drive LEDs or communicate to the host processor. Note that OFF indicates the open-drain transistor is turned off. Note that this assumes CE = High.

Table 2. Status Pins Summary

CHARGE STATE	STAT1	STAT2
Precharge in progress	ON	ON
Fast charge in progress	ON	OFF
Charge done	OFF	ON
Charge suspend (temperature), timer fault, and sleep mode	OFF	OFF

$\overline{PG}$, Outputs (Power Good)

The open-drain pin, $\overline{PG}$, indicates when input power is present, and above the battery voltage. The corresponding output turns ON (low) when exiting sleep mode (input voltage above battery voltage). This output is turned off in the sleep mode (open drain). The $\overline{PG}$ pin can be used to drive an LED or communicate to the host processor. Note that OFF indicates the open-drain transistor is turned off.

CE Input (Chip Enable)

The CE (chip enable) digital input is used to disable or enable the IC. A high-level signal on this pin enables the chip, and a low-level signal disables the device and initiates the standby mode. The bq24070/1 enters the low-power standby mode when the CE input is low with input present. In this suspend mode, internal power FET Q1 (see block diagram) is turned off; the battery (BAT pin) is used to power the system via Q2 and the OUT pin. This feature is designed to limit the power drawn from the input supply (such as USB suspend mode).

Charge Disable Functions

The DPPM input can be used to disable the charge process. This can be accomplished by floating the DPPM pin.

Timer Fault Recovery

As shown in Figure 4, bq24070/1 provides a recovery method to deal with timer fault conditions. The following summarizes this method:

Condition 1: Charge voltage above recharge threshold ($V_{(RCH)}$) and timeout fault occurs.

Recovery Method: bq24070/1 waits for the battery voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge, or battery removal. Once the battery falls below the recharge threshold, the bq24070/1 clears the fault and starts a new charge cycle. A POR or CE toggle also clears the fault.

Condition 2: Charge voltage below recharge threshold ($V_{(RCH)}$) and timeout fault occurs.

Recovery Method: Under this scenario, the bq24070/1 applies the $I_{(FAULT)}$ current. This small current is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, then the bq24070/1 disables the $I_{(FAULT)}$ current and executes the recovery method described for condition 1. Once the battery falls below the recharge threshold, the bq24070/1 clears the fault and starts a new charge cycle. A POR or CE toggle also clears the fault.

Short-Circuit Recovery

The output can experience two types of short-circuit protection, one associated with the input and one with the battery.

If the output drops below ~1 V, an input short-circuit condition is declared and the input FET, Q1 is turned off. To recover from this state, a 500-Ω pullup resistor from the input is applied (switched) to the output. To recover, the load on the output has to be reduced {R_{load} > 1 V × 500 Ω/ (V_{in}–V_{out})} such that the pullup resistor is able to lift the output voltage above 1 V, for the input FET to be turned back on.

If the output drops 200 mV below the battery voltage, the battery FET, Q2 is considered in short circuit and the battery FET turns off. To recover from this state, there is a 10-mA current source from the battery to the output. Once the output load is reduced, such that the 10-mA current source can pick up the output within 200 mV of the battery, the FET turns back on.

If the *short* is removed, and the minimum system load is still too large [R<(VBat-200 mV) / 10 mA], the short-circuit protection can be temporarily defeated. The battery short-circuit protection can be disabled (recommended only for a short time) if the voltage on the DPPM pin is less than 1 V. Pulsing this pin below 1 V, for a few microseconds, should be enough to recover.

This short-circuit disable feature was implemented mainly for power up when inserting a battery. Because the BAT input voltage rises much faster than the OUT voltage (V_{out}<V_{bat}-200 mV), with most any capacitive load on the output, the part can get stuck in short-circuit mode. Placing a capacitor between the DPPM pin and ground slows the V_{DPPM} rise time, during power up, and delays the short-circuit protection. Too large a capacitance on this pin (too much of a delay) could allow too-high currents if the output was shorted to ground. The recommended capacitance is 1 nF to 10 nF. The V_{DPPM} rise time is a function of the 100-µA DPPM current source, the DPPM resistor, and the capacitor added.

V_{REF}

The V_{REF} is used for internal reference and compensation (3.3 V typ). Additionally, it can be used to disable the safety timer and termination by connecting the TMR to the V_{REF} pin. For internal compensation, the V_{REF} pin requires a minimum 0.1 µF ceramic capacitor. The V_{REF} capacitor should not exceed 1 µF.

APPLICATION INFORMATION

Selecting the Input and Output Capacitors

In most applications, all that is needed is a high-frequency decoupling capacitor on the input. A 0.1-µF ceramic capacitor, placed in close proximity to IN to VSS pins, works well. In some applications depending on the power supply characteristics and cable length, it may be necessary to add an additional 10-µF ceramic capacitor to the input.

The bq24070/1 only requires a small output capacitor for loop stability. A 0.1-µF ceramic capacitor placed between the OUT and VSS pin is typically sufficient.

It is recommended to install a minimum of 33-µF capacitor between the BAT pin and VSS (in parallel with the battery). This ensures proper hot plug power up with a no-load condition (no system load or battery attached).

Thermal Considerations

The bq24070/1 is packaged in a thermally enhanced MLP package. The package includes a QFN thermal pad to provide an effective thermal contact between the device and the printed-circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled *QFN/SON PCB Attachment* (SLUA271). The power pad should be tied to the VSS plane. The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient).

The mathematical expression for θ_{JA} is:

$$\theta_{JA} = \frac{T_J - T_A}{P} \tag{9}$$

where

T_J = chip junction temperature
T_A = ambient temperature
P = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- whether or not the device is board mounted
- trace size, composition, thickness, and geometry
- orientation of the device (horizontal or vertical)
- volume of the ambient air surrounding the device under test and airflow
- whether other surfaces are in close proximity to the device being tested

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal power FET. It can be calculated from Equation 10:

$$P = \left[\left(V_{IN} - V_{OUT}\right) \times \left(I_{OUT} + I_{BAT}\right)\right] + \left[\left(V_{OUT} - V_{BAT}\right) \times \left(I_{BAT}\right)\right] \tag{10}$$

Due to the charge profile of Li-xx batteries, the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. See Figure 2. Typically the Li-ion battery's voltage quickly (< 2 V minutes) ramps to approximately 3.5 V, when entering fast charge (1-C charge rate and battery above 3 V). Therefore, it is customary to perform the steady-state thermal design using 3.5 V as the minimum battery voltage because the system board and charging device does not have time to reach a maximum temperature due to the thermal mass of the assembly during the early stages of fast charge. This theory is easily verified by performing a charge cycle on a discharged battery while monitoring the battery voltage and chargers power pad temperature.

PCB Layout Considerations

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the decoupling capacitor from the input terminal to VSS and the output filter capacitor from OUT to VSS should be placed as close as possible to the bq24070/1, with short trace runs to both signal and VSS pins.
- All low-current VSS connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high-current charge paths into IN and from the BAT and OUT pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The bq24070/1 is packaged in a thermally enhanced MLP package. The package includes a QFN thermal pad to provide an effective thermal contact between the device and the printed-circuit board. Full PCB design guidelines for this package are provided in the application note entitled *QFN/SON PCB Attachment* (SLUA271).

Changes from Revision E (October 2009) to Revision F **Page**

- Changed *Charge Termination and Recharge* description 18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
BQ24070RHLR	ACTIVE	QFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24070RHLRG4	ACTIVE	QFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24070RHLT	ACTIVE	QFN	RHL	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24070RHLTG4	ACTIVE	QFN	RHL	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24071RHLR	ACTIVE	QFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24071RHLRG4	ACTIVE	QFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24071RHLT	ACTIVE	QFN	RHL	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24071RHLTG4	ACTIVE	QFN	RHL	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

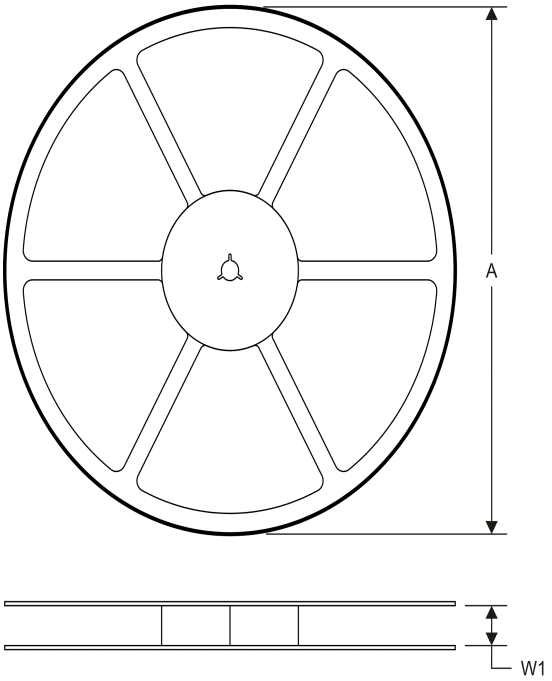
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

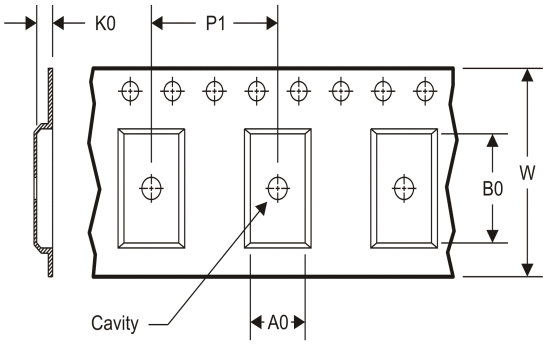
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



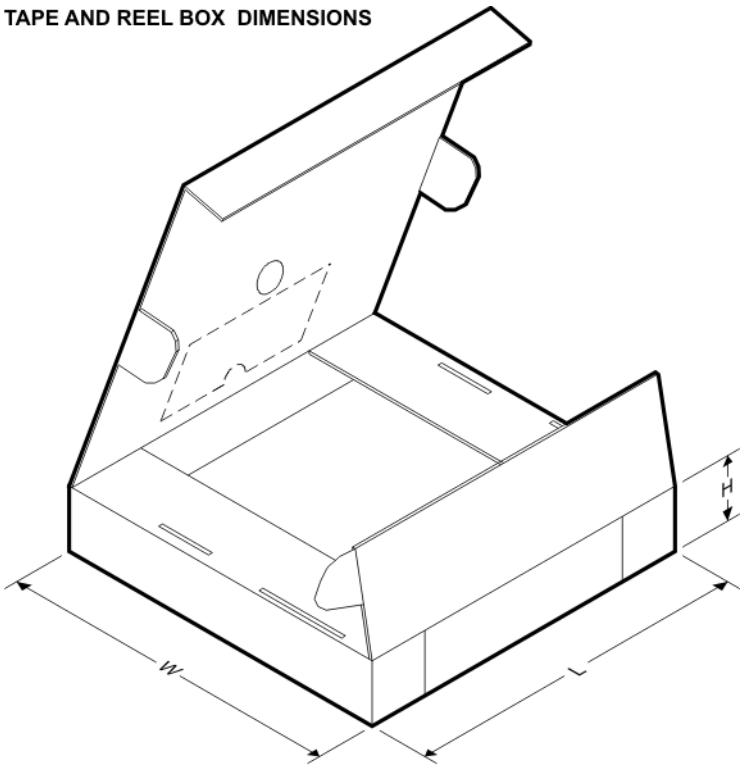
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24070RHLR	QFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
BQ24070RHLR	QFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.3	8.0	12.0	Q1
BQ24070RHLT	QFN	RHL	20	250	180.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
BQ24070RHLT	QFN	RHL	20	250	180.0	12.4	3.8	4.8	1.3	8.0	12.0	Q1
BQ24070RHLT	QFN	RHL	20	250	180.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
BQ24071RHLR	QFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
BQ24071RHLR	QFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.3	8.0	12.0	Q1
BQ24071RHLT	QFN	RHL	20	250	180.0	12.4	3.8	4.8	1.3	8.0	12.0	Q1
BQ24071RHLT	QFN	RHL	20	250	180.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

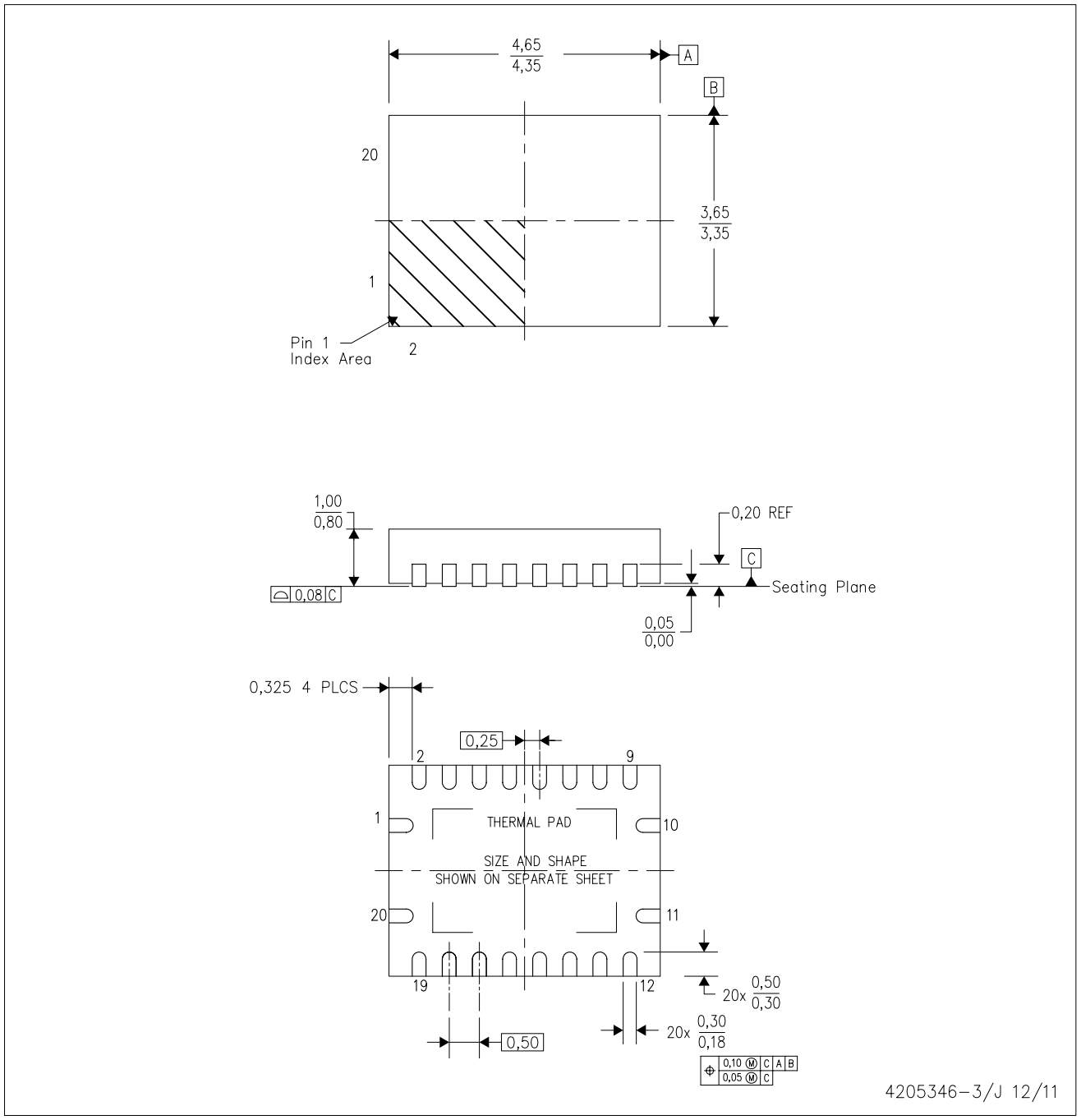
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24070RHLR	QFN	RHL	20	3000	346.0	346.0	29.0
BQ24070RHLR	QFN	RHL	20	3000	370.0	355.0	55.0
BQ24070RHLT	QFN	RHL	20	250	210.0	185.0	35.0
BQ24070RHLT	QFN	RHL	20	250	195.0	200.0	45.0
BQ24070RHLT	QFN	RHL	20	250	210.0	185.0	35.0
BQ24071RHLR	QFN	RHL	20	3000	346.0	346.0	29.0
BQ24071RHLR	QFN	RHL	20	3000	370.0	355.0	55.0
BQ24071RHLT	QFN	RHL	20	250	195.0	200.0	45.0
BQ24071RHLT	QFN	RHL	20	250	210.0	185.0	35.0

RHL (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

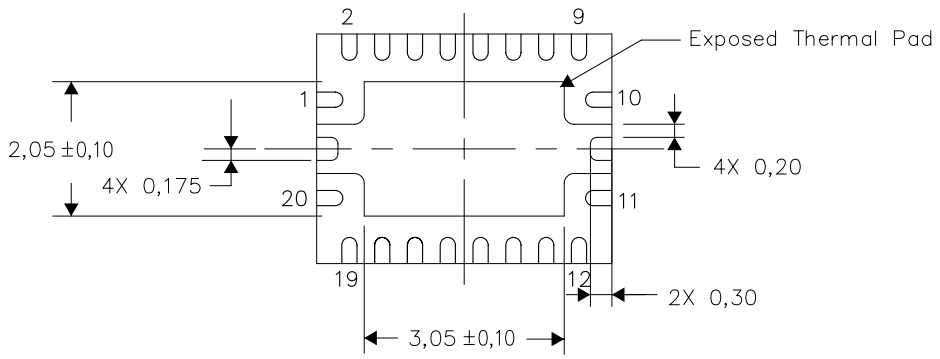
RHL (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



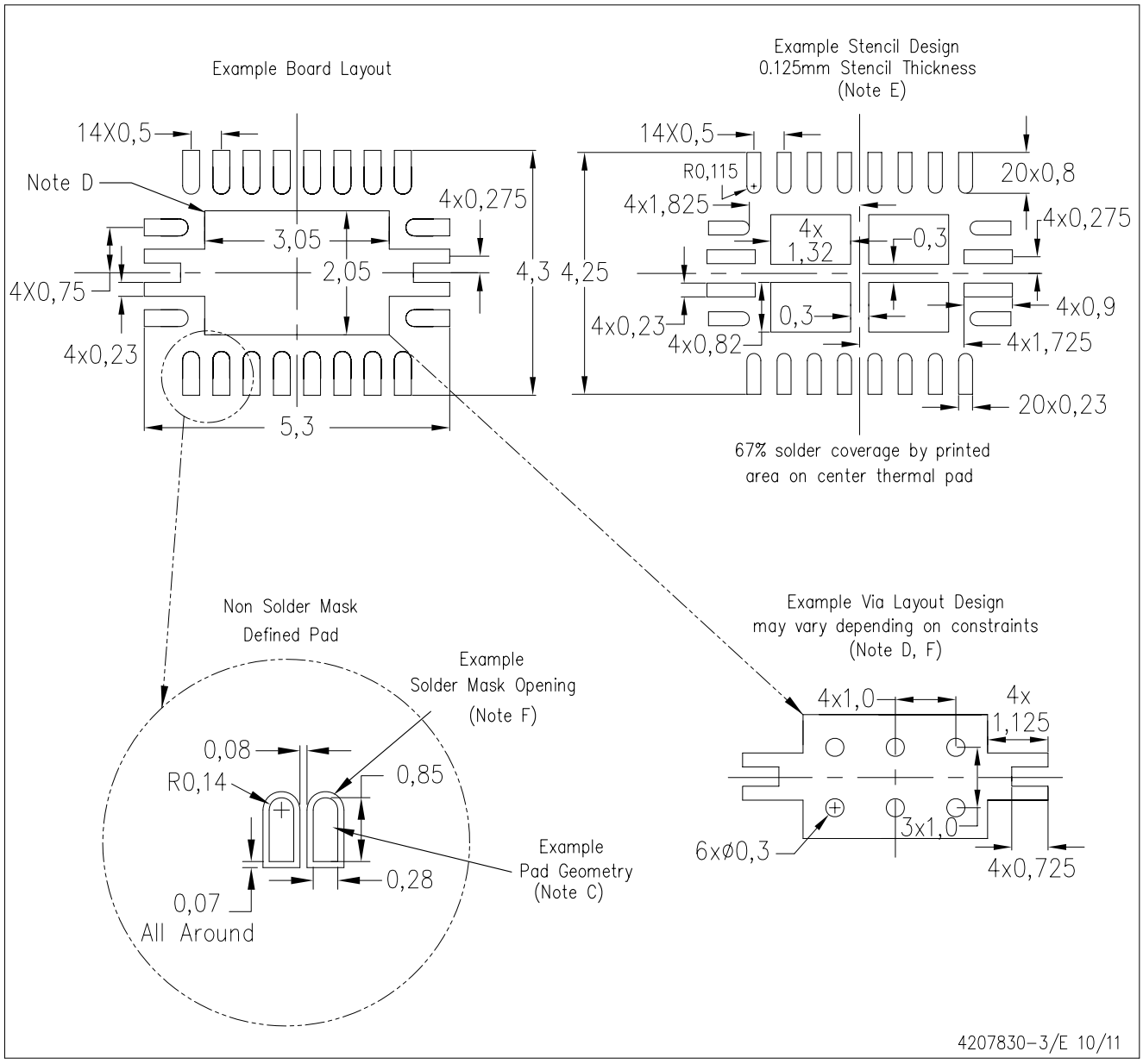
Bottom View

Exposed Thermal Pad Dimensions

4206363–3/L 09/11

NOTE: All linear dimensions are in millimeters

RHL (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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