

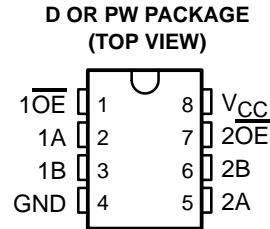
SN74CBTS3306 DUAL FET BUS SWITCH WITH SCHOTTKY DIODE CLAMPING

SCDS029H – JANUARY 1996 – REVISED NOVEMBER 2001

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels

description

The SN74CBTS3306 features independent line switches with Schottky diodes on the I/Os to clamp undershoot. Each switch is disabled when the associated output-enable (\overline{OE}) input is high.



ORDERING INFORMATION

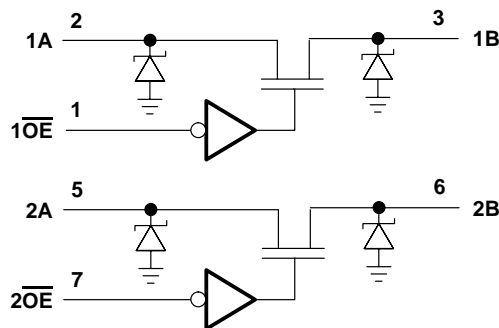
T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – D	Tube	SN74CBTS3306D	CR306
		Tape and reel	SN74CBTS3306DR	
	TSSOP – PW	Tape and reel	SN74CBTS3306PWR	CR306

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE
(each bus switch)**

INPUT \overline{OE}	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	97°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
V_{CC} Supply voltage	4	5.5	V
V_{IH} High-level control input voltage	2		V
V_{IL} Low-level control input voltage		0.8	V
T_A Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IK}	A or B inputs	$V_{CC} = 4.5$ V, $I_I = -18$ mA		-0.7	V
	Control inputs			-1.2	
I_I	I_{IL}	$V_{CC} = 5.5$ V, $V_I = GND$		-1	μ A
	I_{IH}	$V_{CC} = 5.5$ V, $V_I = 5.5$ V		150	
I_{CC}	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND			3	μ A
ΔI_{CC} §	Control inputs $V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs $V_I = 3$ V or 0			5	pF
$C_{io(OFF)}$	$V_O = 3$ V or 0, $\overline{OE} = V_{CC}$			6	pF
r_{on} ¶	$V_{CC} = 4$ V, TYP at $V_{CC} = 4$ V	$V_I = 2.4$ V, $I_I = 15$ mA	14	20	Ω
		$V_I = 0$, $I_I = 64$ mA	5	7	
	$V_{CC} = 4.5$ V	$V_I = 0$, $I_I = 30$ mA	5	7	
		$V_I = 2.4$ V, $I_I = 15$ mA	10	15	

‡ All typical values are at $V_{CC} = 5$ V (unless otherwise noted), $T_A = 25^\circ$ C.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B pin at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) pins.

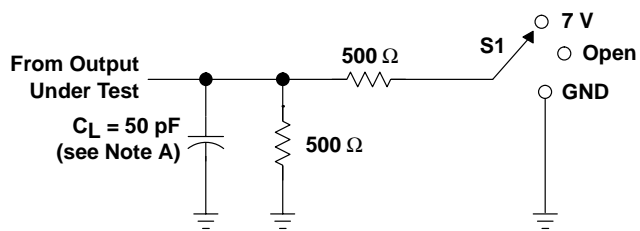


switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4$ V		$V_{CC} = 5$ V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}^\dagger	A or B	B or A	0.35		0.25		ns
t_{en}	\overline{OE}	A or B	5.6		1.8	5	ns
t_{dis}	\overline{OE}	A or B	4.6		1	4.3	ns

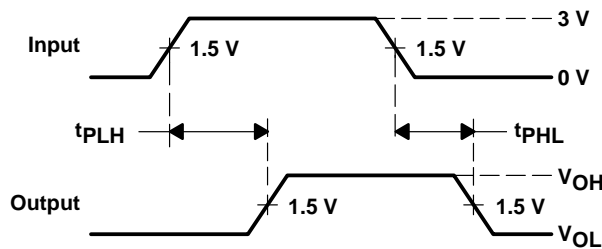
† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

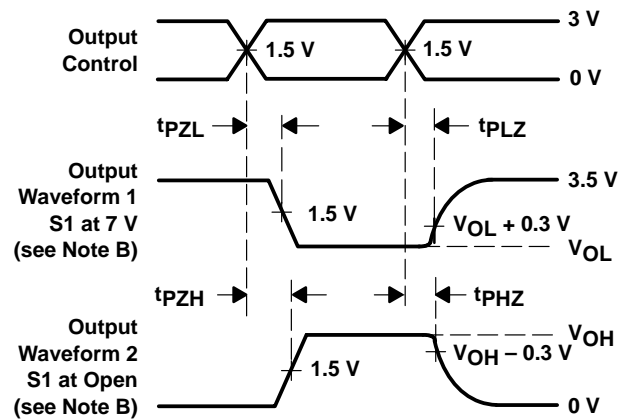


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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