- **Member of the Texas Instruments Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **Isolation Under Power-Off Conditions**

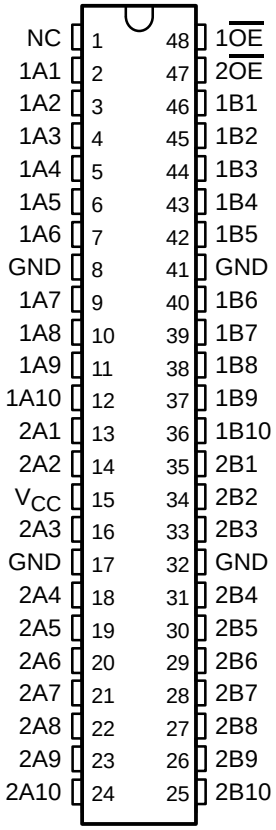
## description

The SN74CBTLV16210 provides 20 bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as dual 10-bit bus switches with separate output-enable ($\overline{OE}$) inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When $\overline{OE}$ is low, the associated 10-bit bus switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**DGG, DGV, OR DL PACKAGE**
**(TOP VIEW)**




NC – No internal connection

**ORDERING INFORMATION**

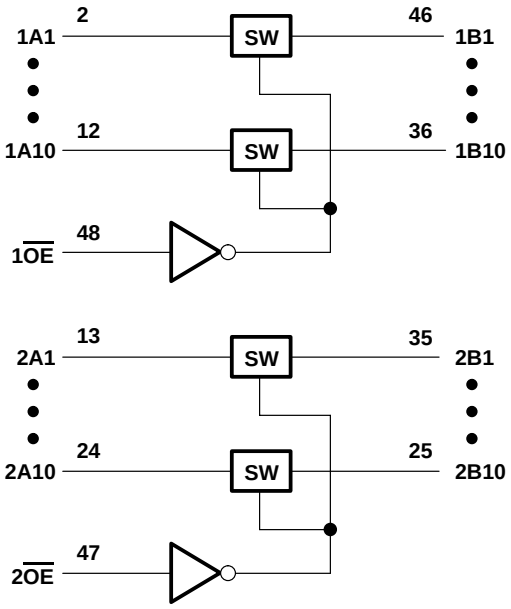
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | SSOP – DL | Tube | SN74CBTLV16210DL | CBTLV16210 |
| | | Tape and reel | SN74CBTLV16210DLR | |
| | TSSOP – DGG | Tape and reel | SN74CBTLV16210GR | CBTLV16210 |
| | TVSOP – DGV | Tape and reel | SN74CBTLV16210VR | CN210 |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

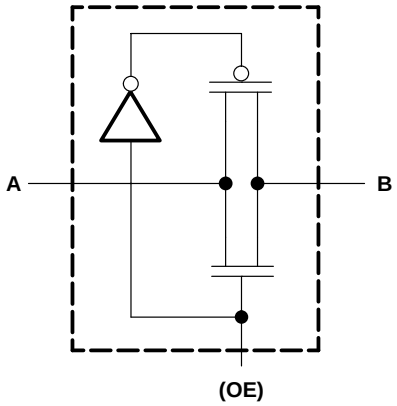
**FUNCTION TABLE**
**(each 10-bit bus switch)**

| INPUT $\overline{OE}$ | FUNCTION |
|---|---|
| L | A port = B port |
| H | Disconnect |

## logic diagram (positive logic)




## simplified schematic, each FET switch




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 4.6 V
Continuous channel current . . . . . 128 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) . . . . . –50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package . . . . . 70°C/W
DGV package . . . . . 58°C/W
DL package . . . . . 63°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.3 | 3.6 | V |
| $V_{IH}$ | High-level control input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level control input voltage | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

NOTE 3: All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 3 V, | $I_I$ = –18 mA | | | | –1.2 | V |
| $I_I$ | | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | | ±1 | μA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$= 0 to 3.6 V | | | | 10 | μA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, | $I_O$ = 0, | $V_I$ = $V_{CC}$ or GND | | | 10 | μA |
| $\Delta I_{CC}$‡ | Control inputs | $V_{CC}$ = 3.6 V, | One input at 3 V, | Other inputs at $V_{CC}$ or GND | | | 300 | μA |
| $C_i$ | Control inputs | $V_I$ = 3 V or 0 | | | | 4.5 | | pF |
| $C_{io(OFF)}$ | | $V_O$ = 3 V or 0, | $\overline{OE}$ = $V_{CC}$ | | | 6.5 | | pF |
| $r_{on}$§ | | $V_{CC}$ = 2.3 V, TYP at $V_{CC}$ = 2.5 V | $V_I$ = 0 | $I_I$ = 64 mA | | 5 | 8 | Ω |
| | | | | $I_I$ = 24 mA | | 5 | 8 | |
| | | | $V_I$ = 1.7 V, | $I_I$ = 15 mA | | 27 | 40 | |
| | | $V_{CC}$ = 3 V | $V_I$ = 0 | $I_I$ = 64 mA | | 5 | 7 | |
| | | | | $I_I$ = 24 mA | | 5 | 7 | |
| | | | $V_I$ = 2.4 V, | $I_I$ = 15 mA | | 10 | 15 | |

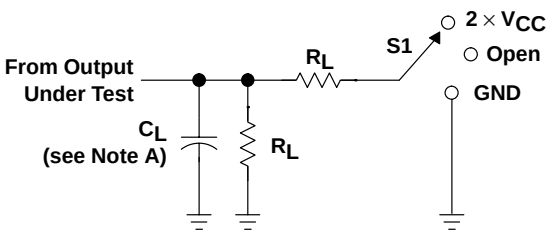
† All typical values are at $V_{CC}$ = 3.3 V (unless otherwise noted), $T_A$ = 25°C.
‡ This is the increase in supply current for each input that is at the specified voltage level rather than $V_{CC}$ or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{pd}$¶ | A or B | B or A | | 0.15 | | 0.25 | ns |
| $t_{en}$ | $\overline{OE}$ | A or B | 1 | 6.8 | 1 | 6 | ns |
| $t_{dis}$ | $\overline{OE}$ | A or B | 1 | 7.3 | 1 | 7.4 | ns |

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

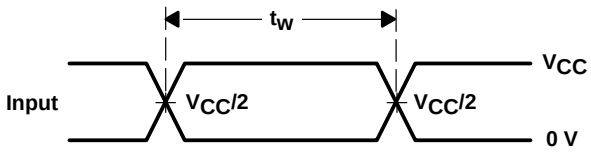
## PARAMETER MEASUREMENT INFORMATION



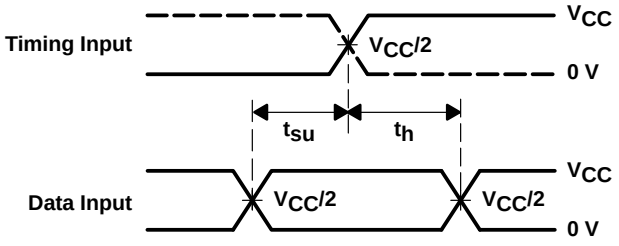

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

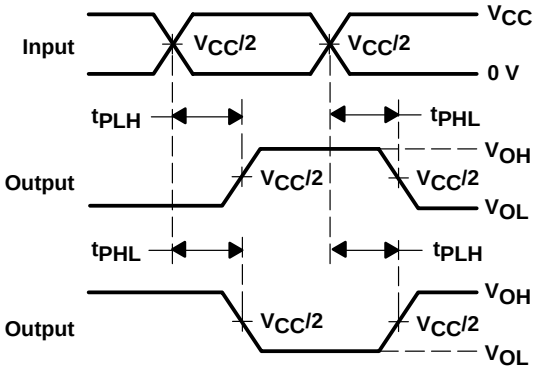
| $V_{CC}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|
| 2.5 V ±0.2 V | 30 pF | 500 Ω | 0.15 V |
| 3.3 V ±0.3 V | 50 pF | 500 Ω | 0.3 V |



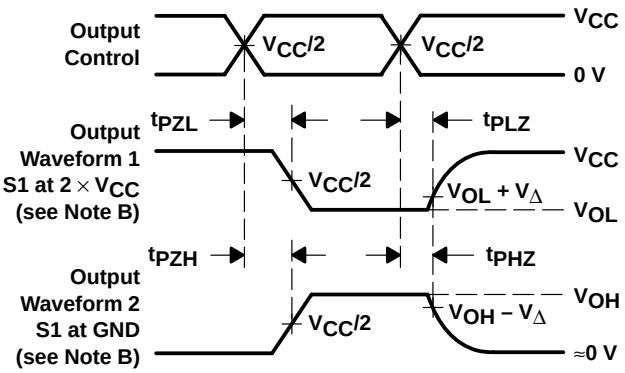

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

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