

SN74ALVC164245

16-BIT 2.5-V TO 3.3-V/3.3-V TO 5-V LEVEL-SHIFTING TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS416J – MARCH 1994 – REVISED JUNE 2002

- Member of the Texas Instruments Widebus™ Family
- Latch-Up Performance Exceeds 250 mA Per JESD 17

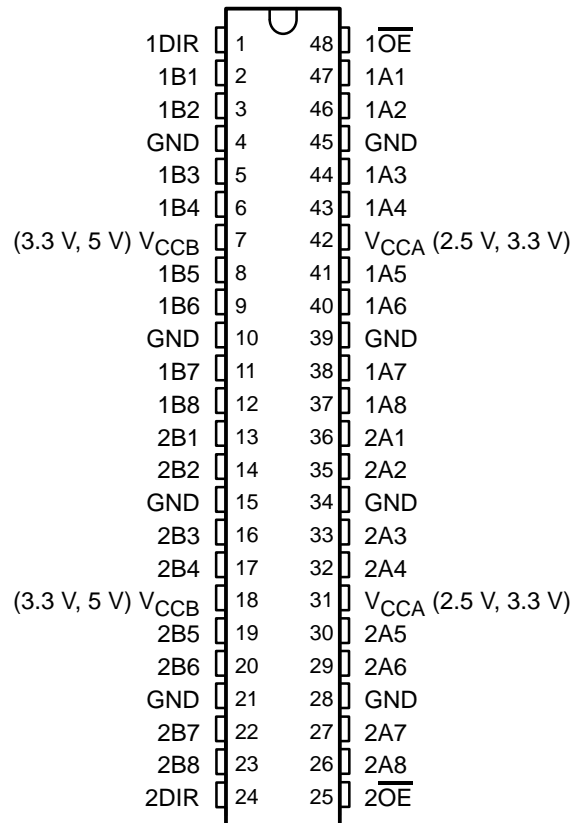
description

This 16-bit (dual-octal) noninverting bus transceiver contains two separate supply rails. B port has V_{CCB} , which is set to operate at 3.3 V and 5 V. A port has V_{CCA} , which is set to operate at 2.5 V and 3.3 V. This allows for translation from a 2.5-V to a 3.3-V environment, and vice versa, or from a 3.3-V to a 5-V environment, and vice versa.

The SN74ALVC164245 is designed for asynchronous communication between data buses.

To ensure the high-impedance state during power up or power down, the output-enable (\overline{OE}) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DGG OR DL PACKAGE (TOP VIEW)



ORDERING INFORMATION

| TA | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|-------------|---------------|-----------------------|------------------|
| -40°C to 85°C | SSOP – DL | Tube | SN74ALVC164245DL | ALVC164245 |
| | | Tape and reel | SN74ALVC164245DLR | |
| | TSSOP – DGG | Tape and reel | SN74ALVC164245DGGR | ALVC164245 |
| | VFBGA – GQL | Tape and reel | SN74ALVC164245KR | VC4245 |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each 8-bit section)

| INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |



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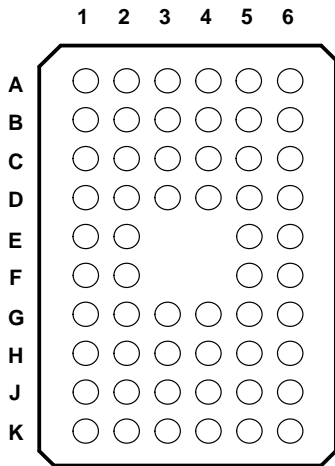
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SCAS416J – MARCH 1994 – REVISED JUNE 2002

**GQL PACKAGE
(TOP VIEW)**

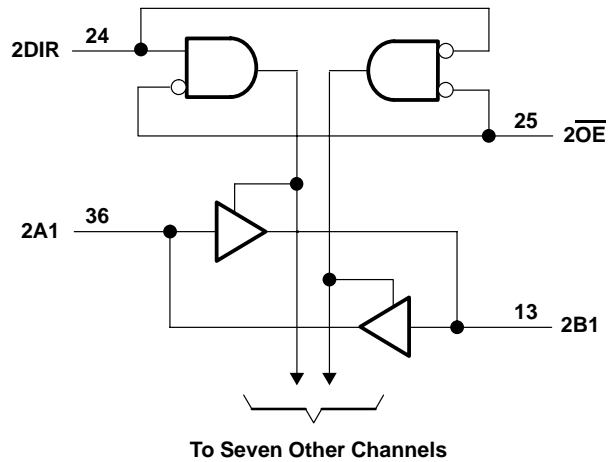
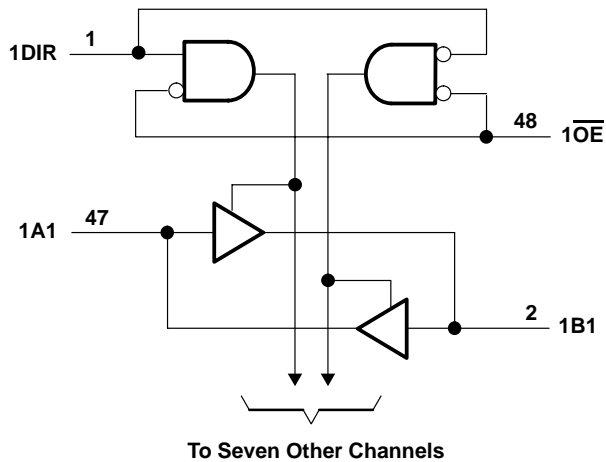


terminal assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|------|-----|------------------|------------------|-----|------------------|
| A | 1DIR | NC | NC | NC | NC | $\overline{1OE}$ |
| B | 1B2 | 1B1 | GND | GND | 1A1 | 1A2 |
| C | 1B4 | 1B3 | V _{CCB} | V _{CCA} | 1A3 | 1A4 |
| D | 1B6 | 1B5 | GND | GND | 1A5 | 1A6 |
| E | 1B8 | 1B7 | | | 1A7 | 1A8 |
| F | 2B1 | 2B2 | | | 2A2 | 2A1 |
| G | 2B3 | 2B4 | GND | GND | 2A4 | 2A3 |
| H | 2B5 | 2B6 | V _{CCB} | V _{CCA} | 2A6 | 2A5 |
| J | 2B7 | 2B8 | GND | GND | 2A8 | 2A7 |
| K | 2DIR | NC | NC | NC | NC | $\overline{2OE}$ |

NC – No internal connection

logic diagram (positive logic)



Pin numbers shown are for the DGG and DL packages.

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SCAS416J – MARCH 1994 – REVISED JUNE 2002

absolute maximum ratings over operating free-air temperature range for V_{CCB} at 5 V and V_{CCA} at 3.3 V (unless otherwise noted)[†]

| | |
|--|-----------------------------|
| Supply voltage range: V_{CCA} | –0.5 V to 4.6 V |
| V_{CCB} | –0.5 V to 6 V |
| Input voltage range, V_I : Except I/O ports (see Note 1) | –0.5 V to 6 V |
| I/O port A (see Note 2) | –0.5 V to $V_{CCA} + 0.5$ V |
| I/O port B (see Note 1) | –0.5 V to $V_{CCB} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | –50 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | –50 mA |
| Continuous output current, I_O | ±50 mA |
| Continuous current through each V_{CC} or GND | ±100 mA |
| Package thermal impedance, θ_{JA} (see Note 3): DGG package | 70°C/W |
| DL package | 63°C/W |
| GQL package | 42°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. This value is limited to 6 V maximum.
 2. This value is limited to 4.6 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions for V_{CCB} at 3.3 V and 5 V (see Note 4)

| | | MIN | MAX | UNIT |
|---------------------|------------------------------------|-----|----------------------------|------|
| V_{CCB} | Supply voltage | 3 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | V |
| V_{IL} | Low-level input voltage | | $V_{CCB} = 3$ V to 3.6 V | 0.7 |
| | | | $V_{CCB} = 4.5$ V to 5.5 V | 0.8 |
| V_{IA} | Input voltage | 0 | V_{CCB} | V |
| V_{OB} | Output voltage | 0 | V_{CCB} | V |
| I_{OH} | High-level output current | | –24 | mA |
| I_{OL} | Low-level output current | | 24 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | ns/V |
| T_A | Operating free-air temperature | –40 | 85 | °C |

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74ALVC164245

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SCAS416J – MARCH 1994 – REVISED JUNE 2002

recommended operating conditions for V_{CCA} at 2.5 V and 3.3 V (see Note 4)

| | | MIN | MAX | UNIT |
|---------------------|------------------------------------|---|-----------|------|
| V_{CCA} | Supply voltage | 2.3 | 3.6 | V |
| V_{IH} | High-level input voltage | $V_{CCA} = 2.3 \text{ V to } 2.7 \text{ V}$ | 1.7 | V |
| | | $V_{CCA} = 3 \text{ V to } 3.6 \text{ V}$ | 2 | |
| V_{IL} | Low-level input voltage | $V_{CCA} = 2.3 \text{ V to } 2.7 \text{ V}$ | 0.7 | V |
| | | $V_{CCA} = 3 \text{ V to } 3.6 \text{ V}$ | 0.8 | |
| V_{IB} | Input voltage | 0 | V_{CCA} | V |
| V_{OA} | Output voltage | 0 | V_{CCA} | V |
| I_{OH} | High-level output current | $V_{CCA} = 2.3 \text{ V}$ | -18 | mA |
| | | $V_{CCA} = 3 \text{ V}$ | -24 | |
| I_{OL} | Low-level output current | $V_{CCA} = 2.3 \text{ V}$ | 18 | mA |
| | | $V_{CCA} = 3 \text{ V}$ | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | ns/V |
| T_A | Operating free-air temperature | -40 | 85 | °C |

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range for $V_{CCA} = 2.7 \text{ V to } 3.6 \text{ V}$ and $V_{CCB} = 4.5 \text{ V to } 5.5 \text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CCA} | V_{CCB} | MIN | TYP† | MAX | UNIT | |
|--------------------|-----------------------------|--|----------------|----------------|------|------|----------|---------------|
| V_{OH} (B to A) | $I_{OH} = -100 \mu\text{A}$ | 2.7 V to 3.6 V | | $V_{CC}-0.2$ | | | V | |
| | $I_{OH} = -12 \text{ mA}$ | 2.7 V | | 2.2 | | | | |
| | | 3 V | | 2.4 | | | | |
| | $I_{OH} = -24 \text{ mA}$ | 3 V | | 2 | | | | |
| V_{OH} (A to B) | $I_{OH} = -100 \mu\text{A}$ | | 4.5 V | 4.3 | | | V | |
| | | | 5.5 V | 5.3 | | | | |
| | $I_{OH} = -24 \text{ mA}$ | | 4.5 V | 3.7 | | | | |
| | | 5.5 V | 4.7 | | | | | |
| V_{OL} (B to A) | $I_{OL} = 100 \mu\text{A}$ | 2.7 V to 3.6 V | | | | 0.2 | V | |
| | $I_{OL} = 12 \text{ mA}$ | 2.7 V | | | | 0.4 | | |
| | | 3 V | | | | 0.55 | | |
| V_{OL} (A to B) | $I_{OL} = 100 \mu\text{A}$ | | 4.5 V to 5.5 V | | | 0.2 | V | |
| | $I_{OL} = 24 \text{ mA}$ | | 4.5 V to 5.5 V | | | 0.55 | | |
| I_I | Control inputs | $V_I = V_{CCA}/V_{CCB}$ or GND | 3.6 V | 5.5 V | | | ± 5 | μA |
| I_{OZ}^\ddagger | A or B ports | $V_O = V_{CCA}/V_{CCB}$ or GND | 3.6 V | 5.5 V | | | ± 10 | μA |
| I_{CC} | | $V_I = V_{CCA}/V_{CCB}$ or GND, $I_O = 0$ | 5.5 V | 5.5 V | | | 40 | μA |
| ΔI_{CC}^\S | | One input at $V_{CCA}/V_{CCB} - 0.6 \text{ V}$, Other inputs at V_{CCA}/V_{CCB} or GND | 3 V to 3.6 V | 4.5 V to 5.5 V | | | 750 | μA |
| C_i | Control inputs | $V_I = V_{CCA}/V_{CCB}$ or GND | 3.3 V | 5 V | 6.5 | | pF | |
| C_{io} | A or B ports | $V_O = V_{CCA}/V_{CCB}$ or GND | 3.3 V | 3.3 V | 8.5 | | pF | |

† Typical values are measured at $V_{CCA} = 3.3 \text{ V}$ and $V_{CCB} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than at 0 or the associated V_{CC} .



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SCAS416J – MARCH 1994 – REVISED JUNE 2002

electrical characteristics over recommended operating free-air temperature range for $V_{CCA} = 2.3\text{ V to }2.7\text{ V}$ and $V_{CCB} = 3\text{ V to }3.6\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CCA} | V_{CCB} | MIN | MAX | UNIT |
|--------------------------|----------------|---|----------------|--------------|---------------|----------|---------------|
| V_{OH} (B to A) | | $I_{OH} = -100\ \mu\text{A}$ | 2.3 V to 2.7 V | 3 V to 3.6 V | $V_{CCA}-0.2$ | | V |
| | | $I_{OH} = -8\ \text{mA}$ | 2.3 V | 3 V to 3.6 V | 1.7 | | |
| | | $I_{OH} = -12\ \text{mA}$ | 2.7 V | 3 V to 3.6 V | 1.8 | | |
| V_{OH} (A to B) | | $I_{OH} = -100\ \mu\text{A}$ | 2.3 V to 2.7 V | 3 V to 3.6 V | $V_{CCB}-0.2$ | | V |
| | | $I_{OH} = -18\ \text{mA}$ | 2.3 V to 2.7 V | 3 V | 2.2 | | |
| V_{OL} (B to A) | | $I_{OL} = 100\ \mu\text{A}$ | 2.3 V to 2.7 V | 3 V to 3.6 V | | 0.2 | V |
| | | $I_{OL} = 12\ \text{mA}$ | 2.3 V | 3 V to 3.6 V | | 0.6 | |
| V_{OL} (A to B) | | $I_{OL} = 100\ \mu\text{A}$ | 2.3 V to 2.7 V | 3 V to 3.6 V | | 0.2 | V |
| | | $I_{OL} = 18\ \text{mA}$ | 2.3 V | 3 V | | 0.55 | |
| I_I | Control inputs | $V_I = V_{CCA}/V_{CCB}$ or GND | 2.3 V to 2.7 V | 3 V to 3.6 V | | ± 5 | μA |
| I_{OZ}^\dagger | A or B ports | $V_O = V_{CCA}/V_{CCB}$ or GND | 2.3 V to 2.7 V | 3 V to 3.6 V | | ± 10 | μA |
| I_{CC} | | $V_I = V_{CCA}/V_{CCB}$ or GND, $I_O = 0$ | 2.3 V to 2.7 V | 3 V to 3.6 V | | 20 | μA |
| ΔI_{CC}^\ddagger | | One input at $V_{CCA}/V_{CCB} - 0.6\text{ V}$, Other inputs at V_{CCA}/V_{CCB} or GND | 2.3 V to 2.7 V | 3 V to 3.6 V | | 750 | μA |

† For I/O ports, the parameter I_{OZ} includes the input leakage current.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than at 0 or the associated V_{CC} .

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1-4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$ | | $V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$ | | | | UNIT |
|-----------|-----------------|-------------|---|-----|---|-----|---|-----|------|
| | | | $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ | | $V_{CCA} = 2.7\text{ V}$ | | $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A | B | 7.6 | | 5.9 | | 1 | 5.8 | ns |
| | B | A | 7.6 | | 6.7 | | 1.2 | 5.8 | |
| t_{en} | \overline{OE} | B | 11.5 | | 9.3 | | 1 | 8.9 | ns |
| t_{dis} | \overline{OE} | B | 10.5 | | 9.2 | | 2.1 | 9.5 | ns |
| t_{en} | \overline{OE} | A | 12.3 | | 10.2 | | 2 | 9.1 | ns |
| t_{dis} | \overline{OE} | A | 9.3 | | 9 | | 2.9 | 8.6 | ns |

operating characteristics, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | $V_{CCB} = 3.3\text{ V}$ | | $V_{CCB} = 5\text{ V}$ | | UNIT |
|-----------|-------------------------------|---|--------------------------|--|--------------------------|----|------|
| | | | $V_{CCA} = 2.5\text{ V}$ | | $V_{CCA} = 3.3\text{ V}$ | | |
| | | | TYP | | TYP | | |
| C_{pd} | Power dissipation capacitance | $C_L = 50\ \text{pF}, f = 10\ \text{MHz}$ | Outputs enabled (B) | | 55 | 56 | pF |
| | Outputs disabled (B) | | 27 | | 6 | | |
| | Outputs enabled (A) | $C_L = 50\ \text{pF}, f = 10\ \text{MHz}$ | 118 | | 56 | | |
| | | | Outputs disabled (A) | | 58 | | |



power-up considerations†

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. Take these precautions to guard against such power-up problems.

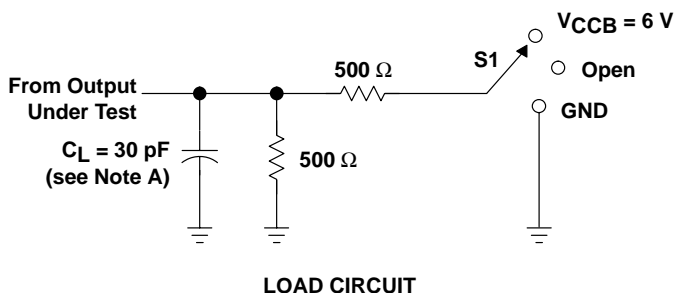
1. Connect ground before any supply voltage is applied.
2. Next, power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie \overline{OE} to V_{CCA} with a pullup resistor so that it ramps with V_{CCA} .
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA} . Otherwise, keep DIR low.

† Refer to the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, literature number SCEA021.

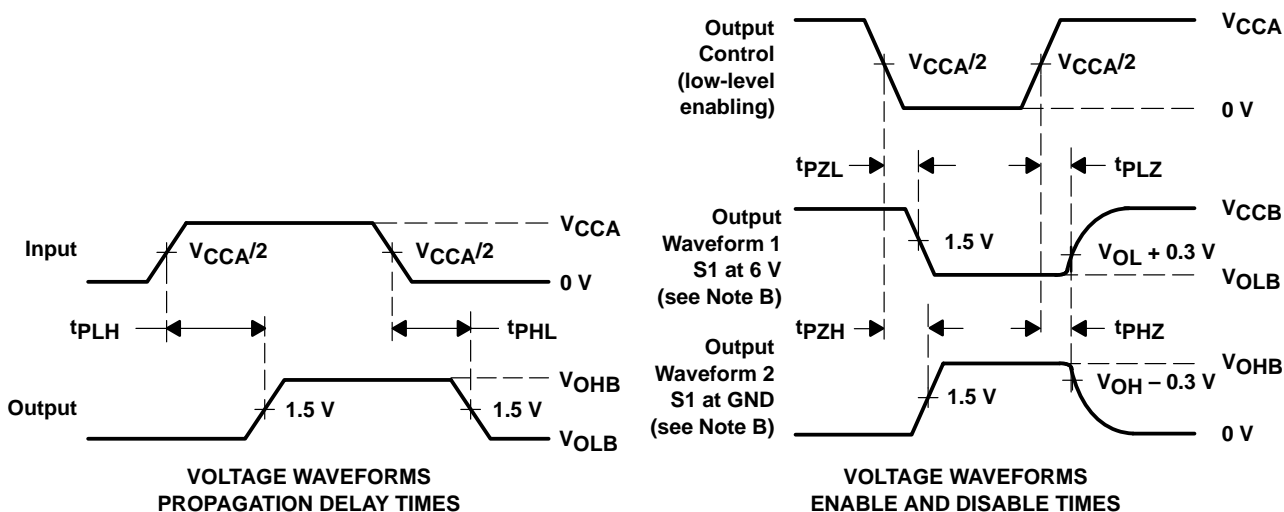
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PARAMETER MEASUREMENT INFORMATION
 $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ TO $V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$



| TEST | S1 |
|--|---------------------------------------|
| t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH} | Open $V_{CCB} = 6\text{ V}$ GND |



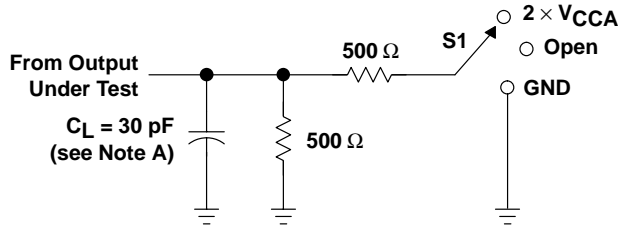
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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WITH 3-STATE OUTPUTS

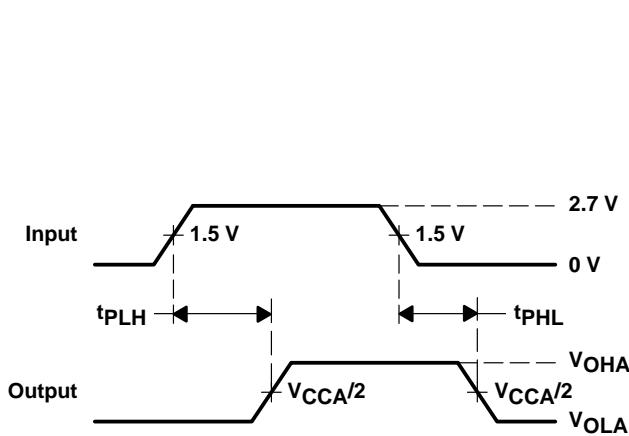
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PARAMETER MEASUREMENT INFORMATION
 $V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$ TO $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$

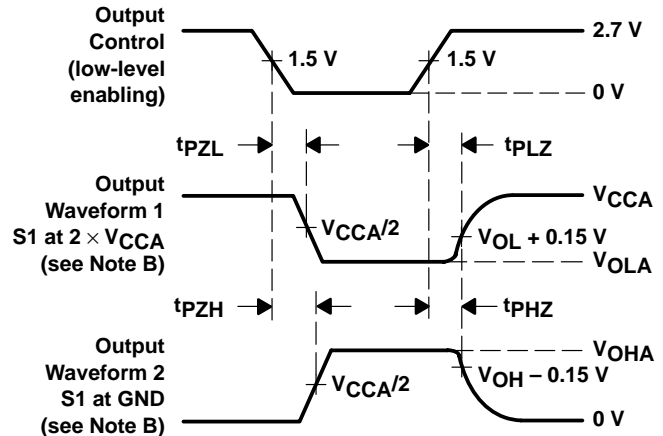


LOAD CIRCUIT

| TEST | S1 |
|-------------------|--------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CCA}$ |
| t_{PHZ}/t_{PZH} | GND |



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

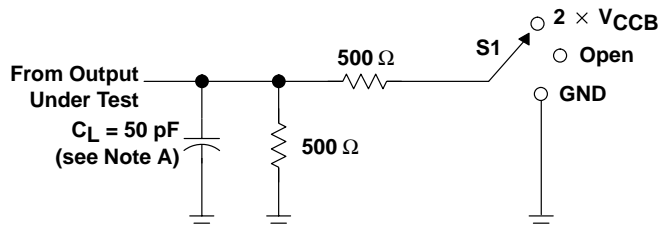
Figure 2. Load Circuit and Voltage Waveforms

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SCAS416J – MARCH 1994 – REVISED JUNE 2002

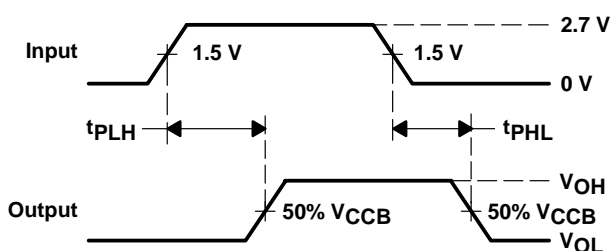
PARAMETER MEASUREMENT INFORMATION

$V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V TO } V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$

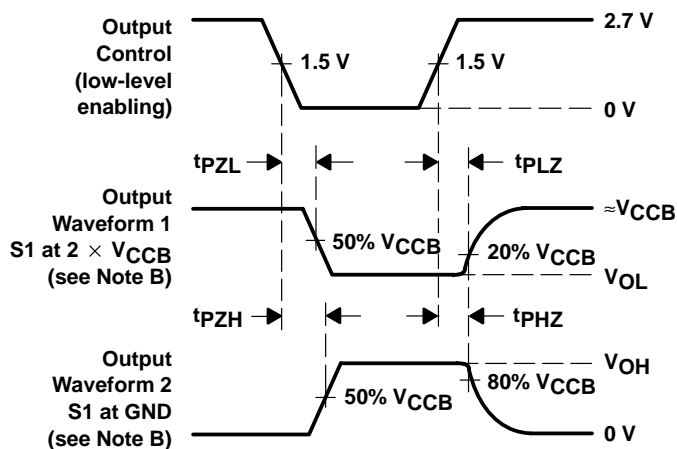


LOAD CIRCUIT

| TEST | S1 |
|-------------------|--------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | 2 $\times V_{CCB}$ |
| t_{PHZ}/t_{PZH} | GND |



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

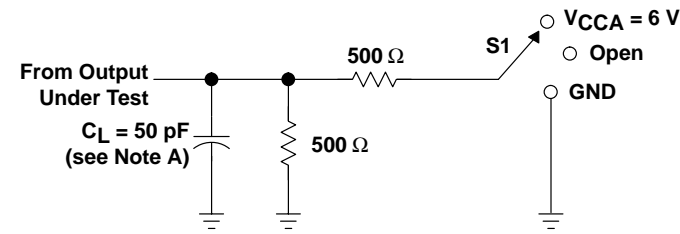
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

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WITH 3-STATE OUTPUTS

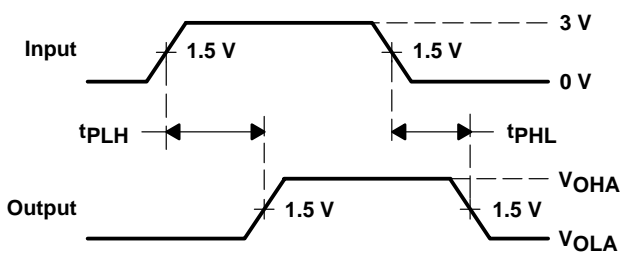
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PARAMETER MEASUREMENT INFORMATION
 $V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$ TO $V_{CCA} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$

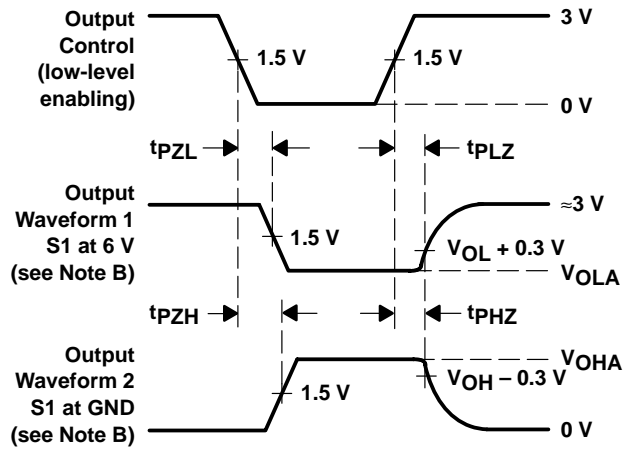


LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | $V_{CCA} = 6\text{ V}$ |
| t_{PHZ}/t_{PZH} | GND |



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 4. Load Circuit and Voltage Waveforms

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265