

EMC OPTIMIZED CAN TRANSCEIVER

Check for Samples: [SN65HVD1050](#)

FEATURES

- Improved Replacement for the TJA1050
- High Electromagnetic Immunity (EMI)
- Very Low Electromagnetic Emissions (EME)
- Meets or Exceeds the Requirements of ISO 11898-2
- Bus-Fault Protection of -27 V to 40 V
- Dominant Time-Out Function
- Power-Up/Down Glitch-Free Bus Inputs and Outputs
 - High Input Impedance with Low V_{CC}
 - Monotonic Outputs During Power Cycling

APPLICATIONS

- Industrial Automation
 - DeviceNet™ Data Buses (Vendor ID #806)
- SAE J2284 High Speed CAN for Automotive Applications
- SAE J1939 Standard Data Bus Interface
- ISO 11783 Standard Data Bus Interface
- NMEA 2000 Standard Data Bus Interface

DESCRIPTION

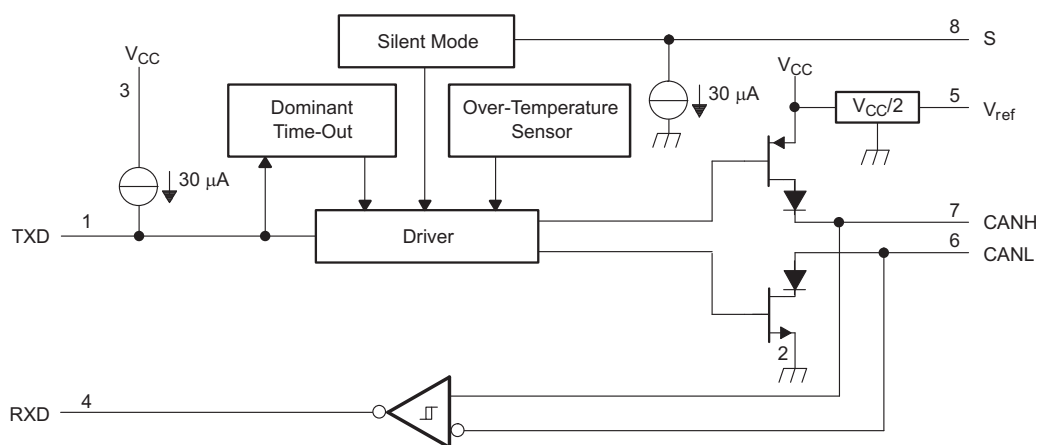
The SN65HVD1050 meets or exceeds the specifications of the ISO 11898 standard for use in applications employing a Controller Area Network (CAN).

As a CAN transceiver, this device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to 1 megabit per second (Mbps)⁽¹⁾.

Designed for operation in especially harsh environments, the HVD1050 features cross-wire, over-voltage and loss of ground protection from -27 V to 40V, over-temperature shut down, a -12 V to 12 V common-mode range, and will withstand voltage transients from -200 V to 200 V according to ISO 7637.

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

FUNCTION BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

Pin 8 provides for two different modes of operation: high-speed or silent mode. The high-speed mode of operation is selected by connecting S (pin 8) to ground.

If a high logic level is applied to the S pin of the SN65HVD1050, the device enters a listen-only silent mode during which the driver is switched off while the receiver remains fully functional.

In silent mode, all bus activity is passed by the receiver output to the local protocol controller. When data transmission is required, the local protocol controller reverses this low-current silent mode by placing a logic-low on the S pin to resume full operation.

A dominant-time-out circuit in the SN65HVD1050 prevents the driver from blocking network communication with a hardware or software failure. The time-out circuit is triggered by a falling edge on TXD (pin 1). If no rising edge is seen before the time-out constant of the circuit expires, the driver is disabled. The circuit is then reset by the next rising edge on TXD.

V_{ref} (pin 5) is available as a $V_{CC}/2$ voltage reference.

The SN65HVD1050 is characterized for operation from -40°C to 125°C .

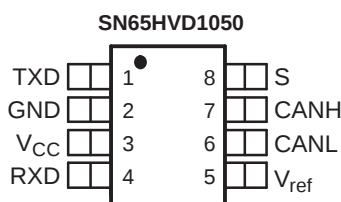


Table 1. ORDERING INFORMATION

PART NUMBER	PACKAGE	MARKED AS	ORDERING NUMBER
SN65HVD1050	SOIC-8	VP1050	SN65HVD1050D (rail)
			SN65HVD1050DR (reel)

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

	UNIT
V_{CC} Supply voltage ⁽²⁾	$-0.3\text{ V to }7\text{ V}$
Voltage range at any bus terminal (CANH, CANL, V_{ref})	$-27\text{ V to }40\text{ V}$
I_O Receiver output current	20 mA
V_I Voltage input, transient pulse ⁽³⁾ (CANH, CANL)	$-200\text{ V to }200\text{ V}$
V_I Voltage input range (TXD, S)	$-0.5\text{ V to }6\text{ V}$
T_J Junction temperature	$-55^{\circ}\text{C to }170^{\circ}\text{C}$

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

(3) Tested in accordance with ISO 7637, test pulses 1, 2, 3a, 3b, 5, 6, and 7.

ELECTROSTATIC DISCHARGE PROTECTION⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		VALUE
IEC Contact Discharge	IEC 61000-4-2	Bus terminals vs GND	±6 kV
Human Body Model	JEDEC Standard 22, Test Method A114-C.01	Bus terminals vs GND	±8 kV
		All pins	±4 kV
Field-Induced-Charged Device Model	JEDEC Standard 22, Test Method C101	All pins	±1.5 kV
Machine Model	ANSI/ESDS5.2-1996		±200 V

(1) All typical values at 25°C.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.5		5.5	V
V _I or V _{IC}	Voltage at any bus terminal (separately or common mode)		–12		12	V
V _{IH}	High-level input voltage	TXD, S	2.1		V _{CC}	V
V _{IL}	Low-level input voltage		0		0.8	V
V _{ID}	Differential input voltage		–7		7	V
I _{OH}	High-level output current	Driver	–70			mA
		Receiver	–2			
I _{OL}	Low-level output current	Driver			70	mA
		Receiver			2	
T _J	Junction temperature	See <i>Thermal Characteristics</i> table, 1 Mbps minimum signaling rate with R _L = 54Ω	–40		150	°C
	Signaling Rate		20			kbps

SUPPLY CURRENT

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
I _{CC}	5-V Supply current	Silent mode	S at V _{CC} , V _I = V _{CC}			6	10	mA
		Dominant	V _I = 0 V, 60 Ω Load, S at 0 V	4.75V < V _{CC} < 5.25V	50	70		
				4.5V < V _{CC} < 5.5V		75		
		Recessive	V _I = V _{CC} , No Load, S at 0 V			6	10	

DEVICE SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{d(LOOP1)}	Total loop delay, driver input to receiver output, recessive to dominant	Figure 9, S at 0V	4.75V < V _{CC} < 5.25V	90		190	ns
t _{d(LOOP2)}	Total loop delay, driver input to receiver output, dominant to recessive		4.5V < V _{CC} < 5.5V	85		195	
			4.75V < V _{CC} < 5.25V	90		190	
			4.5V < V _{CC} < 5.5V	85		195	

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DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT		
V _{O(D)}	Bus output voltage (Dominant)	CANH	V _I = 0 V, S at 0 V, R _L = 60 Ω, See Figure 1 and Figure 2	4.75V < V _{CC} < 5.25V	2.9	3.4	4.5	V	
				4.5V < V _{CC} < 5.5V	2.75		5.2		
				CANL	4.75V < V _{CC} < 5.25V	0.8			1.5
					4.5V < V _{CC} < 5.5V				1.6
V _{O(R)}	Bus output voltage (Recessive)		V _I = 3 V, S at 0 V, R _L = 60 Ω, See Figure 1 and Figure 2	4.75V < V _{CC} < 5.25V	2	2.3	3	V	
				4.5V < V _{CC} < 5.5V	1.8		3		
V _{OD(D)}	Differential output voltage (Dominant)		V _I = 0 V, R _L = 60 Ω, S at 0 V, See Figure 1 , Figure 2 , and Figure 3	4.75V < V _{CC} < 5.25V	1.5		3	V	
				4.5V < V _{CC} < 5.5V	1.4		3		
					4.75V < V _{CC} < 5.25V	1.4		3	V
					4.5V < V _{CC} < 5.5V	1.3		3	
V _{OD(R)}	Differential output voltage (Recessive)		V _I = 3 V, S at 0 V, See Figure 1 and Figure 2		–0.012		0.012	V	
				V _I = 3 V, S at 0 V, No Load	–0.5		0.05		
V _{OC(ss)}	Steady state common-mode output voltage		S at 0 V, Figure 8	4.75V < V _{CC} < 5.25V	2	2.3	3	V	
				4.5V < V _{CC} < 5.5V	1.9		3		
ΔV _{OC(ss)}	Change in steady-state common-mode output voltage					30		mV	
I _{IH}	High-level input current, TXD input	V _I at V _{CC}			–2		2	μA	
I _{IL}	Low-level input current, TXD input	V _I at 0 V			–50		–10		
I _{O(off)}	Power-off TXD output current	V _{CC} at 0 V, TXD at 5 V					1		
I _{OS(ss)}	Short-circuit steady-state output current	V _{CANH} = –12 V, CANL Open, See Figure 11			–105	–72		mA	
		V _{CANH} = 12 V, CANL Open, See Figure 11				0.36	1		
		V _{CANL} = –12 V, CANH Open, See Figure 11			–1	–0.5			
		V _{CANL} = 12 V, CANH Open, See Figure 11				71	105		
C _O	Output capacitance	See receiver input capacitance							

(1) All typical values are at 25°C with a 5-V supply.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	S at 0 V, See Figure 4		25	65	120	ns
t _{PHL}	Propagation delay time, high-to-low-level output			25	45	90	
t _r	Differential output signal rise time				25		
t _f	Differential output signal fall time				50		
t _{en}	Enable time from silent mode to dominant	See Figure 7				1	μs
t _(dom)	Dominant time-out	↓V _I , See Figure 10	4.75V < V _{CC} < 5.25V	300	450	700	μs
			4.5V < V _{CC} < 5.5V	280		700	

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+} Positive-going input threshold voltage	S at 0 V, See Table 4		800	900	mV
V _{IT-} Negative-going input threshold voltage		500	650		
V _{hys} Hysteresis voltage (V _{IT+} – V _{IT-})		100	125		
V _{OH} High-level output voltage	I _O = –2 mA, See Figure 6 4.75V < V _{CC} < 5.25V 4.5V < V _{CC} < 5.5V	4	4.6		V
V _{OL} Low-level output voltage		3.8			
I _{I(off)} Power-off bus input current	I _O = 2 mA, See Figure 6 CANH or CANL = 5 V, Other pin at 0 V, V _{CC} at 0 V, TXD at 0 V		165	250	μA
I _{O(off)} Power-off RXD leakage current	V _{CC} at 0 V, RXD at 5 V			20	μA
C _I Input capacitance to ground, (CANH or CANL)	TXD at 3 V, V _I = 0.4 sin (4E6πt) + 2.5 V		13		pF
C _{ID} Differential input capacitance	TXD at 3 V, V _I = 0.4 sin (4E6πt)		5		
R _{ID} Differential input resistance	TXD at 3 V, S at 0 V	30		80	kΩ
R _{IN} Input resistance, (CANH or CANL)		15	30	40	
R _{I(m)} Input resistance matching [1 – (R _{IN (CANH)} / R _{IN (CANL)})] x 100%	V _(CANH) = V _(CANL)	–3%	0%	3%	

(1) All typical values are at 25°C with a 5-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} Propagation delay time, low-to-high-level output	S at 0 V or V _{CC} , See Figure 6	4.75V < V _{CC} < 5.25V	60	100	ns
		4.5V < V _{CC} < 5.5V	60	135	
t _{PHL} Propagation delay time, high-to-low-level output		4.75V < V _{CC} < 5.25V	45	70	
		4.5V < V _{CC} < 5.5V	45	95	
t _r Output signal rise time			8		
t _f Output signal fall time			8		

S-PIN CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{IH} High level input current	S at 2 V	20	40	70	μA
I _{IL} Low level input current	S at 0.8 V	5	20	30	

VREF-PIN CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _O Reference output voltage	–50 μA < I _O < 50 μA	0.4 V _{CC}	0.5 V _{CC}	0.6 V _{CC}	V

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THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-Air	Low-K thermal resistance ⁽¹⁾		211		°C/W
		High-K thermal resistance		131		
θ_{JB}	Junction-to-Board Thermal Resistance			53		
θ_{JC}	Junction-to-Case Thermal Resistance			79		
P_D	Average power dissipation	$V_{CC} = 5.0\text{ V}$, $T_j = 27^\circ\text{C}$, $R_L = 60\ \Omega$, S at 0 V, Input to TXD a 500 kHz, 50% duty cycle square wave. CL at RXD = 15 pF		112		mW
		$V_{CC} = 5.5\text{ V}$, $T_j = 130^\circ\text{C}$, $R_L = 45\ \Omega$, S at 0 V, Input to TXD a 500 kHz, 50% duty cycle square wave. CL at RXD = 15 pF			170	
$T_{J_shutdown}$	Junction temperature, thermal shutdown ⁽²⁾			190		°C

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface-mount packages.

(2) Extended operation in thermal shutdown may affect device reliability, see APPLICATIONS INFORMATION.

FUNCTION TABLES

Table 2. DRIVER

INPUTS		OUTPUTS		BUS STATE
TXD ⁽¹⁾	S ⁽¹⁾	CANH ⁽¹⁾	CANL ⁽¹⁾	
L	L or Open	H	L	DOMINANT
H	X	Z	Z	RECESSIVE
Open	X	Z	Z	RECESSIVE
X	H	Z	Z	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

Table 3. RECEIVER

DIFFERENTIAL INPUTS $V_{ID} = V(\text{CANH}) - V(\text{CANL})$	OUTPUT RXD ⁽¹⁾	BUS STATE
$V_{ID} \geq 0.9\text{ V}$	L	DOMINANT
$0.5\text{ V} < V_{ID} < 0.9\text{ V}$	?	?
$V_{ID} \leq 0.5\text{ V}$	H	RECESSIVE
Open	H	RECESSIVE

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

PARAMETER MEASUREMENT INFORMATION

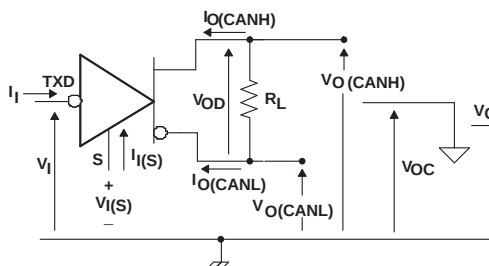


Figure 1. Driver Voltage, Current, and Test Definition

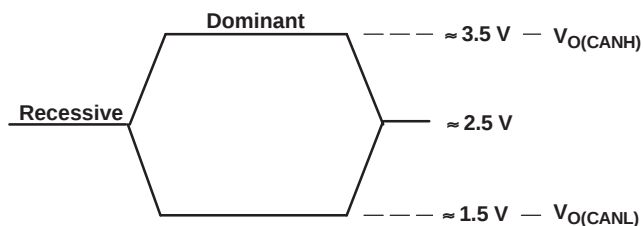


Figure 2. Bus Logic State Voltage Definitions

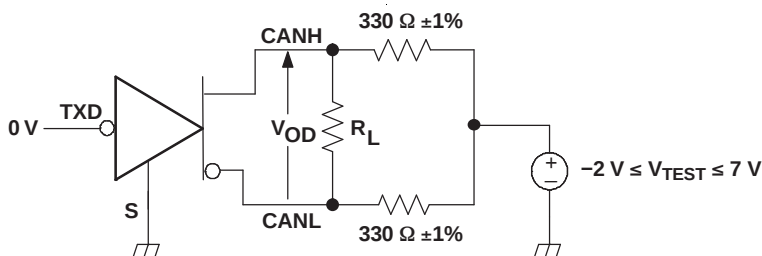


Figure 3. Driver V_{OD} Test Circuit

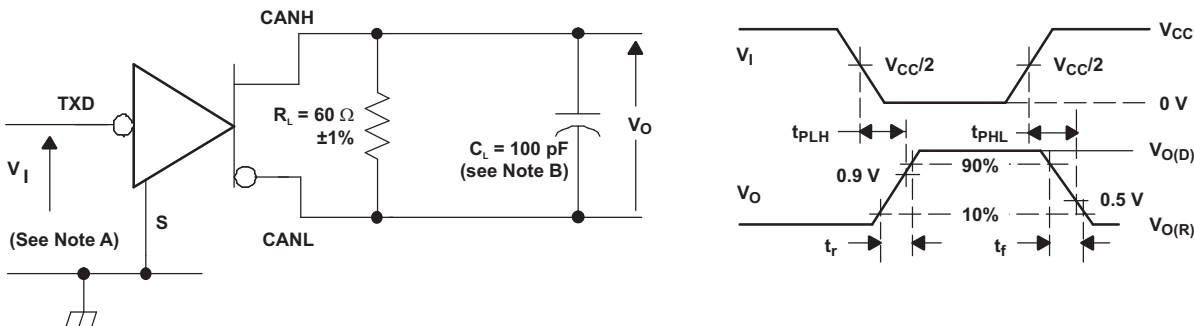


Figure 4. Driver Test Circuit and Voltage Waveforms

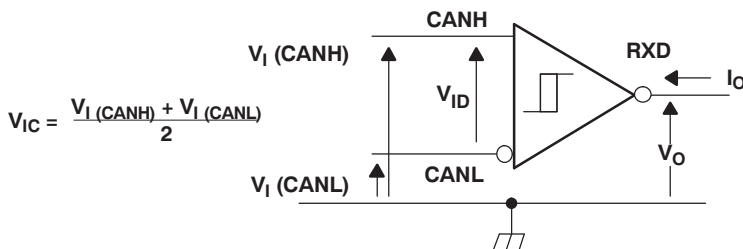
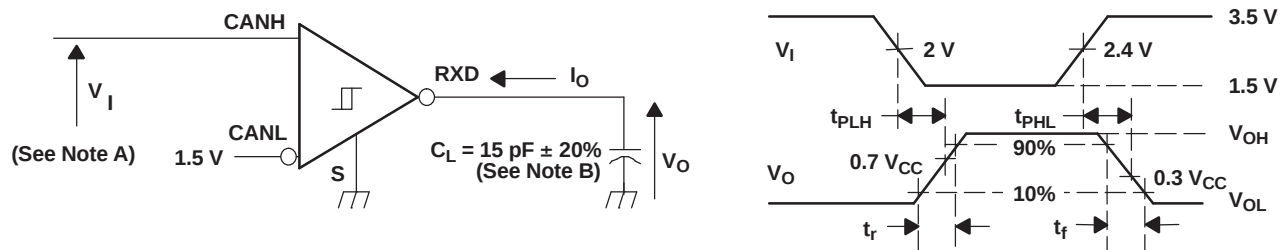


Figure 5. Receiver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

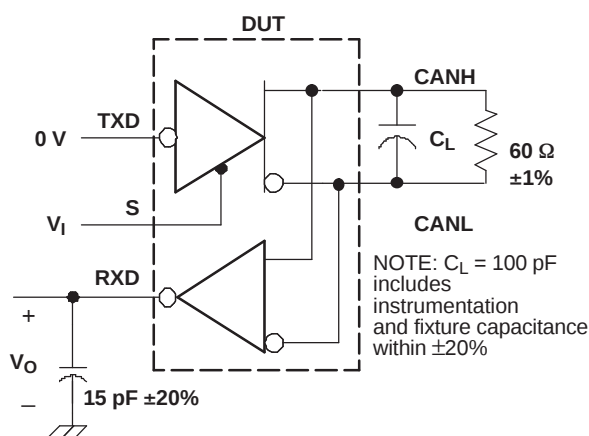


- The input pulse is supplied by a generator having the following characteristics: $PRR \leq 125$ kHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
- C_L includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 6. Receiver Test Circuit and Voltage Waveforms

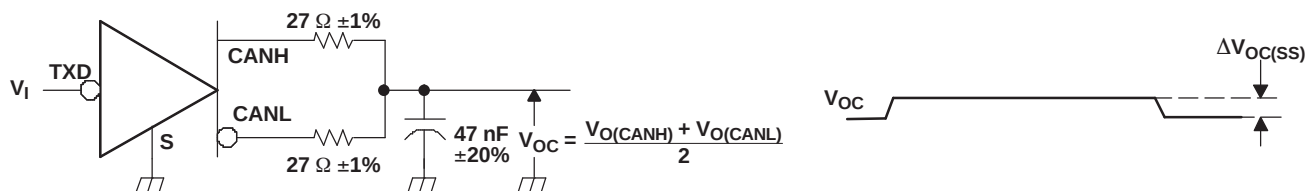
Table 4. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$ V_{ID} $	R	
-11.1 V	-12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
-6 V	-12 V	6 V	L	
12 V	6 V	6 V	L	
-11.5 V	-12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
-12 V	-6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	



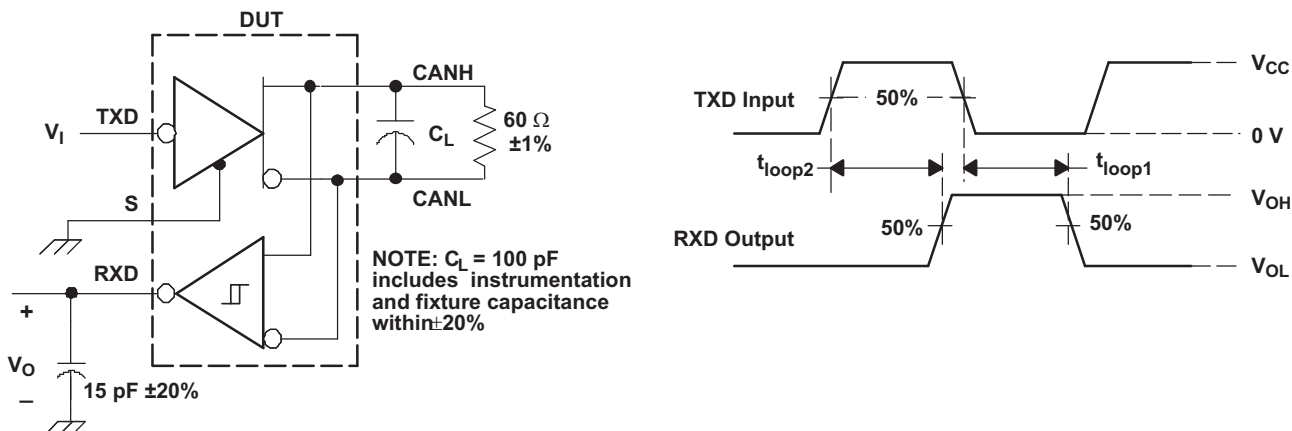
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, Pulse Repetition Rate (PRR) = 25 kHz, 50% duty cycle

Figure 7. t_{en} Test Circuit and Waveform



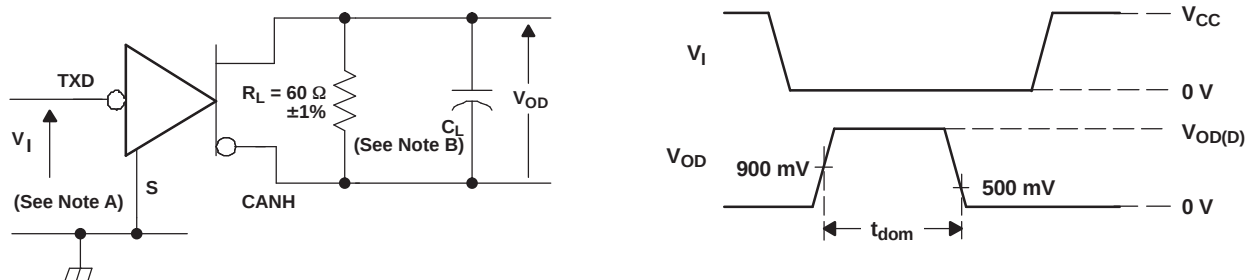
NOTE: All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 8. Common Mode Output Voltage Test and Waveforms



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 9. $t_{(LOOP)}$ Test Circuit and Waveform



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns. Pulse Repetition Rate (PRR) = 500 Hz, 50% duty cycle.

B. $C_L = 100$ pF includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 10. Dominant Time-Out Test Circuit and Waveforms

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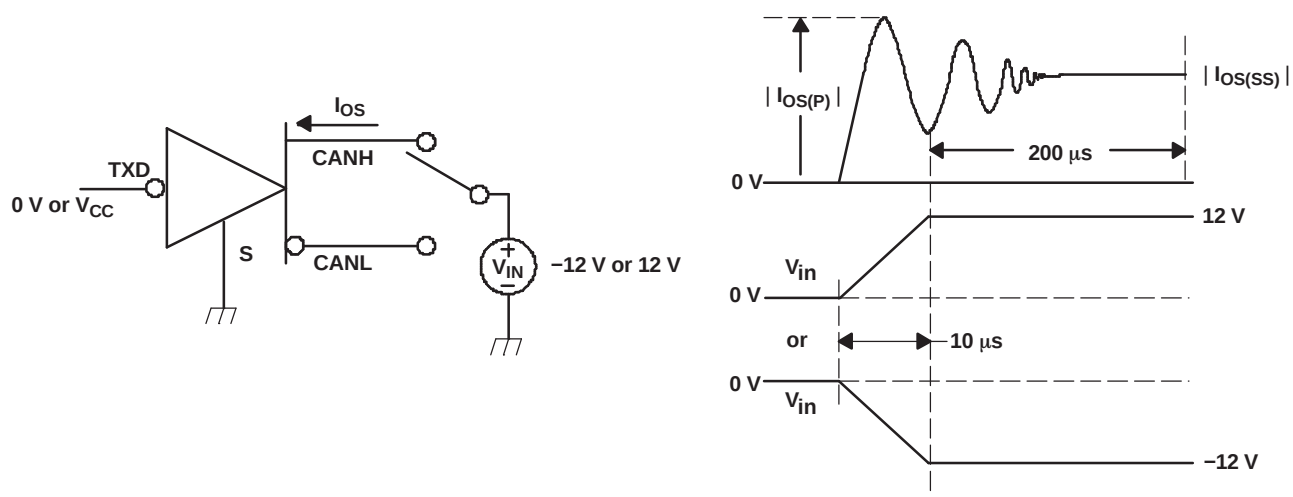


Figure 11. Driver Short-Circuit Current Test and Waveform

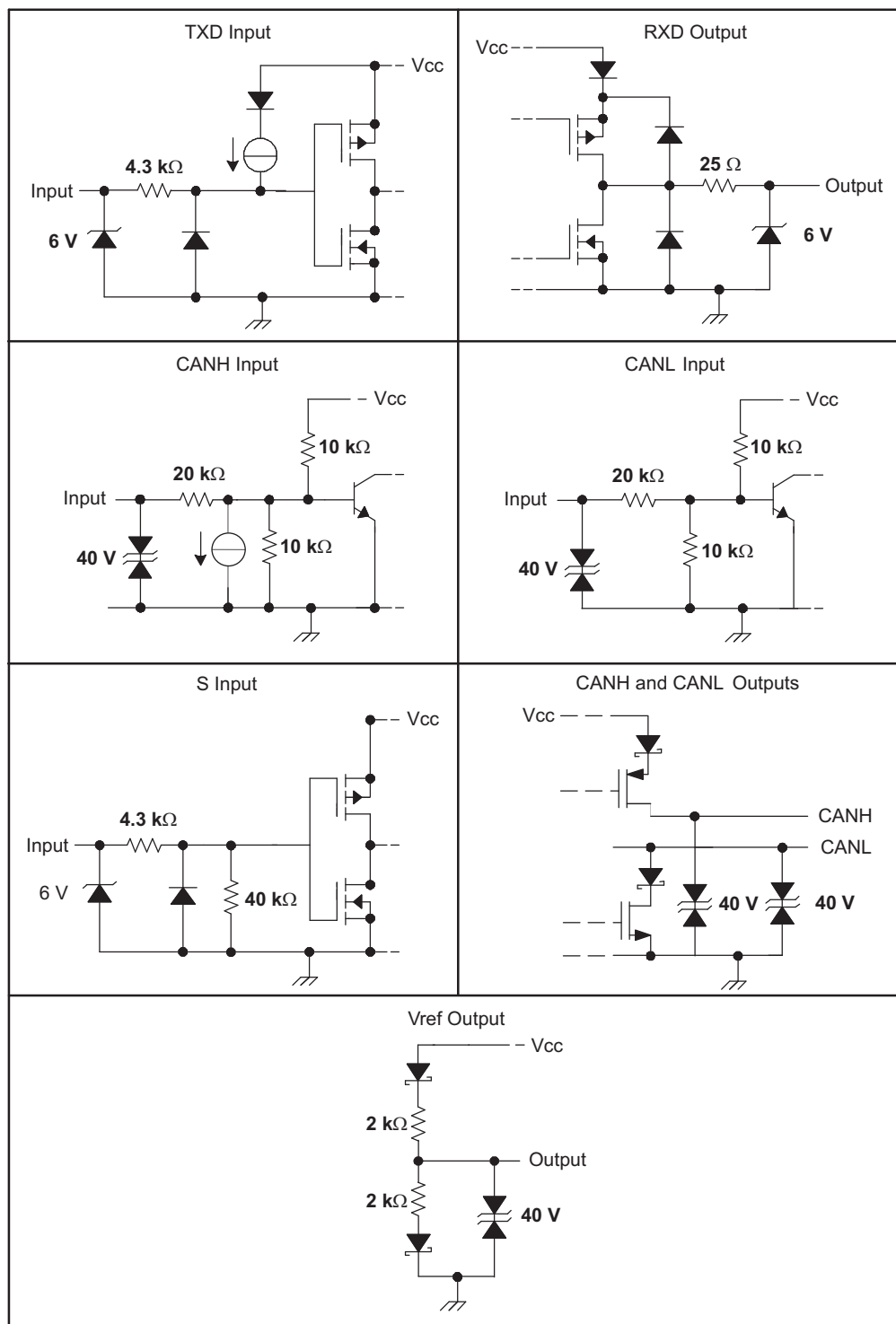
DEVICE INFORMATION

Table 5. Parametric Cross Reference With the TJA1050

TJA1050 ⁽¹⁾	PARAMETER	HVD1050
TRANSMITTER SECTION		
V _{IH}	High-level input voltage	Recommended V _{IH}
V _{IL}	Low-level input voltage	Recommended V _{IL}
I _{IH}	High-level input current	Driver I _{IH}
I _{IL}	Low-level input current	Driver I _{IL}
BUS SECTION		
I _{LI}	Power-off bus input current	Receiver I _{I(off)}
I _{O(SC)}	Short-circuit output current	Driver I _{OS(SS)}
V _{O(dom)}	Dominant output voltage	Driver V _{O(D)}
V _{I(dif)(th)}	Differential input voltage	Receiver V _{IT} and recommended V _{ID}
V _{I(dif)(hys)}	Differential input hysteresis	Receiver V _{hys}
V _{O(reces)}	Recessive output voltage	Driver V _{O(R)}
V _{O(dif)(bus)}	Differential bus voltage	Driver V _{OD(D)} and V _{OD(R)}
R _{I(cm)}	CANH, CANL input resistance	Receiver R _{IN}
R _{I(dif)}	Differential input resistance	Receiver R _{ID}
R _{I(cm) (m)}	Input resistance matching	Receiver R _{I (m)}
C _i	Input capacitance to ground	Receiver C _I
C _{i(dif)}	Differential input capacitance	Receiver C _{ID}
RECEIVER SECTION		
I _{OH}	High-level output current	Recommended I _{OH}
I _{OL}	Low-level output current	Recommended I _{OL}
Vref PIN SECTION		
V _{ref}	Reference output voltage	V _O
TIMING SECTION		
t _{d(TXD-BUSon)}	Delay TXD to bus active	Driver t _{PLH}
t _{d(TXD-BUSoff)}	Delay TXD to bus inactive	Driver t _{PHL}
t _{d(BUSon-RXD)}	Delay bus active to RXD	Receiver t _{PHL}
t _{d(BUSoff-RXD)}	Delay bus inactive to RXD	Receiver t _{PLH}
	t _{d(TXD-BUSon)} + t _{d(BUSon-RXD)}	Device t _{LOOP1}
	t _{d(TXD-BUSoff)} + t _{d(BUSoff-RXD)}	Device t _{LOOP2}
t _{dom(TXD)}	Dominant time out	Driver t _(dom)
S PIN SECTION		
V _{IH}	High-level input voltage	Recommended V _{IH}
V _{IL}	Low-level input voltage	Recommended V _{IL}
I _{IH}	High-level input current	I _{IH}
I _{IL}	Low-level input current	I _{IL}

(1) From TJA1050 Product Specification, Philips Semiconductors, 2002 May 16.

Equivalent Input and Output Schematic Diagrams



TYPICAL CHARACTERISTICS

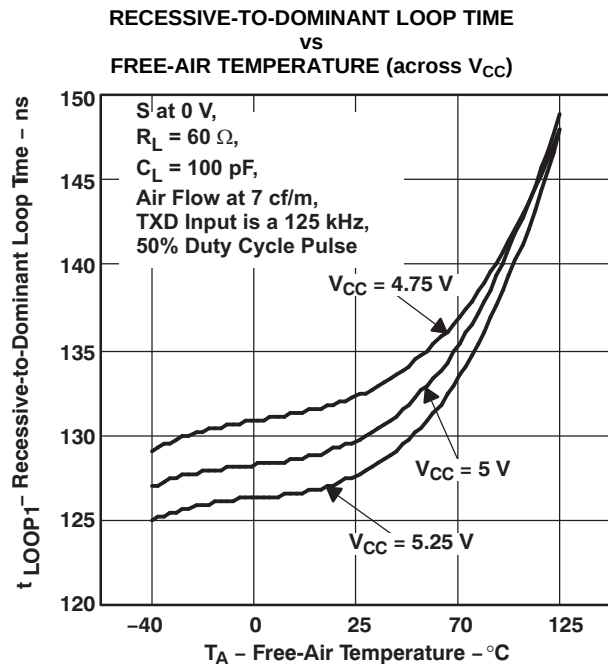


Figure 12.

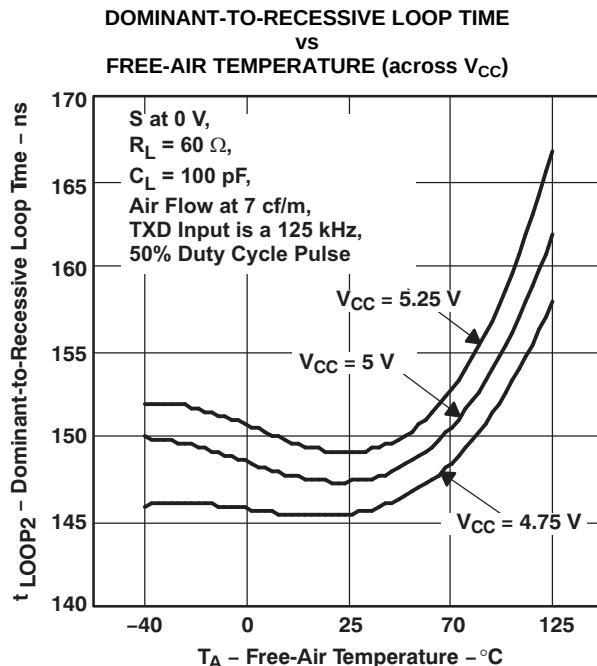


Figure 13.

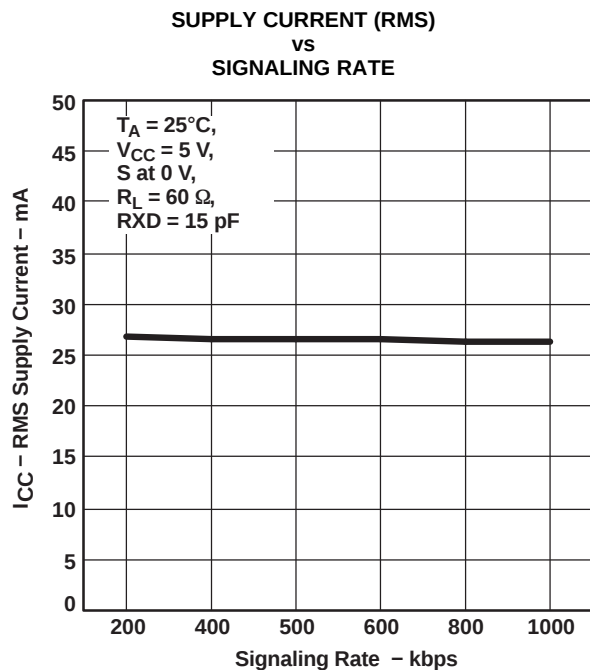


Figure 14.

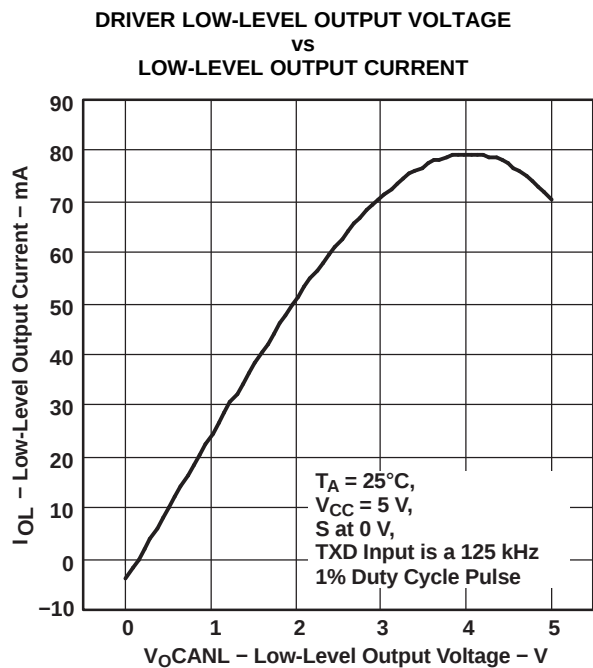
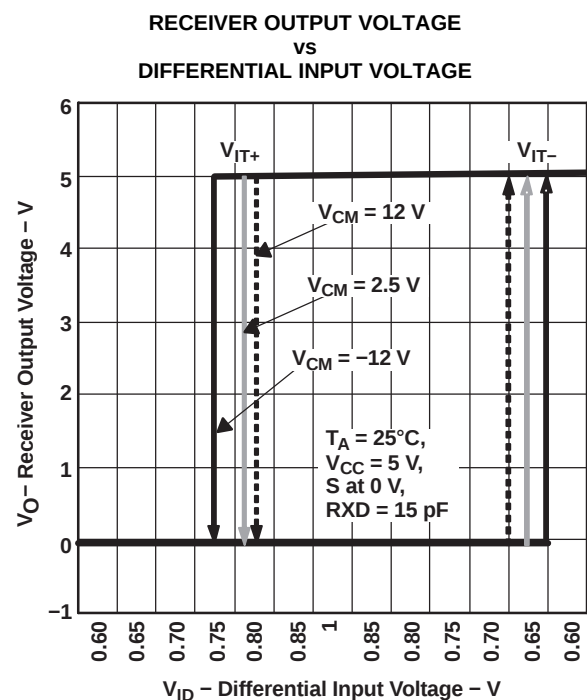
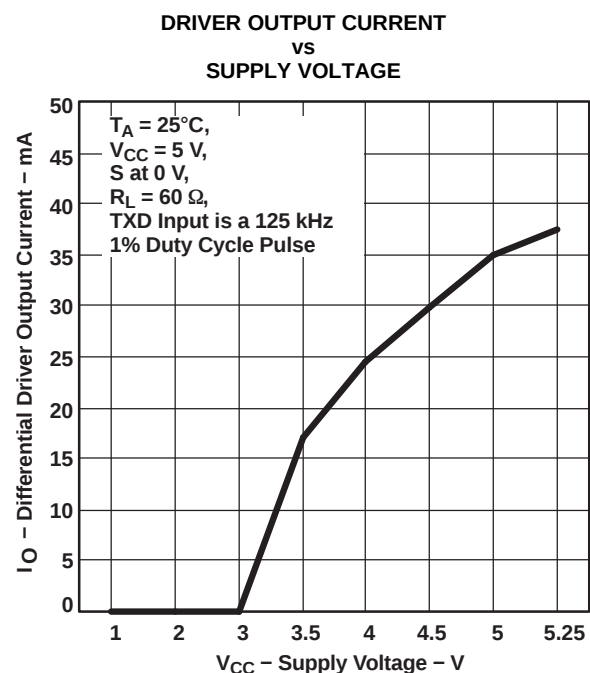
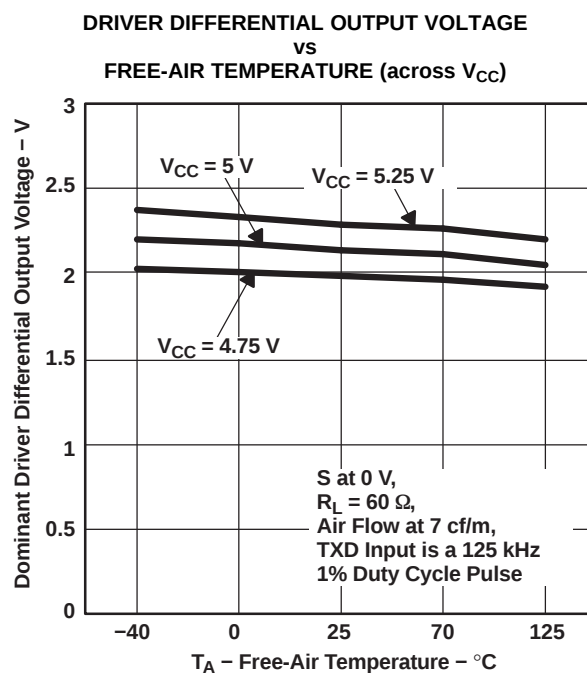
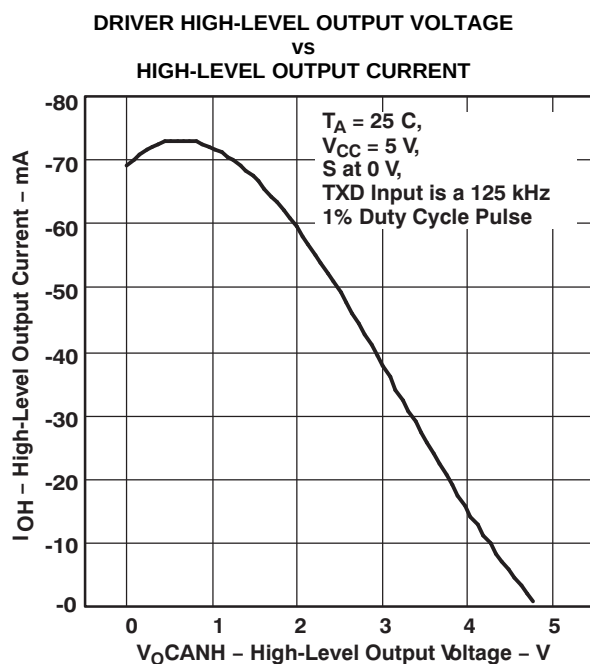


Figure 15.

TYPICAL CHARACTERISTICS (continued)



TYPICAL CHARACTERISTICS (continued)

**TYPICAL ELECTROMAGNETIC EMISSIONS
UP TO 50 MHz (Peak Amplitude)**

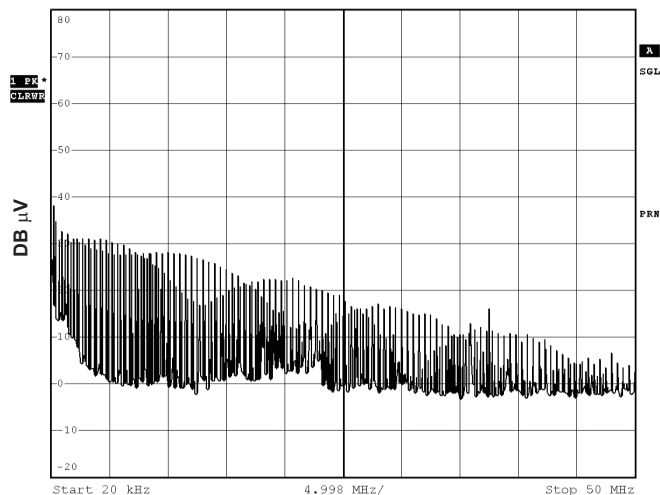


Figure 20. Frequency Spectrum of Common-Mode Emissions

**TYPICAL ELECTROMAGNETIC
IMMUNITY PERFORMANCE**

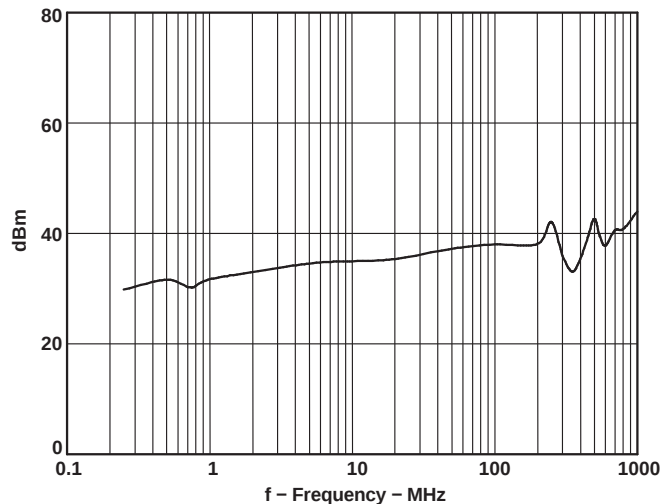


Figure 21. Direct Power Injection (DPI) Response vs Frequency

APPLICATION INFORMATION

Thermal Shutdown

The SN65HVD1050 has a thermal shutdown feature that turns off the driver outputs when the junction temperature nears 190°C. This shutdown prevents catastrophic failure from bus shorts, but does not protect the circuit from possible damage. The user should strive to maintain recommended operating conditions and not exceed absolute-maximum ratings at all times. If an SN65HVD1050 is subjected to many, or long-duration faults that can put the device into thermal shutdown, it should be replaced.

Bus Loading

Q: *How many HVD1050 nodes can be connected on a bus?*

A: In the CAN standard ISO 11898-2 the driver differential output is specified with a 60Ω load (must be greater than 1.5V) and with a fully-loaded bus (must be greater than 1.2V). The HVD1050 is specified to meet the 1.5V requirement with a 60Ω load, and 1.4V with a 45Ω load. The differential input resistance of the HVD1050 is a minimum of 30kΩ. If 167 transceivers are in parallel on a bus, this is equivalent to a 180Ω differential load. That transceiver load of 180Ω in parallel with the 60Ω (two 120Ω termination resistors) gives a total 45Ω. Therefore, the HVD1050 supports over 167 transceivers on a single bus segment, with margin to the 1.2V CAN requirement.

Dominant Time-Out Feature

A dominant-time-out circuit in the SN65HVD1050 prevents the driver from blocking network communication in the event of a hardware or software failure of the local CAN controller. The time-out circuit is triggered by a falling edge on TXD (pin 1). If no rising edge is seen before the time-out constant of the circuit expires, the driver is disabled. The circuit is then reset by the next rising edge on TXD. This feature prevents a faulty local CAN controller from corrupting the entire network with a “stuck” dominant state. The dominant time-out timer is selected to pass all normal CAN messages; however, non-standard applications may inadvertently trigger the dominant time-out if long strings of dominant bits are attempted at slow data rates.

REVISION HISTORY

Changes from Revision A (May 2007) to Revision B	Page
Deleted sentence, "The device is also qualified for use in ISO 11898-2 automotive applications in accordance with AEC-Q100." and footnote, "The device is available with Q100 qualification as the SN65HVD1050Q."	1
Changed V_{CC} min/max range from 4.75-5.25V to 4.5-5.5V	3
Changed V_{IH} max from 5.25V to 5.5V	3
Added rows for various parameters showing parameters with $V_{CC} \pm 5\%$ and $\pm 10\%$	3
Added Signaling Rate spec, min 20kbps	3
Changed V_{IH} min from 2 to 2.1V	3
Changed Bus output voltage (Dominant) CANH $4.5V < V_{CC} < 5.5V$ from 4.75 to 5.2	4
Added Bus Loading application discussion.	16
Added Dominant Time-Out Feature discussion.	16

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65HVD1050D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1050DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1050DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD1050DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN65HVD1050 :

- Automotive: [SN65HVD1050-Q1](#)
- Enhanced Product: [SN65HVD1050-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1050DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD1050DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1050DR	SOIC	D	8	2500	346.0	346.0	29.0
SN65HVD1050DR	SOIC	D	8	2500	346.0	346.0	29.0

D (R-PDSO-G8)

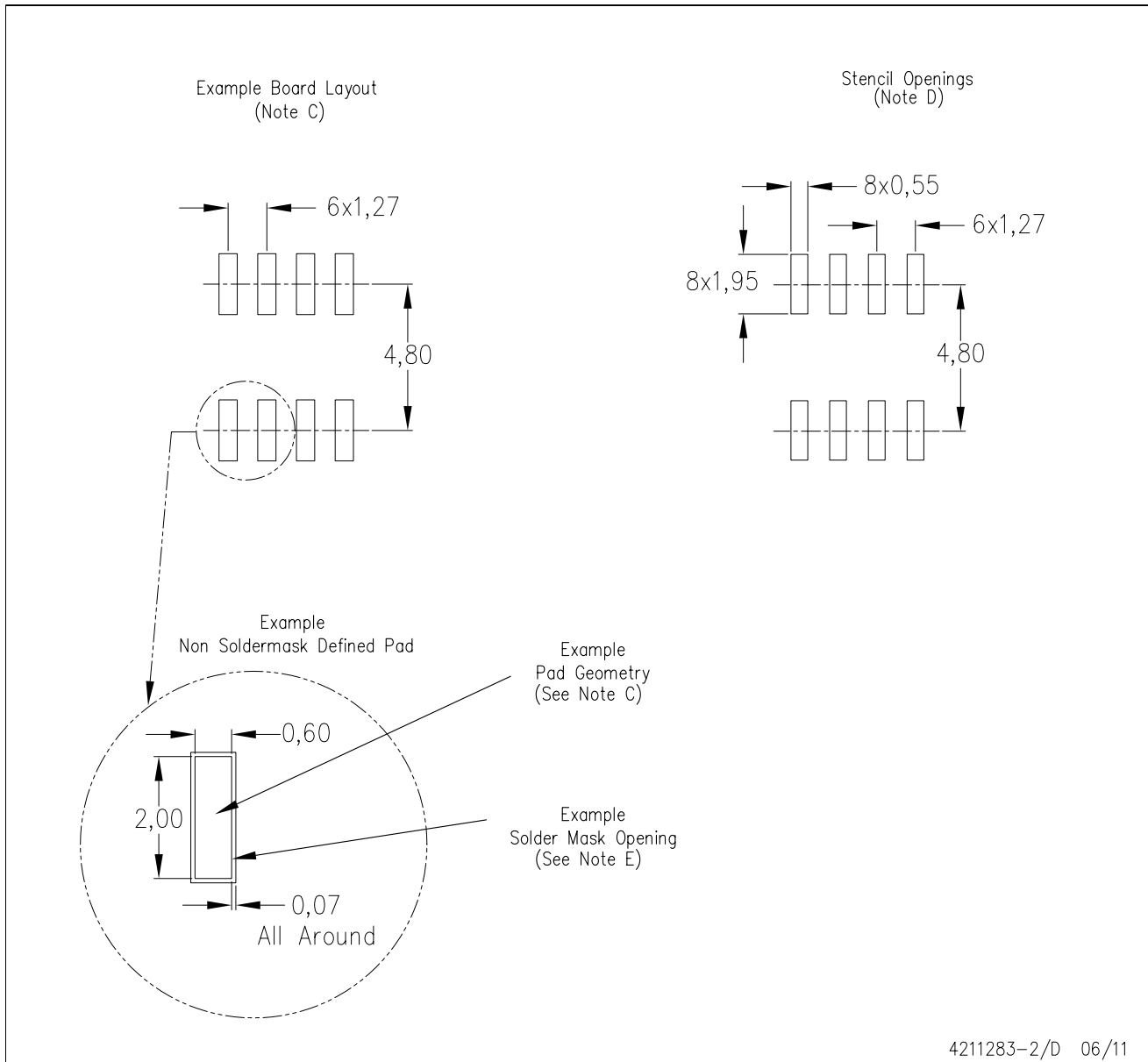
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/D 06/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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