



## STS4DNF60L

N-channel 60V - 0.045Ω - 4A - SO-8  
STripFET™ Power MOSFET

### General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STS4DNF60L	60V	<0.055Ω	4A

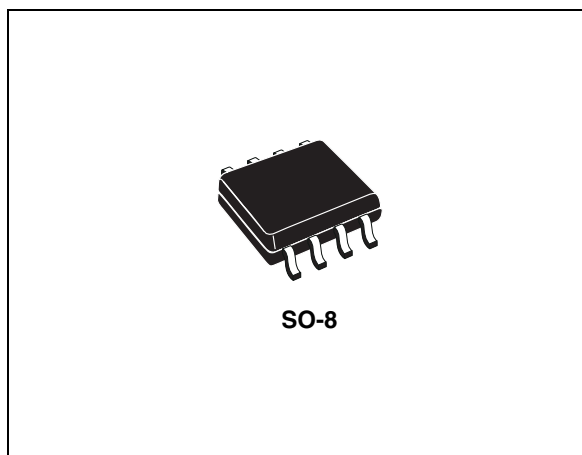
- Standard outline for easy automated surface mount assembly
- Low threshold drive

### Description

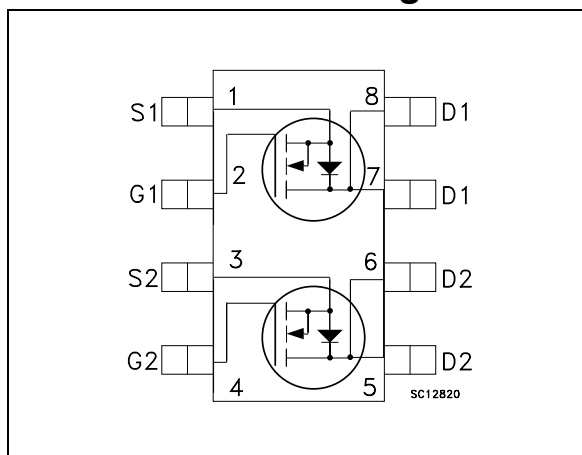
This Power MOSFET is the latest development of STMicroelectronics unique “Single Feature Size™” strip-based process. The resulting transistor shows extremely high packing density, low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

### Application

- Switching application



### Internal schematic diagram



### Order codes

Part number	Marking	Package	Packaging
STS4DNF60L	S4DNF60L	SO-8	Tape & reel

## Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	60	V
$V_{GS}$	Gate- source voltage	$\pm 15$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	4	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	2.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	16	A
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25^\circ\text{C}$	2	W
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

2.  $P_{tot}=1.6\text{W}$  for Single Operation

**Table 2. Thermal data**

$R_{thj-pcb}$	Thermal resistance junction-pcb D.O. <sup>(1)</sup>	62.5	$^\circ\text{C}/\text{W}$
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1. When mounted on inch<sup>2</sup> FR-4 board, 2 Oz Cu,  $t \leq 10\text{sec}$ , dual operation

## 2 Electrical characteristics

(T<sub>case</sub> = 25°C unless otherwise specified)

**Table 3. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 250μA, V <sub>GS</sub> = 0	60			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating V <sub>DS</sub> = Max rating, T <sub>C</sub> = 125°C			1 10	μA μA
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 15V			± 100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1	1.7	2.5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 2A V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 2A		0.045 0.050	0.055 0.065	Ω Ω

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub>	Forward transconductance	V <sub>DS</sub> = 25V, I <sub>D</sub> = 2A		25		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0		1030 140 40		pF pF pF
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	V <sub>DD</sub> = 48V, I <sub>D</sub> = 4A, V <sub>GS</sub> = 4.5V (see <a href="#">Figure 12</a> )		15 4 4		nC nC nC

**Table 5. Switching times**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD} = 30V$ , $I_D = 2.2A$ , $R_G = 4.7\Omega$ , $V_{GS} = 10V$ (see <a href="#">Figure 11</a> )		15 28		ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time	$V_{DD} = 30V$ , $I_D = 2.2A$ , $R_G = 4.7\Omega$ , $V_{GS} = 10V$ (see <a href="#">Figure 11</a> )		45 10		ns ns

**Table 6. Source drain diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				16	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4A$ , $V_{GS} = 0$			1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 4A$ , $di/dt = 100A/\mu s$		85		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 20V$ , $T_j = 25^\circ C$		85		nC
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 16</a> )		2		A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

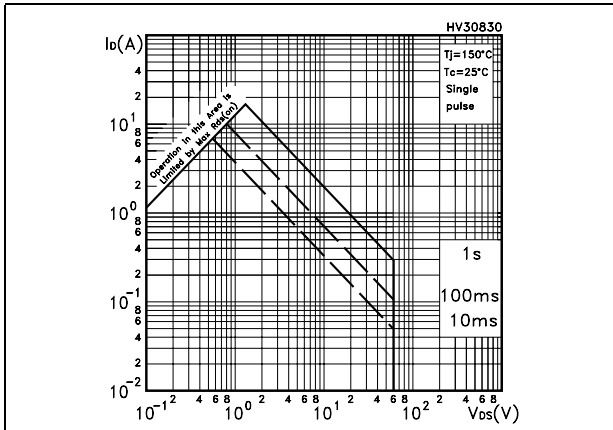


Figure 2. Thermal impedance

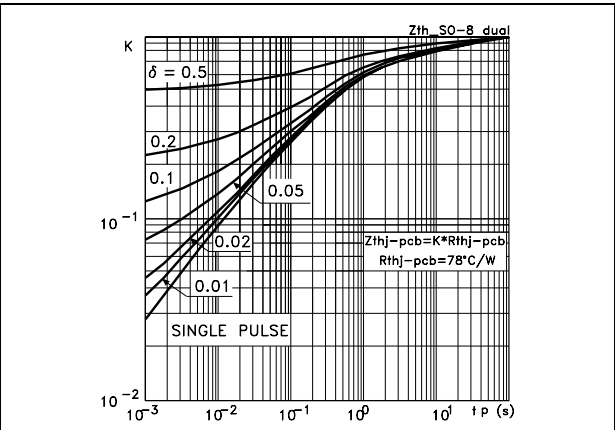


Figure 3. Output characteristics

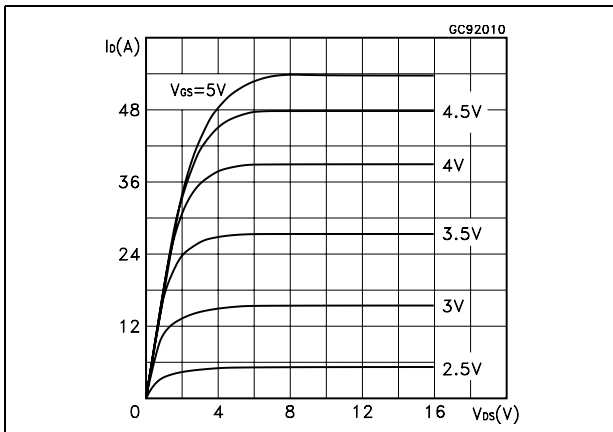


Figure 4. Transfer characteristics

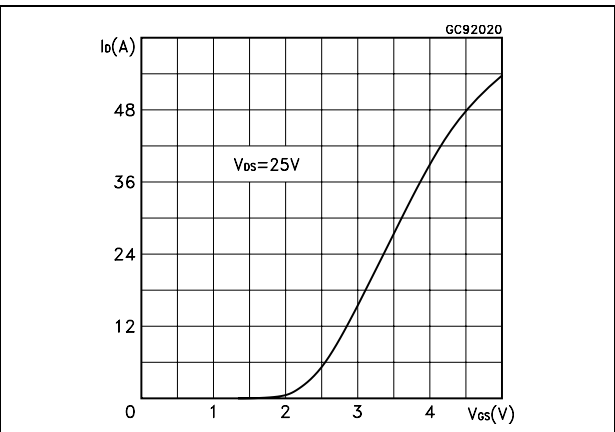


Figure 5. Source-drain diode forward characteristics

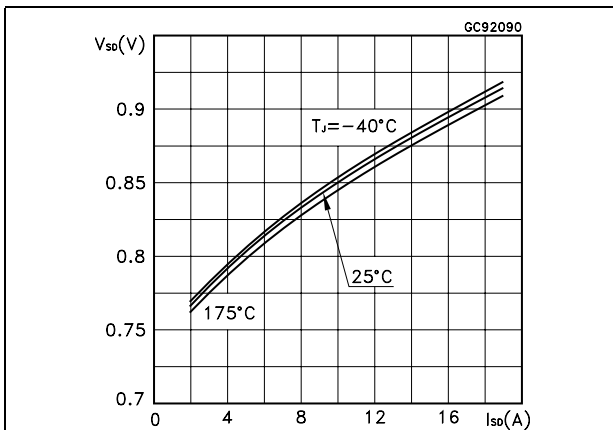


Figure 6. Static drain-source on resistance

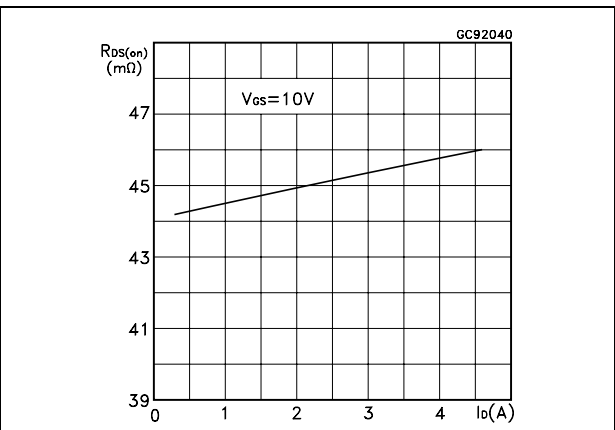


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

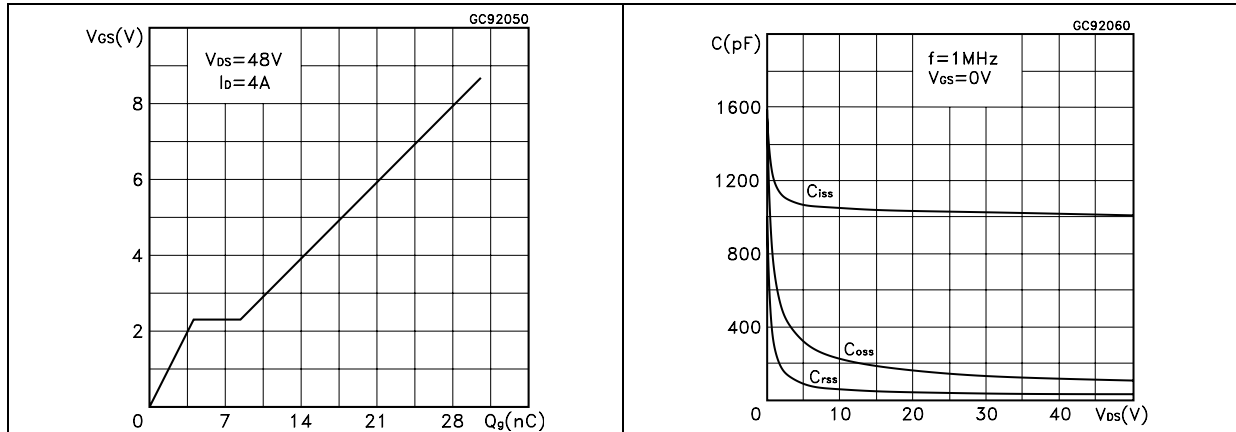
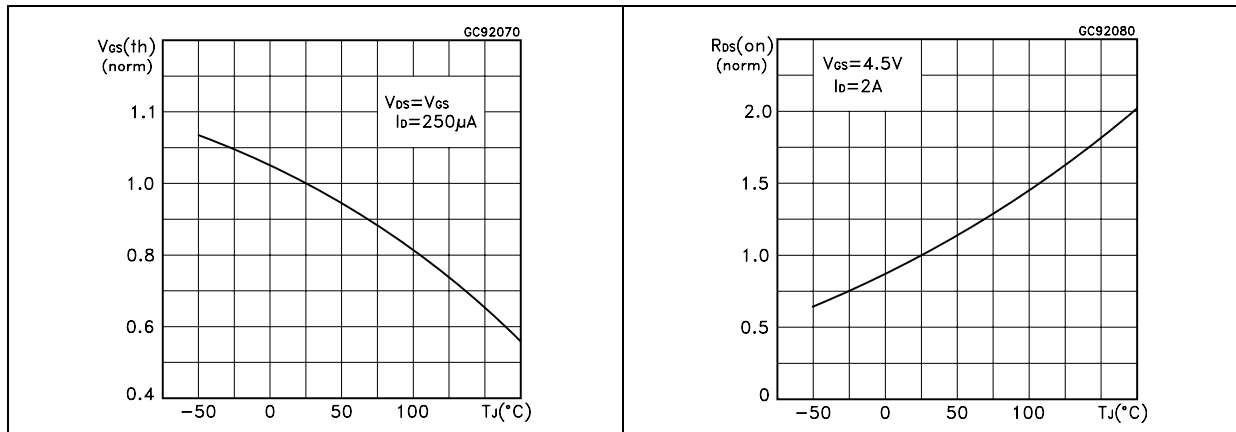


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature



### 3 Test circuits

Figure 11. Switching times test circuit for resistive load

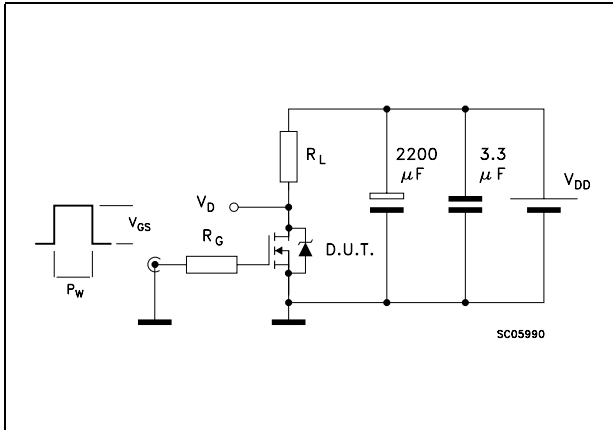


Figure 12. Gate charge test circuit

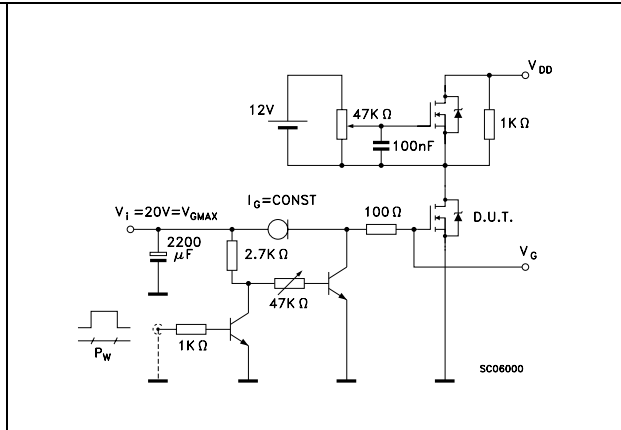


Figure 13. Test circuit for inductive load switching and diode recovery times

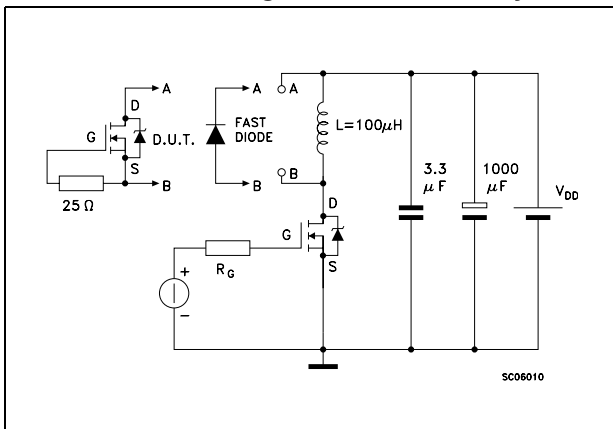


Figure 14. Unclamped Inductive load test circuit

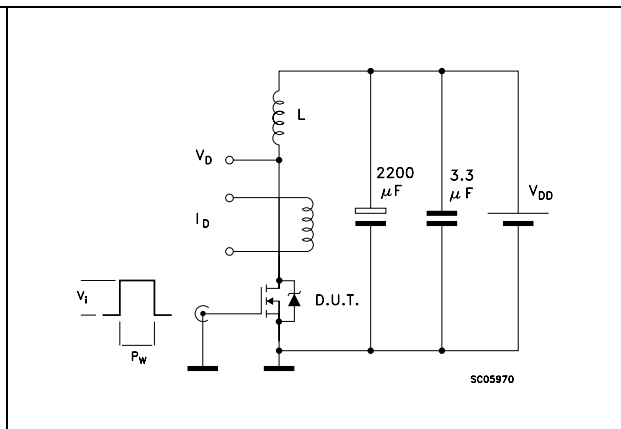


Figure 15. Unclamped inductive waveform

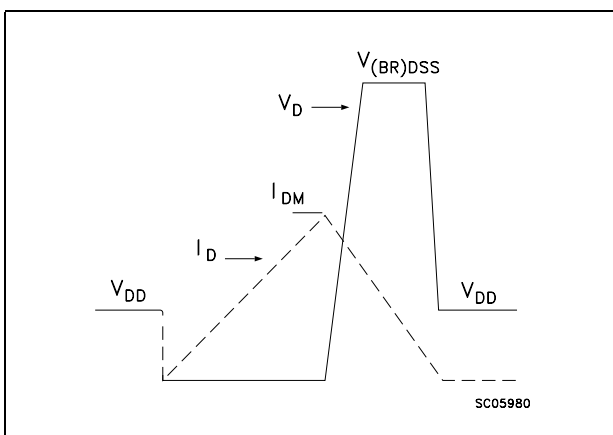
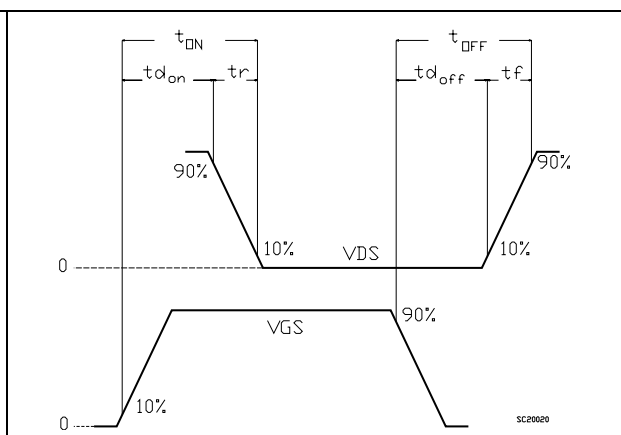


Figure 16. Switching time waveform

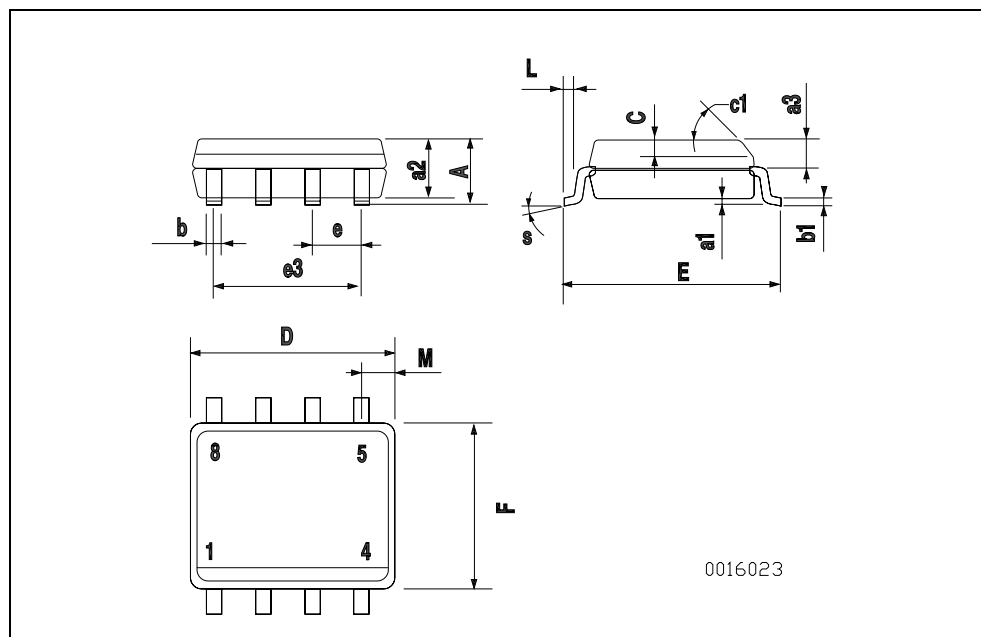


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**SO-8 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



## 5 Revision history

Table 7.

Date	Revision	Changes
30-May-2005	5	New format
29-Mar-2006	6	Modified <a href="#">Figure 1</a> and <a href="#">Figure 2</a>
16-May-2006	7	Modified internal schematic diagram

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