



## STS2DNF30L

Dual N-channel 30V - 0.09Ω - 3A SO-8  
STripFET™ Power MOSFET

### General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STS2DNF30L	30V	<0.011Ω	3A

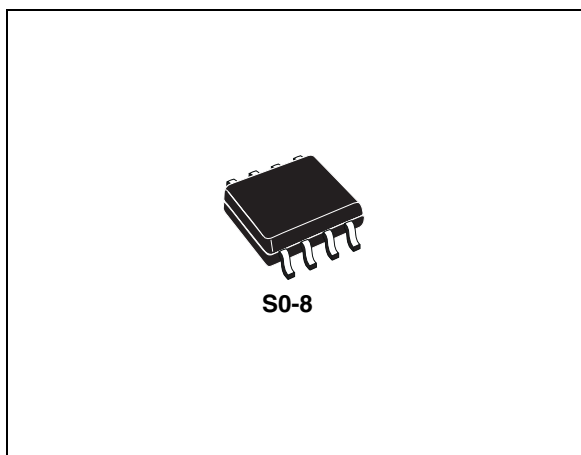
- Standard outline for easy automated surface mount assembly
- Low threshold gate drive

### Description

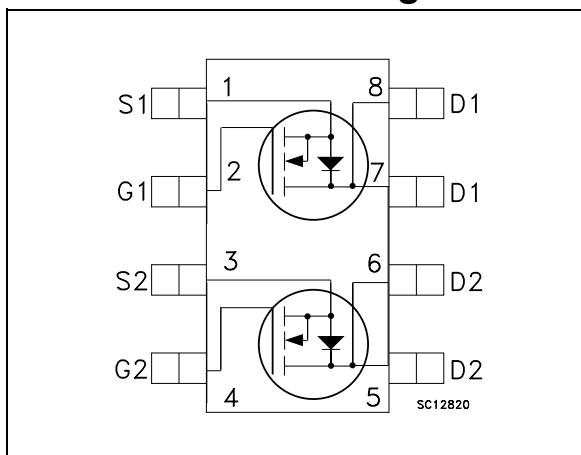
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

### Applications

- Switching application



### Internal schematic diagram



### Order codes

Part number	Marking	Package	Packaging
STS2DNF30L	S2DNF30L	SO-8	Tape & reel

# Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $v_{GS} = 0$ )	30	V
$V_{GS}$	Gate- source voltage	$\pm 18$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	3	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	1.9	A
$I_{DM}^{(1)}$	Drain current (pulsed)	9	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$ dual operation	1.6	W
	Total dissipation at $T_C = 25^\circ\text{C}$ single operation	2	W
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

**Table 2. Thermal data**

$R_{thj-a}$	Thermal resistance junction-ambient Max single operation	62.5	$^\circ\text{C}/\text{W}$
	Thermal resistance junction-ambient Max dual operation	78	$^\circ\text{C}/\text{W}$
$T_J$	Maximum operating junction ambient	150	$^\circ\text{C}$
$T_{stg}$	Storage temperature	-55 to 175	$^\circ\text{C}$

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	30			V
$I_{DSS}$	Zero gate voltage	$V_{DS} = \text{Max rating}$			1	$\mu A$
	Drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating},$ $T_C = 125^{\circ}C$			10	$\mu A$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 18V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 1A$		0.09	0.011	$\Omega$
		$V_{GS} = 5V, I_D = 1A$		0.13	0.15	$\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 2.5A$		2.5		S
$C_{iss}$	Input capacitance	$V_{DS} = 25V, f = 1 \text{ MHz},$ $V_{GS} = 0$		121		pF
$C_{oss}$	Output capacitance			45		pF
$C_{rss}$	Reverse transfer capacitance			11		pF
$Q_g$	Total gate charge	$V_{DD} = 24V, I_D = 2A,$ $V_{GS} = 10V$		4.5		nC
$Q_{gs}$	Gate-source charge			1.7		nC
$Q_{gd}$	Gate-drain charge			0.9		nC

1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 .

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time	$V_{DD} = 15V, I_D = 1A,$ $R_G = 4.7\Omega, V_{GS} = 4.5V$ (see Figure 12)		19		ns
	Rise time			20		ns
$t_{d(off)}$ $t_f$	Turn-off delay time	$V_{DD} = 15V, I_D = 1A,$ $R_G = 4.7\Omega, V_{GS} = 4.5V$ (see Figure 12)		12		ns
	Fall time			8		ns

**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				3	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				12	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2A, V_{GS} = 0$			1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 2A, V_{DD} = 30V$ $di/dt = 100A/\mu s,$ $T_j = 150^\circ C$ (see Figure 14)		19		ns
$Q_{rr}$	Reverse recovery charge			8.1		nC
$I_{RRM}$	Reverse recovery current			0.85		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

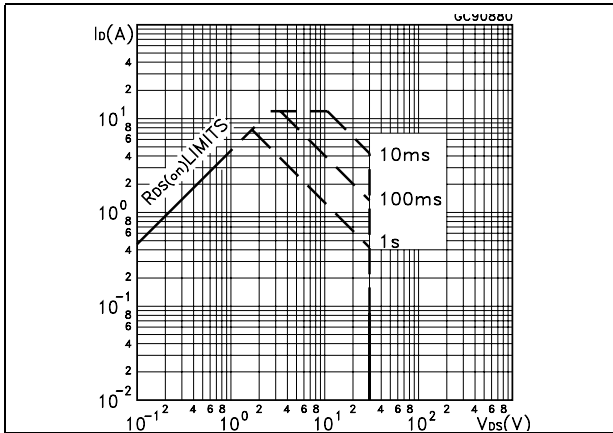


Figure 2. Thermal impedance

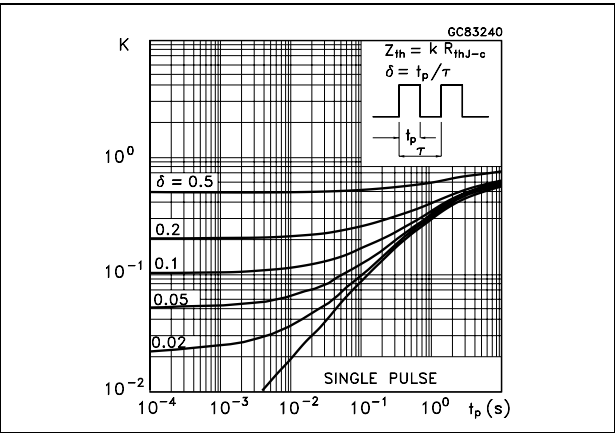


Figure 3. Output characteristics

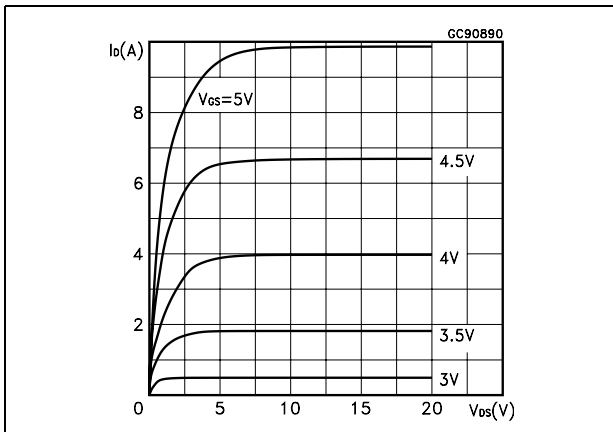


Figure 4. Transfer characteristics

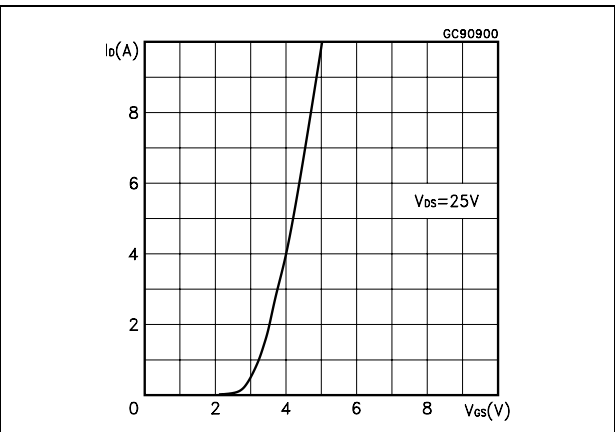


Figure 5. Transconductance

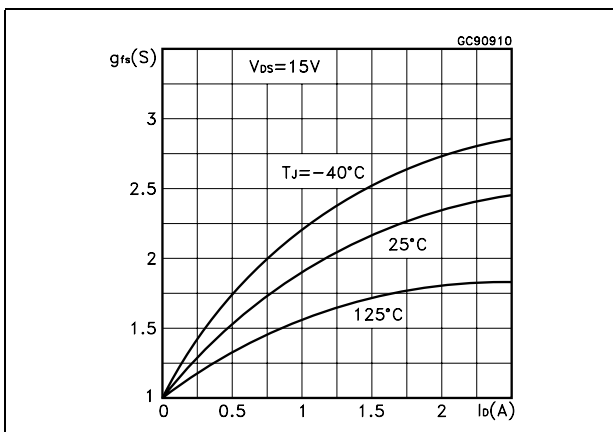


Figure 6. Static drain-source on resistance

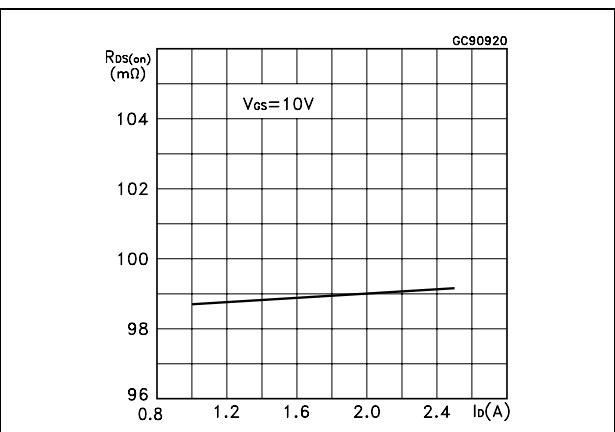


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

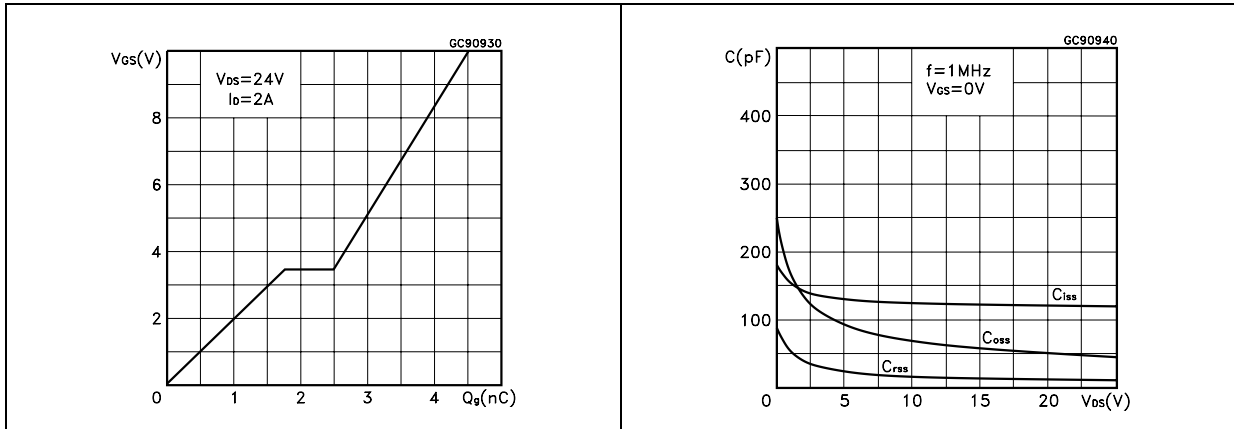


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

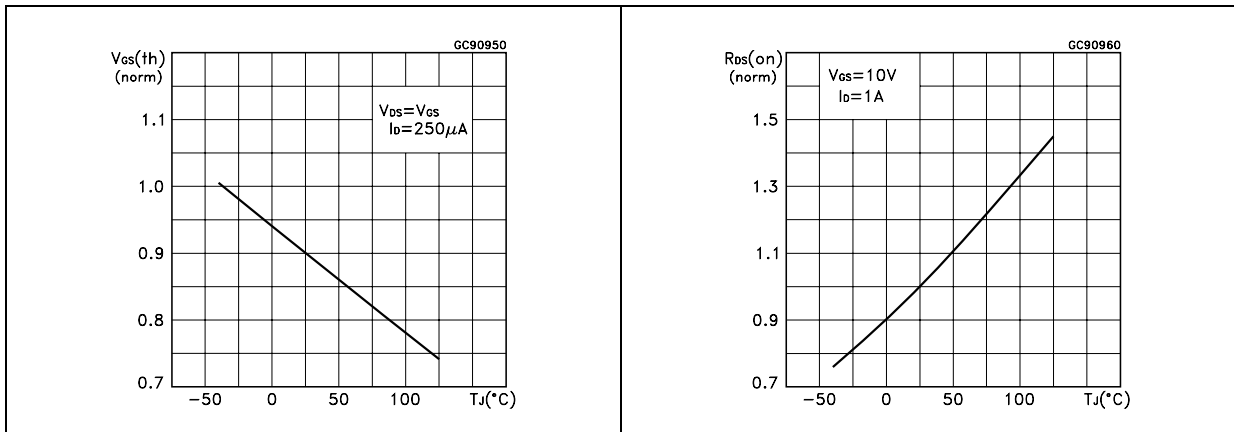
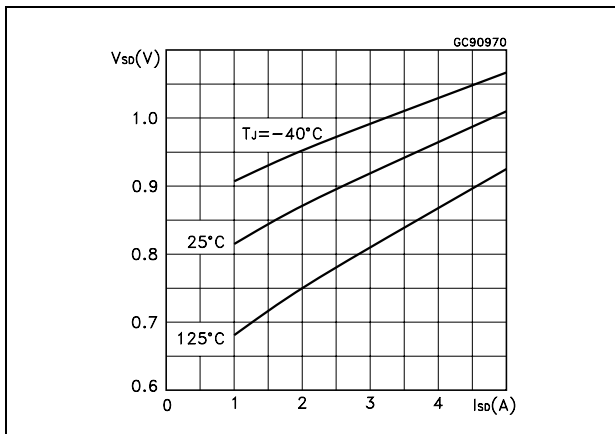


Figure 11. Source-drain diode forward characteristics



### 3 Test circuit

Figure 12. Switching times test circuit for resistive load

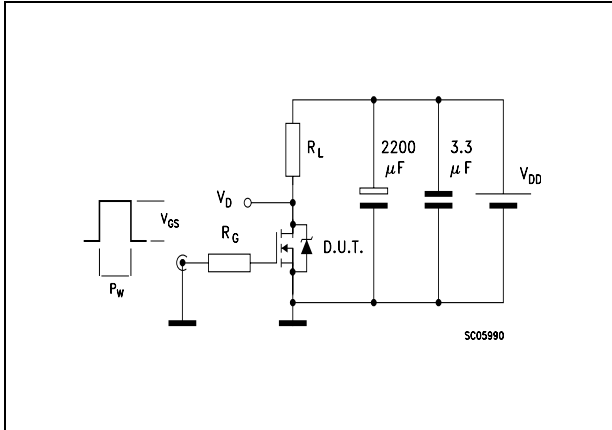


Figure 13. Gate charge test circuit

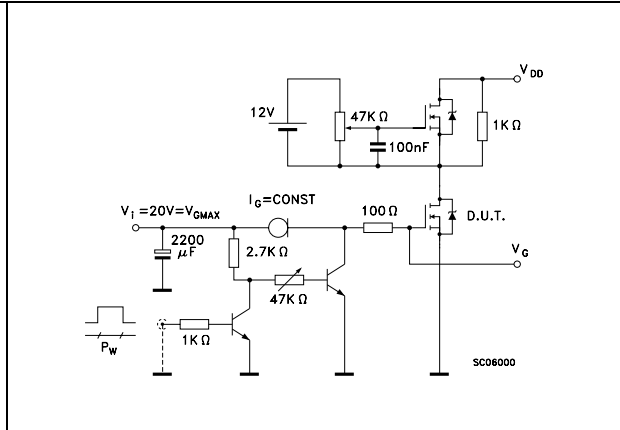


Figure 14. Test circuit for inductive load switching and diode recovery times

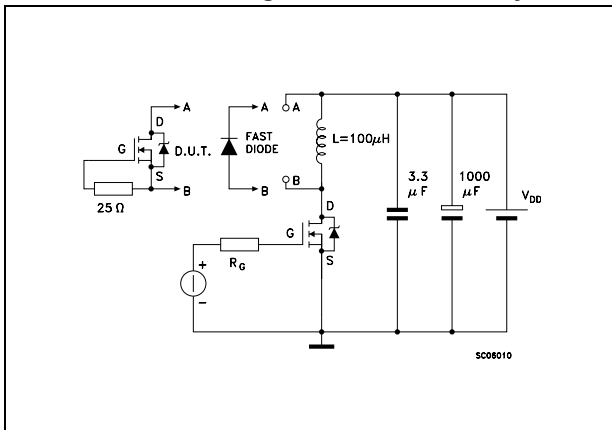


Figure 15. Unclamped Inductive load test circuit

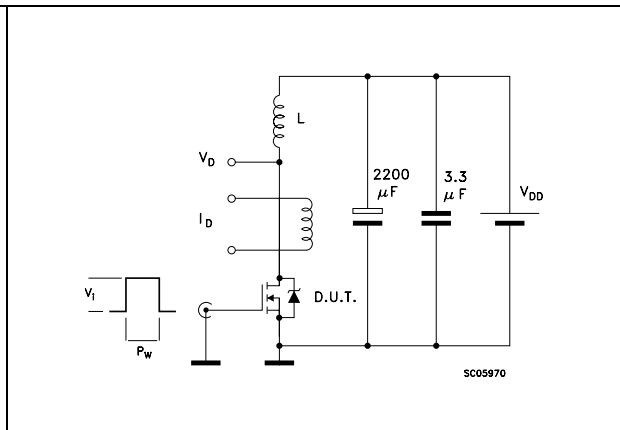


Figure 16. Unclamped inductive waveform

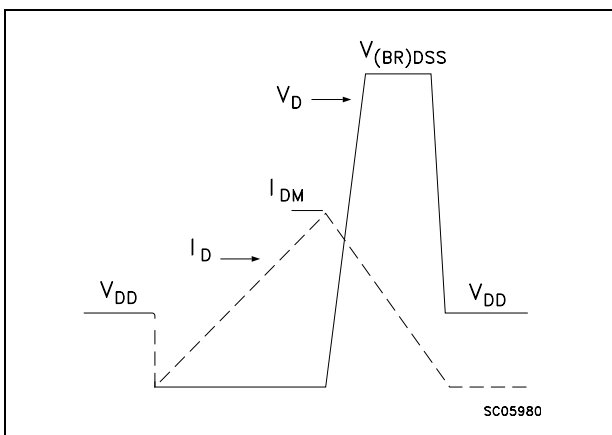
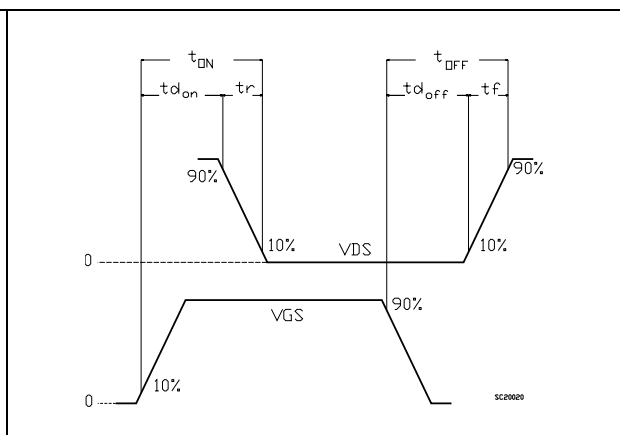


Figure 17. Switching time waveform

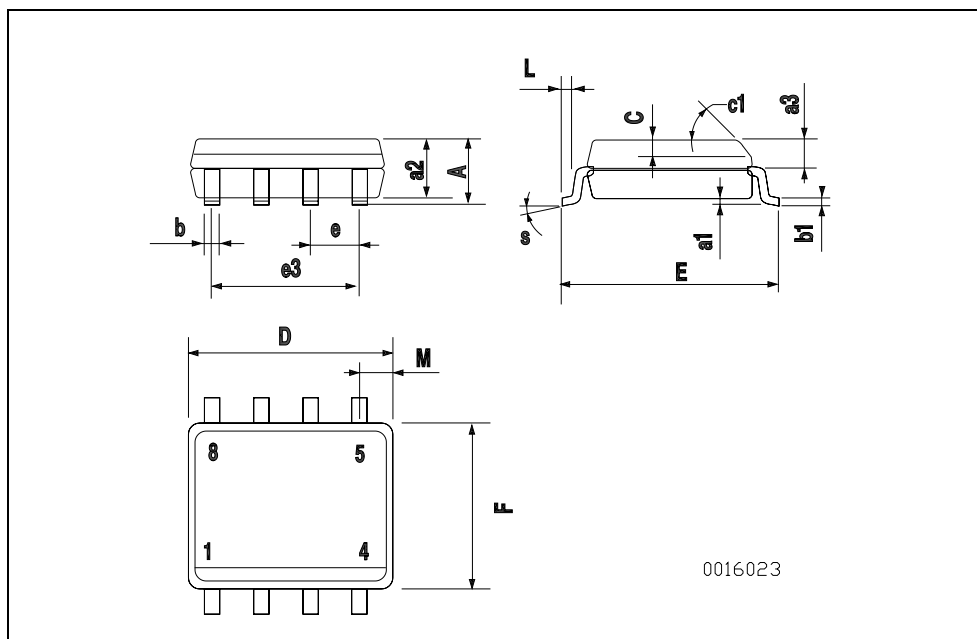


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : [www.st.com](http://www.st.com)

**SO-8 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



## 5 Revision history

Table 7. Revision history

Date	Revision	Changes
21-Jun-2004	3	Complete document
10-Nov-2006	4	The document has been reformatted

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