



STN5PF02V

P-channel 20V - 0.065Ω - 4.2A - SOT-223
2.5V - Drive STripFET™ II Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STN5PF02V	20V	<0.080Ω	4.2A

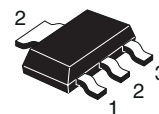
- Ultra low threshold gate drive (2.5V)
- Standard outline for easy automated surface mount assembly

Description

This Power MOSFET is the latest development of STMicroelectronics unique “single feature size™” strip-based process. The resulting transistor shows extremely extremely low on-resistance when driven at 2.5V.

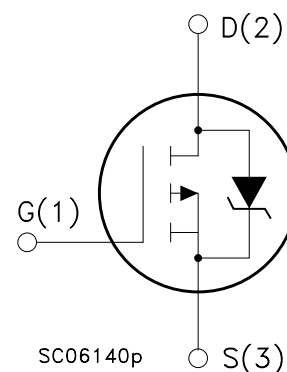
Applications

- Switching application



SOT-223

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STN5PF02V	N5PF02V	SOT-223	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	20	V
V_{GS}	Gate- source voltage	± 8	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	4.2	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	2.6	A
$I_{DM}^{(1)}$	Drain current (pulsed)	17	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	2.5	W
T_j T_{stg}	Max. operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

Note: For the p-channel Power MOSFET actual polarity of voltages and current has to be reversed

Table 2. Thermal resistance

Symbol	Parameter	Max value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pc board	50	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	90	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1inch² pad, 2oz Cu and $t_c < 10\text{sec}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0$	20			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating, @ } 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 8\text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	0.45			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 4.5\text{V}$, $I_D = 2.1\text{A}$ $V_{GS} = 2.5\text{V}$, $I_D = 2.1\text{A}$		0.065 0.085	0.080 0.10	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{V}$, $I_D = 2.5\text{A}$		6.6		S
C_{iss}	Input capacitance	$V_{DS} = 15\text{V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		412		pF
C_{oss}	Output capacitance			179		pF
C_{rss}	Reverse transfer capacitance			42.5		pF
Q_g	Total gate charge	$V_{DD} = 10\text{V}$, $I_D = 4.2\text{A}$, $V_{GS} = 2.5\text{V}$ (see Figure 13)		4.5	6	nC
Q_{gs}	Gate-source charge			0.73		nC
Q_{gd}	Gate-drain charge			1.75		nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

Table 5. Switching times

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 10V$, $I_D = 2.1A$ $R_G = 4.7\Omega$, $V_{GS} = 2.5V$ (see Figure 12)		11		ns
t_r	Rise time			47		ns
$t_{d(off)}$	Turn-off-delay time			38		ns
t_f	Fall time			20		ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				4.2	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				17	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4.2A$, $V_{GS} = 0$			1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 4.2A$, $di/dt=100A/\mu s$, $V_{DD} = 16V$, $T_j = 150^\circ C$ (see Figure 14)		32		ns
Q_{rr}	Reverse recovery charge			12.8		nC
I_{RRM}	Reverse recovery current			0.8		A

1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

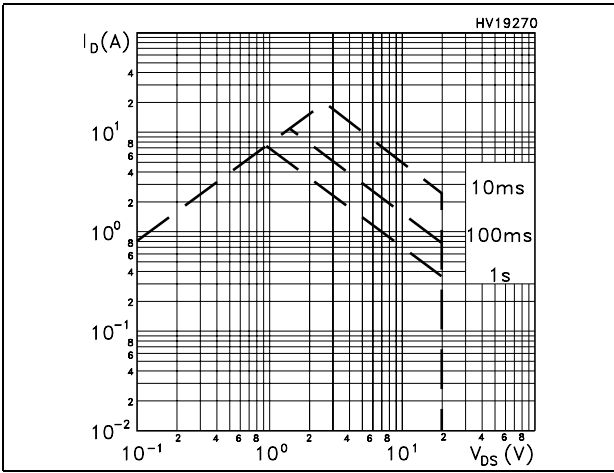


Figure 2. Thermal impedance

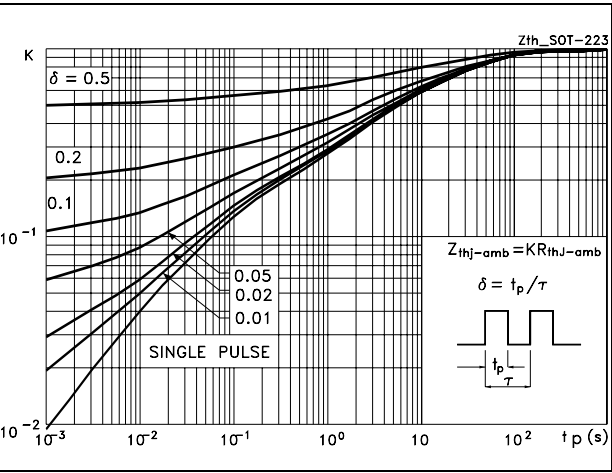


Figure 3. Output characteristics

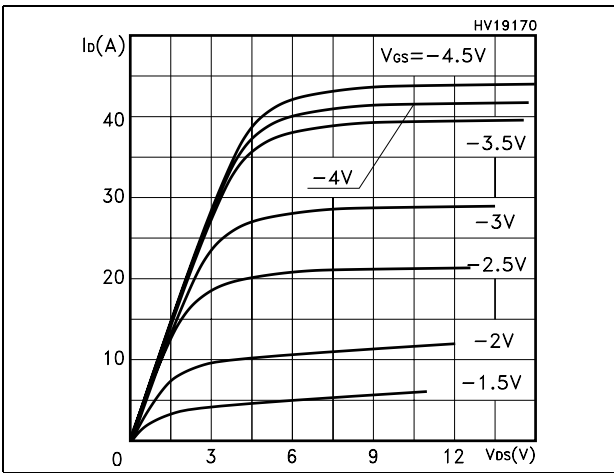


Figure 4. Transfer characteristics

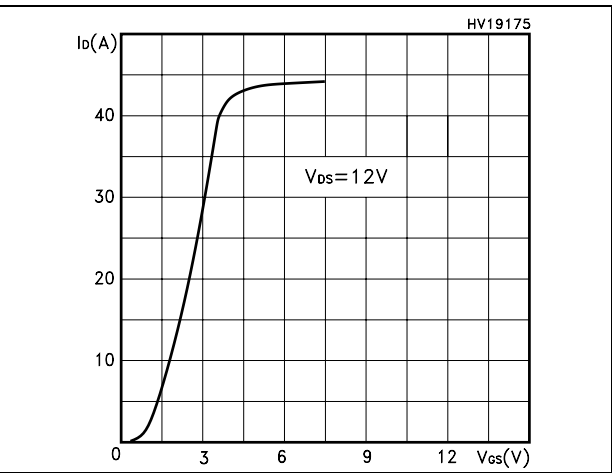


Figure 5. Transconductance

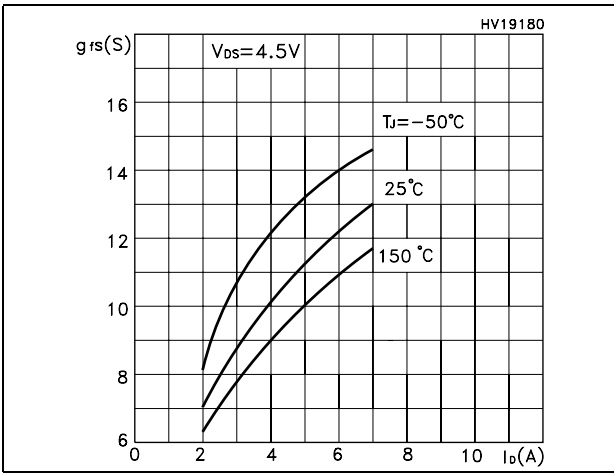


Figure 6. Static drain-source on resistance

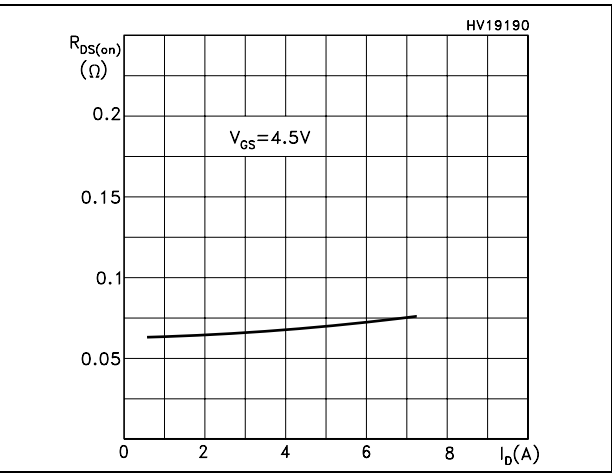


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

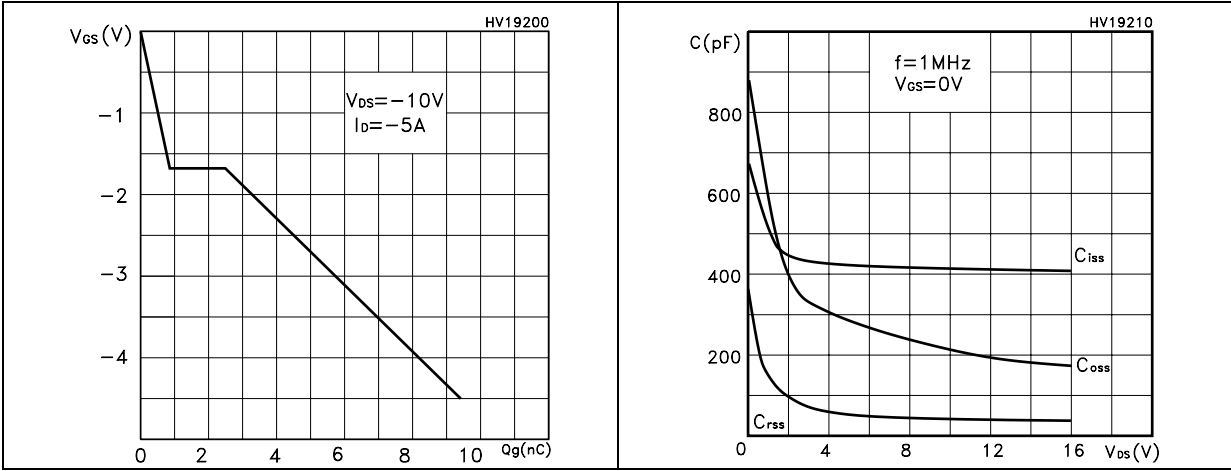


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

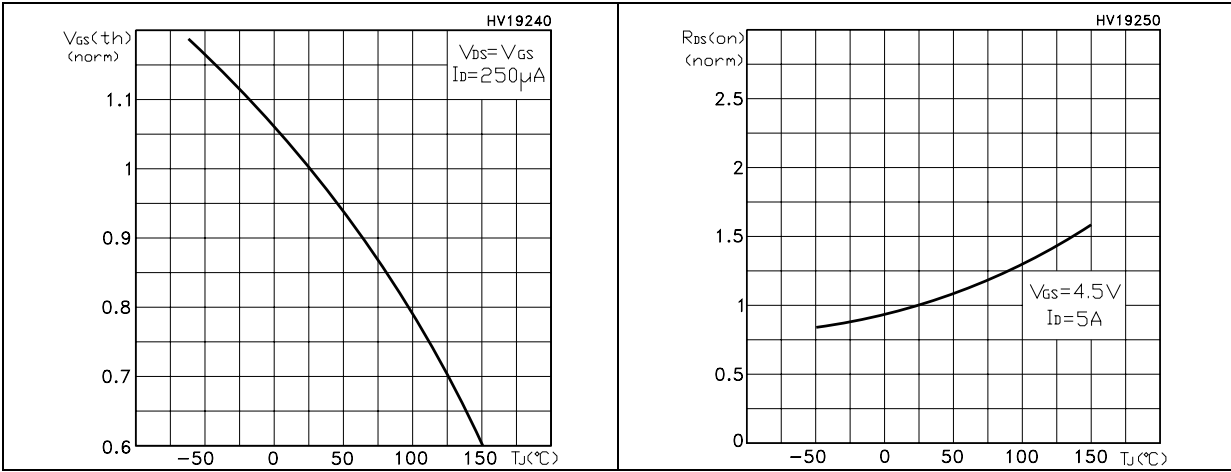
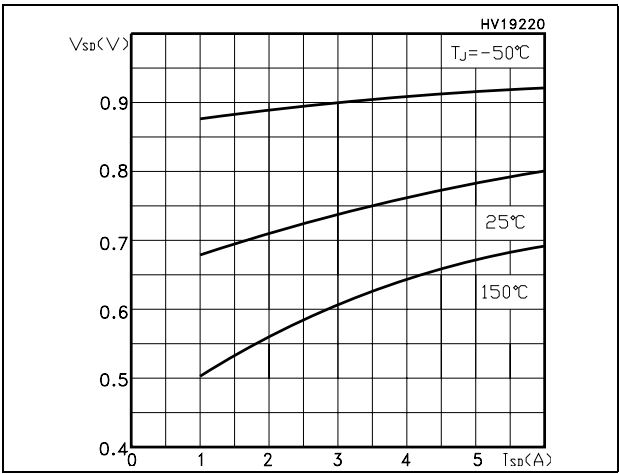


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

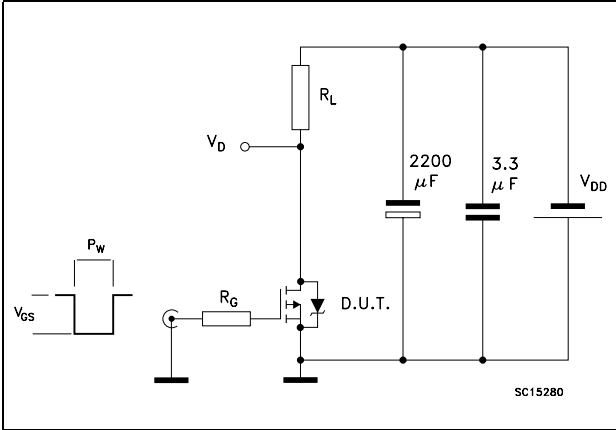


Figure 13. Gate charge test circuit

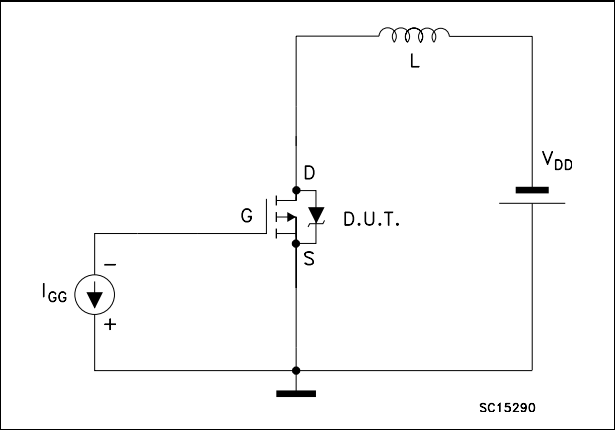
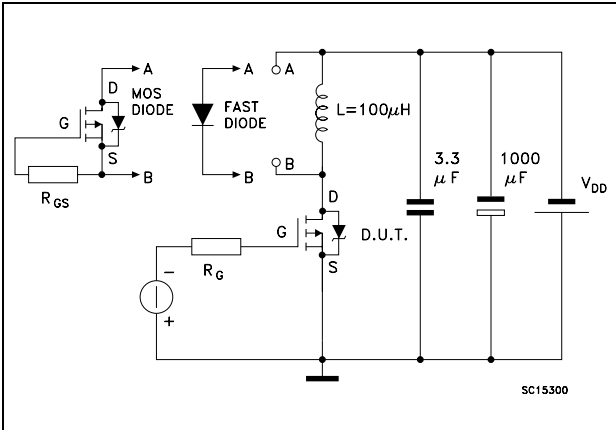


Figure 14. Test circuit for diode recovery behaviour



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

SOT-223 MECHANICAL DATA						
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.80			0.071
B	0.60	0.70	0.80	0.024	0.027	0.031
B1	2.90	3.00	3.10	0.114	0.118	0.122
c	0.24	0.26	0.32	0.009	0.010	0.013
D	6.30	6.50	6.70	0.248	0.256	0.264
e		2.30			0.090	
e1		4.60			0.181	
E	3.30	3.50	3.70	0.130	0.138	0.146
H	6.70	7.00	7.30	0.264	0.276	0.287
V			10°			10°
A1		0.02				

The image contains three mechanical drawings of the SOT-223 package. The top-left drawing is a top view showing dimensions A (height of the top flange), A1 (height of the top flange at the lead), B (width of the top flange), B1 (width of the top flange at the lead), c (width of the top flange at the lead), D (width of the top flange), e (pitch of the leads), e1 (pitch of the leads at the lead), E (height of the top flange), H (height of the top flange), V (lead angle), and A1 (height of the top flange at the lead). The top-right drawing is a side view showing the profile of the package. The bottom drawing is a bottom view showing the layout of the three leads, labeled 1, 2, and 3, with dimensions D (width of the top flange), B1 (width of the top flange at the lead), e (pitch of the leads), and E (height of the top flange).

P008B

5 Revision history

Table 7. Revision history

Date	Revision	Changes
20-Jun-2005	1	First release
13-Dec-2005	2	Final version
04-Aug-2006	3	New template

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