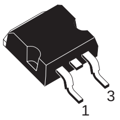
STB75NH02L

N-CHANNEL 24V - 0.0062Ω - 60A - D²PAK
STripFET™ III Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STB75NH02L	24 V	<0.008 Ω	60 A *Note* 1

- $R_{DS(ON)}$ * Qg INDUSTRY's BENCHMARK
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DEVICE

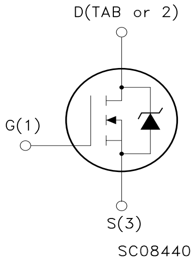


D²PAK

Description

The STB75NH02L utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

Internal schematic diagram



Applications

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY DC/DC CONVERTERS

Order codes

Sales Type	Marking	Package	Packaging
STB75NH02LT4	B75NH02L	D²PAK	TAPE & REEL

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{spike} Note 2	Drain-Source Voltage Rating	30	V
V_{DS}	Drain-Source Voltage (V_{GS} = 0)	24	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D Note 1	Drain Current (continuous) at T_C = 25°C	60	A
I_D	Drain Current (continuous) at T_C = 100°C	53	A
I_{DM} Note 3	Drain Current (pulsed)	240	A
P_{TOT} Note 4	Total Dissipation at T_C = 25°C	80	W
	Derating Factor	0.53	W/°C
E_{AS} Note 5	Single Pulse Avalanche Energy	360	mJ
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 175	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal Resistance Junction-case Max	1.88	°C/W
Rthj-amb	Thermal Resistance Junction-amb Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	I_D = 25 mA, V_{GS}= 0	24			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = 20 V, V_{DS} = 20 V,Tc = 125°C			1 10	µA µA
I_{GSS}	Gate Body Leakage Current (V_{DS} = 0)	V_{GS} = ±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D = 250 µA	1	1.8		V
$R_{DS(on)}$	Static Drain-Source On Resistance	V_{GS}= 10 V, I_D= 30 A V_{GS}= 5 V, I_D= 30 A		0.0062 0.008	0.008 0.014	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} *Note* 6	Forward Transconductance	V_{DS} =10V, I_D = 18A		27		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} =15V, f=1 MHz, V_{GS}=0		2050 545 70		pF pF pF
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}=10V, I_D = 60 A V_{GS} =5V (see Figure 14)		17 7.7 3.5	22	nC nC nC
R_G	Gate Input Resistance	f=1MHz Gate DC Bias =0 Test Signal Level =20mV Open Drain		1.1		Ω

Table 5. Switching times

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD}=10 V, I_D=30 A, R_G=4.7Ω, V_{GS}=10V (see Figure 15)		12 200		ns ns
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD}=10 V, I_D=30A, R_G=4.7Ω, V_{GS}=10V (see Figure 15)		18 25		ns ns

Table 6. Source drain diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain Current Source-drain Current (pulsed)				60 240	A A
V_{SD}*Note* 6	Forward on Voltage	I_{SD}=30 A, V_{GS}=0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD}=60 A, di/dt = 100A/µs, V_{DD}=15 V, Tj=150°C		36 35 3.6		ns µC A

(1) Value limited by wire bonding

(2) Garanted when external Rg=4.7Ω and t_f<t_{fmax}

(3) Pulse width limited by safe operating area

(4) This value is rated according to Rthj-c

(5) Starting Tj =25°C, Id = 30A, Vdd = 15V

(6) Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical Characteristics (curves)

Figure 1. Safe Operating Area

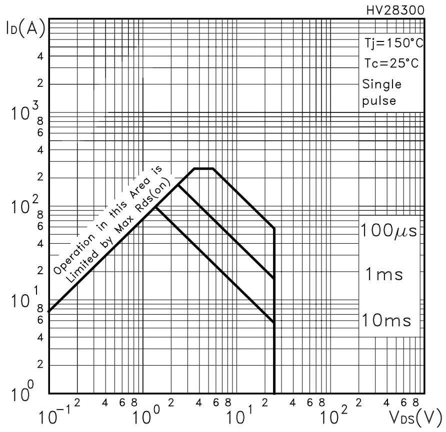


Figure 2. Thermal Impedance

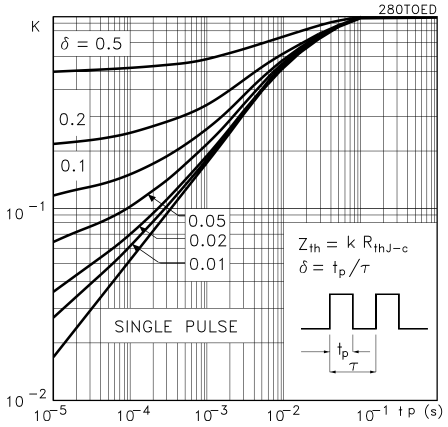


Figure 3. Output Characteristics

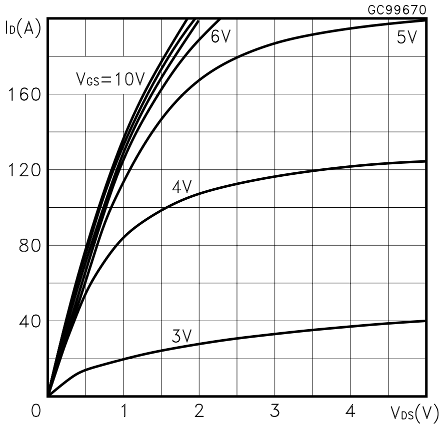


Figure 5. Transfer Characteristics

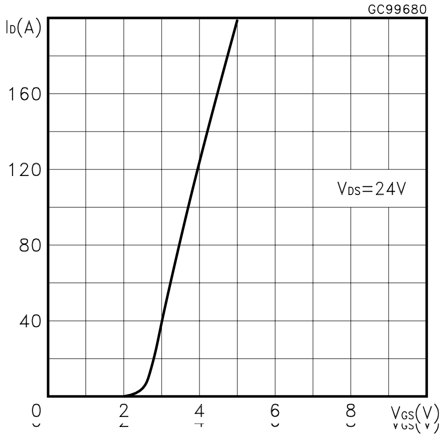


Figure 4. Transconductance

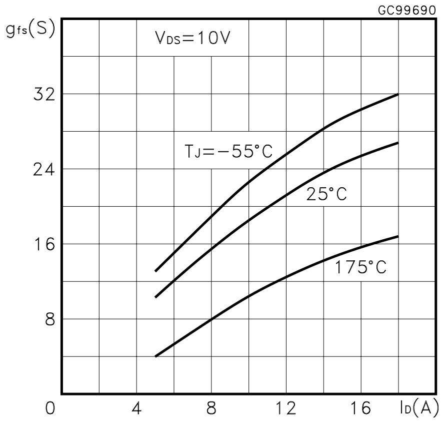


Figure 6. Static Drain-Source on Resistance

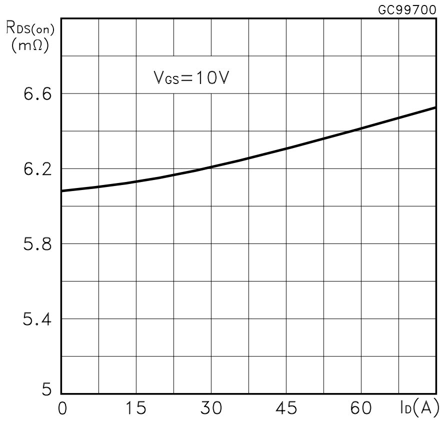


Figure 7. Gate Charge vs Gate -Source Voltage

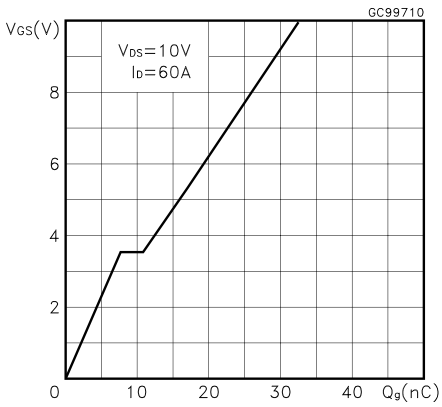


Figure 10. Capacitance Variations

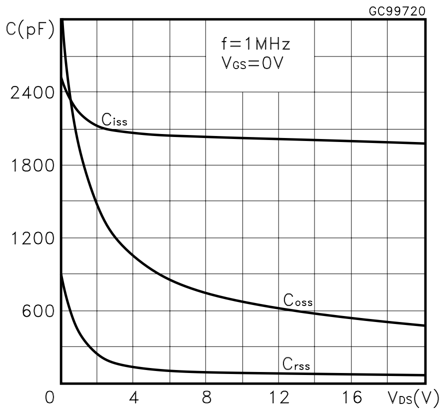


Figure 8. Normalized Gate Threshold Voltage vs Temperatute

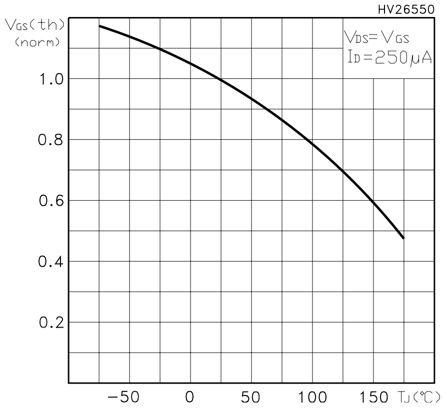


Figure 11. Normalized on Resistance vs Temperature

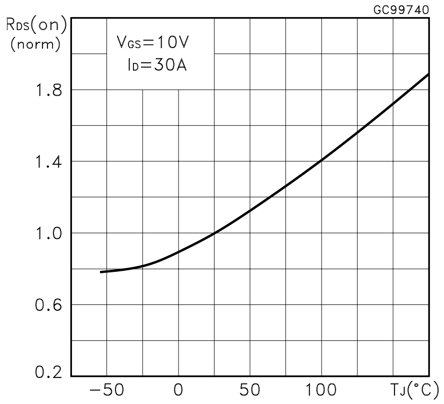


Figure 9. Source-drain Diode Forward Characteristics

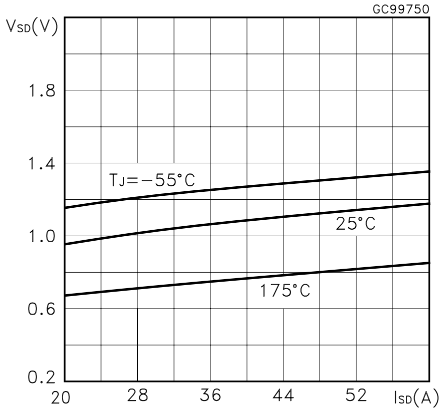
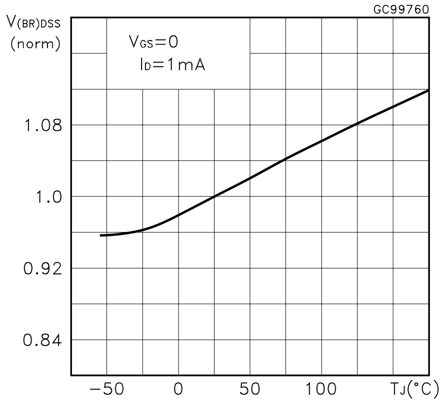


Figure 12. Normalized BVDSS vs Temperature



3 Test circuits

Figure 13. Switching Times Test Circuit For Resistive Load

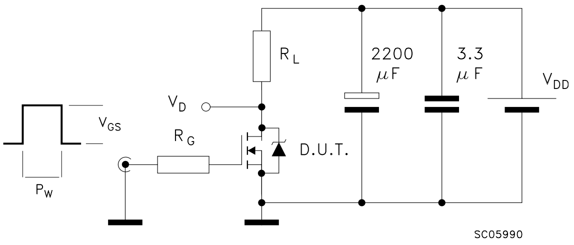


Figure 14. Gate Charge Test Circuit

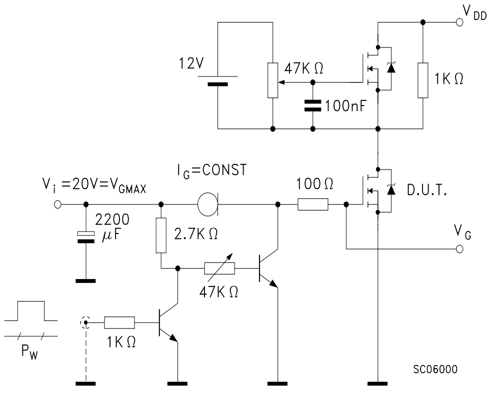


Figure 15. Test Circuit For Indictive Load Switching and Diode Recovery Times

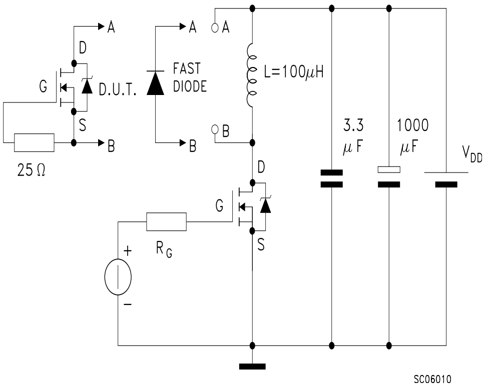


Figure 17. Unclamped Inductive Load Test Circuit

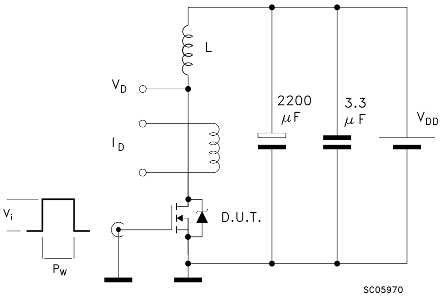
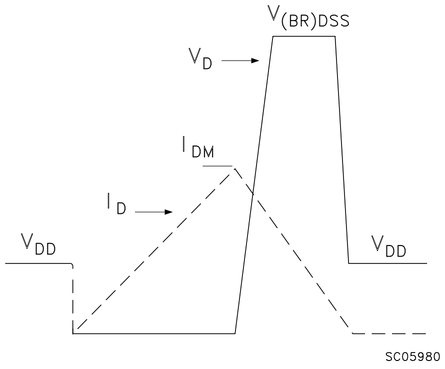


Figure 16. Unclamped Inductive Waveform

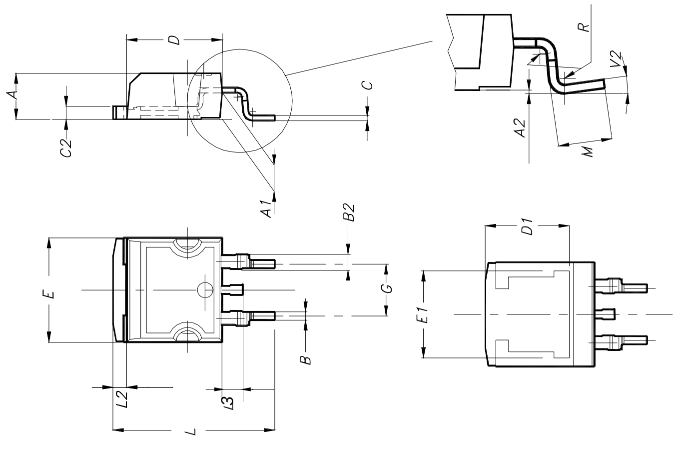


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

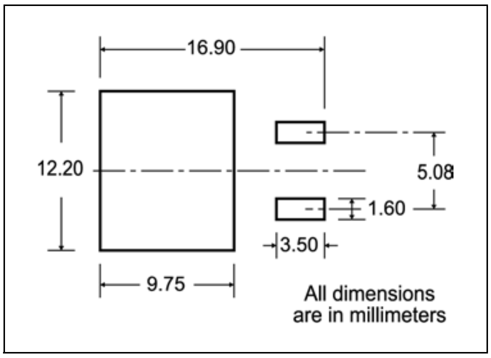
D^2PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0º		4º			

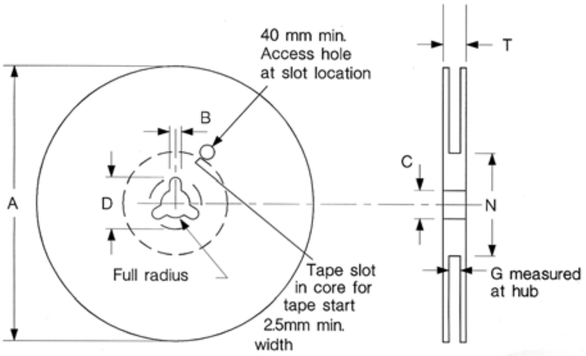


5 Packing mechanical data

D^{2}PAK FOOTPRINT



TAPE AND REEL SHIPMENT



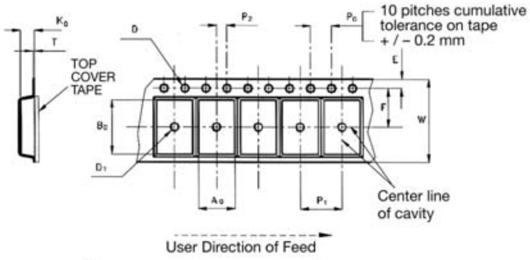
REEL MECHANICAL DATA

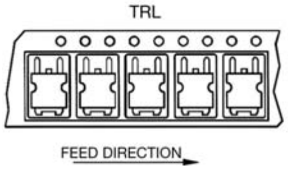
DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

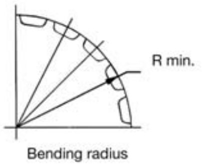
BASE QTY	BULK QTY
1000	1000

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956







* on sales type

6 Revision History

Date	Revision	Changes
19-Oct-2005	2	Complete version

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