



STF3NK100Z - STD3NK100Z STP3NK100Z

N-channel 1000V - 5.4Ω - 2.5A - TO-220 - TO-220FP - DPAK
Zener-protected SuperMESH™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} Max	I _D	P _{TOT}
STF3NK100Z	1000V	< 6Ω	2.5A	25W
STP3NK100Z	1000V	< 6Ω	2.5A	90W
STD3NK100Z	1000V	< 6Ω	2.5A	90W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability

Application

- Switching applications

Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, specialties is taken to ensure a very good dv/dt capability for the most demanding application. Such series complements ST full range of high voltage Power MOSFETs.

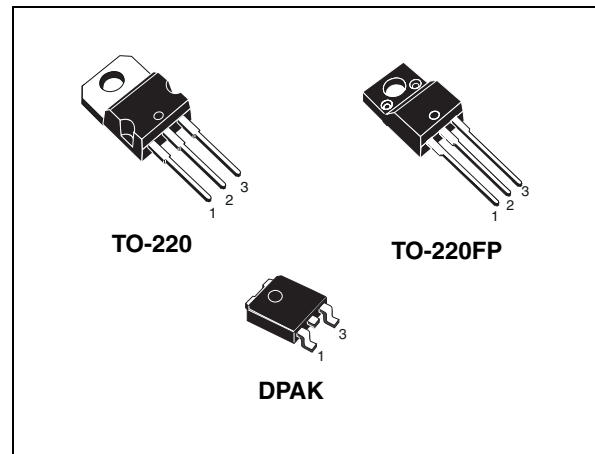


Figure 1. Internal schematic diagram

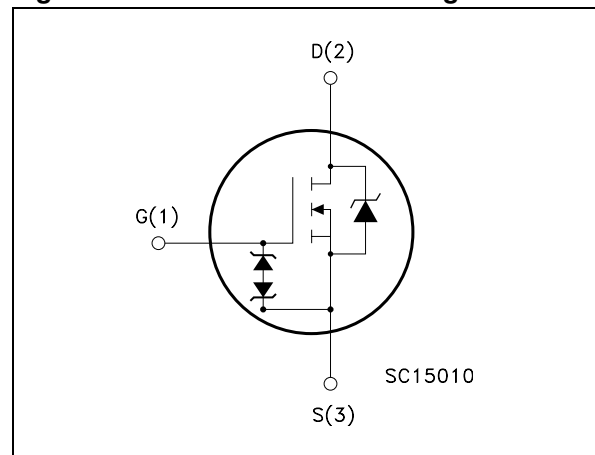


Table 1. Device summary

Order codes	Marking	Package	Packaging
STF3NK100Z	F3NK100Z	TO-220FP	Tube
STP3NK100Z	P3NK100Z	TO-220	Tube
STD3NK100Z	D3NK100Z	DPAK	Tape & reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/DPAK	TO-220FP	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	1000		V
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	2.5	2.5 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	1.57	1.57 ⁽²⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	10	10 ⁽²⁾	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	90	25	W
	Derating factor	0.72	0.2	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD (HBM-C=100pF, R=1.5K Ω)	3000		V
$dv/dt^{(3)}$	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t=1s; T_C=25^\circ\text{C}$)	--	2500	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150		$^\circ\text{C}$

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 2.5\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220/DPAK	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	1.39	5	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb max	62.5		$^\circ\text{C}/\text{W}$
T_L	Maximum lead temperature for soldering purpose	300		

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not-repetitive	2.5	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	110	mJ

1. Pulse width limited by T_{jmax}
2. Starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{V}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 5. On/off

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{mA}$, $V_{GS} = 0$	1000			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating}$, $T_c = 125^{\circ}\text{C}$			1 50	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$, $I_D = 1.25\text{A}$		5.4	6	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{V}$, $I_D = 1.25\text{A}$		2.4		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$		601 53 12		pF pF pF
$C_{oss\text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V to } 800\text{V}$		15		pF
R_G	Gate input resistance	$f = 1\text{MHz}$, open drain		8.6		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 800\text{V}$, $I_D = 2.5\text{A}$ $V_{GS} = 10\text{V}$ (see Figure 17)		18 3.6 9.2		nC nC nC

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2. $C_{oss\text{ eq.}}$ is defined as constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=500V$, $I_D=1.25A$, $R_G=4.7\Omega$, $V_{GS}=10V$ (see Figure 16)		15 7.5		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=500V$, $I_D=1.25A$, $R_G=4.7\Omega$, $V_{GS}=10V$ (see Figure 16)		39 32		ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				2.5 10	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=2.5A$, $V_{GS}=0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=2.5A$, $di/dt=100A/\mu s$, $V_{DD}=100V$, $T_j=25^\circ C$ (see Figure 21)		584 2.3 8		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=2.5A$, $di/dt=100A/\mu s$, $V_{DD}=100V$, $T_j=150^\circ C$ (see Figure 21)		628 2.5 8.1		ns μC A

1. Pulse width limited by package

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 9. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{GS}=\pm 1mA$ (open drain)	30			V

1. The built in back-to-back zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220/ DPAK

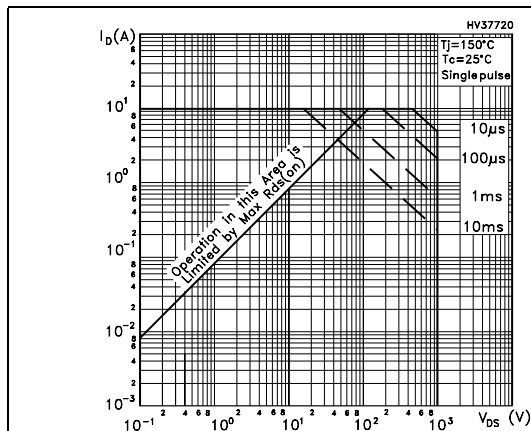


Figure 3. Thermal impedance for TO-220/ DPAK

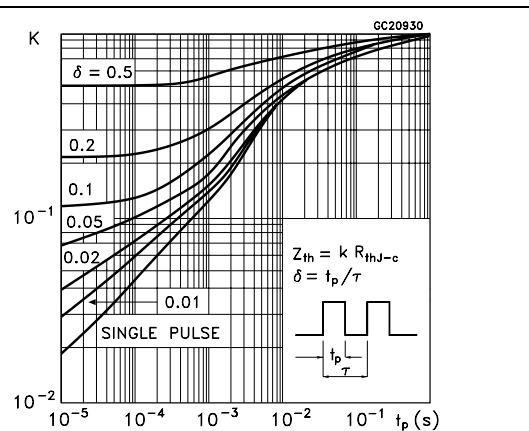


Figure 4. Safe operating area for TO-220FP

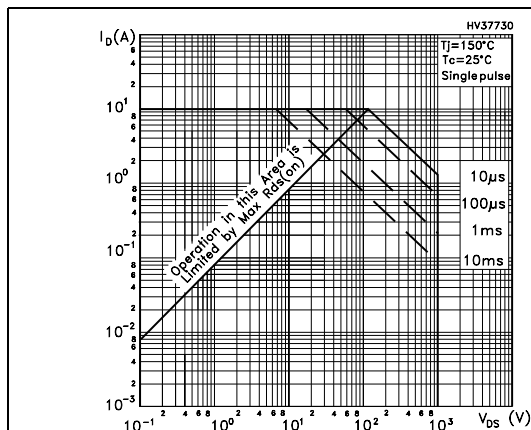


Figure 5. Thermal impedance for TO-220FP

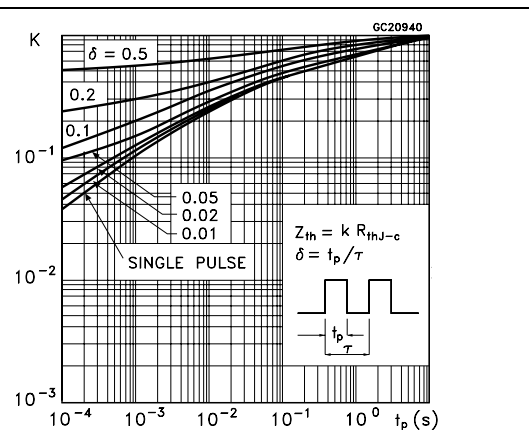


Figure 6. Output characteristics

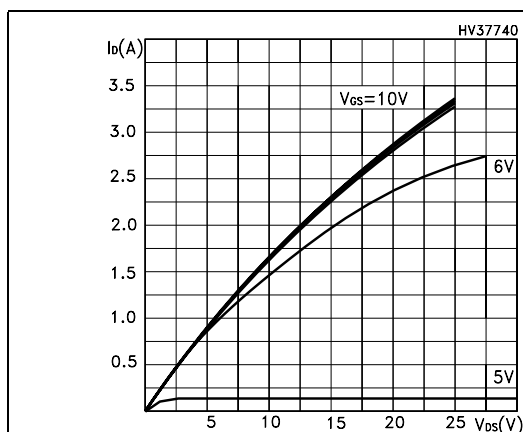


Figure 7. Transfer characteristics

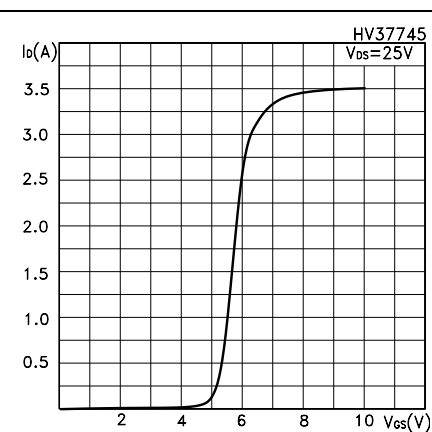


Figure 8. Normalized BV_{DSS} vs. temperature Figure 9. Static drain-source on resistance

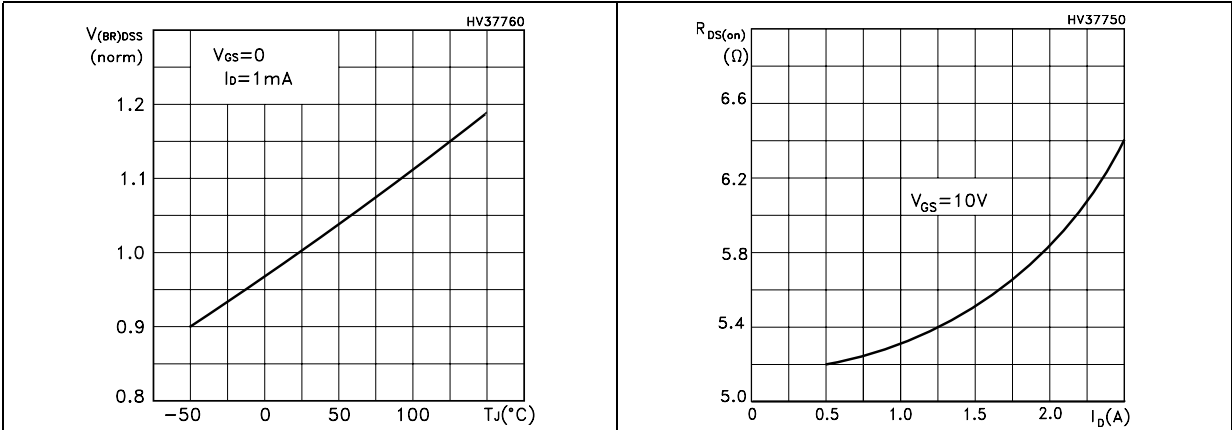


Figure 10. Gate charge vs. gate-source voltage Figure 11. Capacitance variations

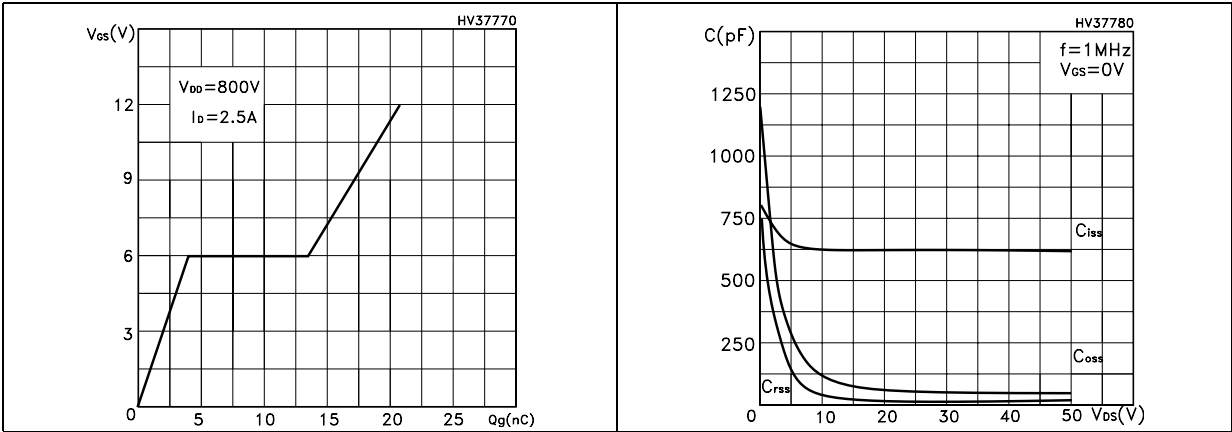


Figure 12. Normalized gate threshold voltage vs. temperature Figure 13. Normalized on resistance vs. temperature

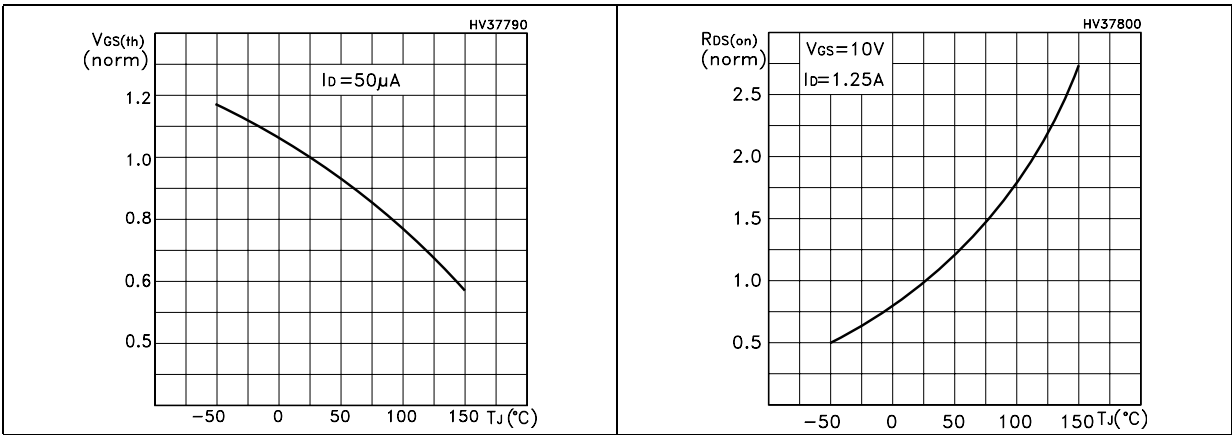


Figure 14. Source-drain diode forward characteristics

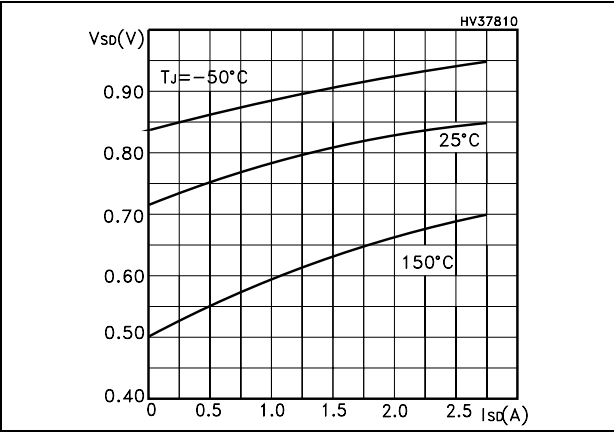
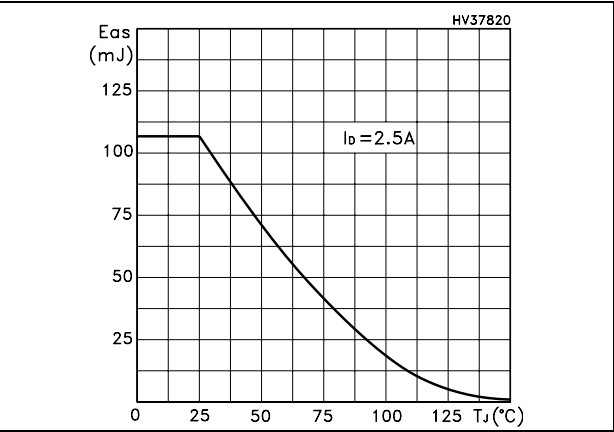


Figure 15. Maximum avalanche energy vs T_J



3 Test circuits

Figure 16. Switching times test circuit for resistive load

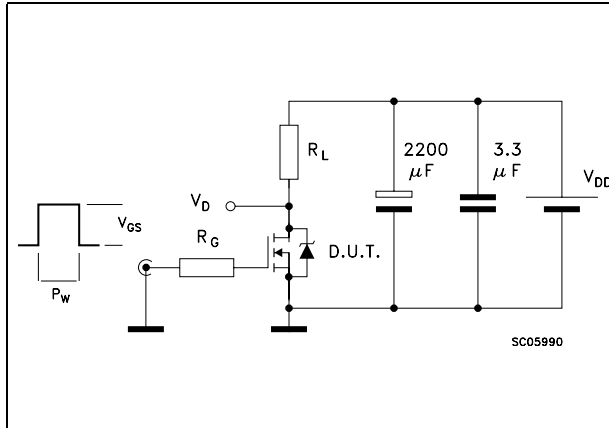


Figure 17. Gate charge test circuit

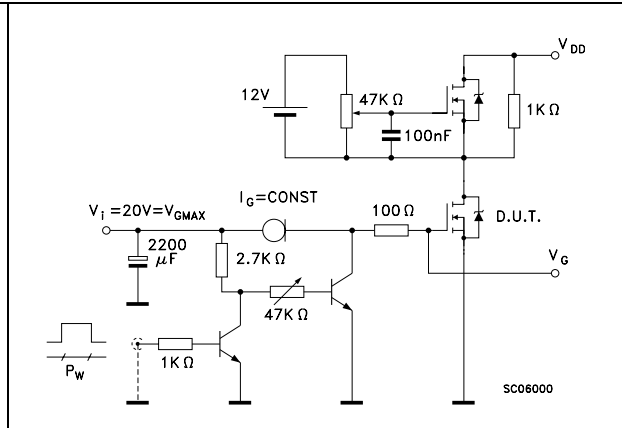


Figure 18. Test circuit for inductive load switching and diode recovery times

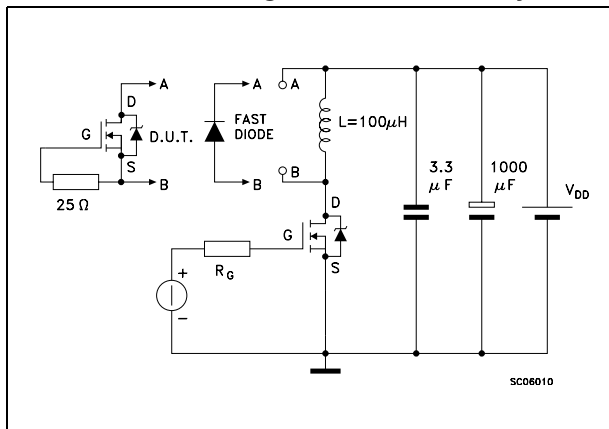


Figure 19. Unclamped inductive load test circuit

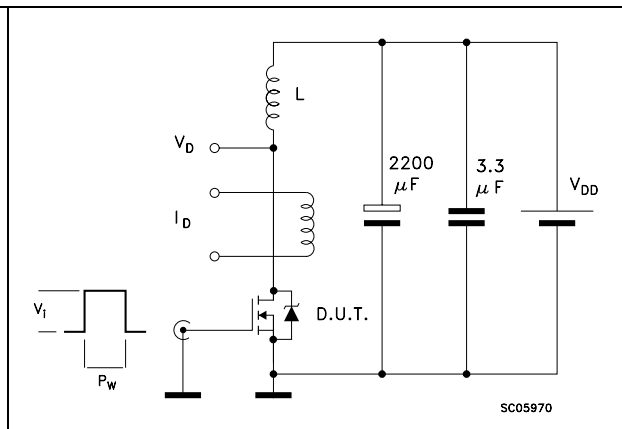


Figure 20. Unclamped inductive waveform

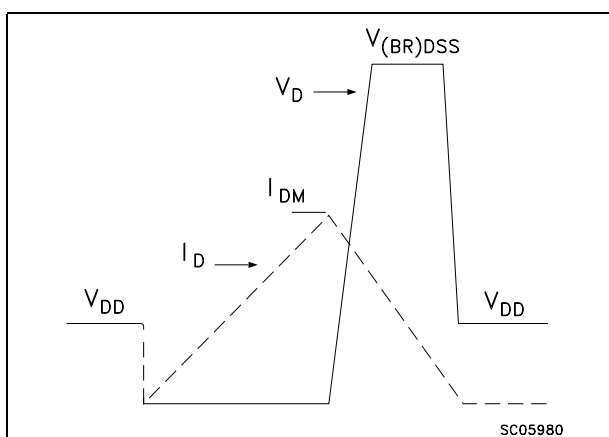
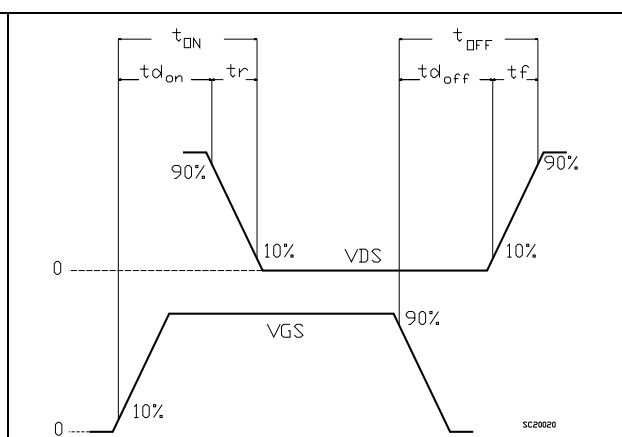


Figure 21. Switching time waveform

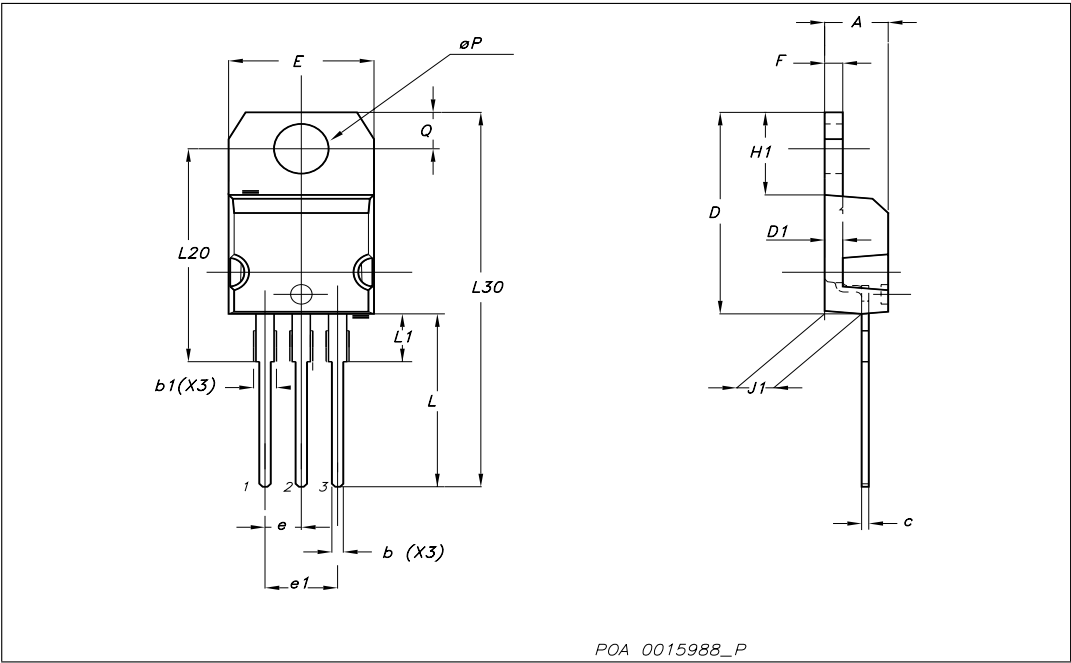


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

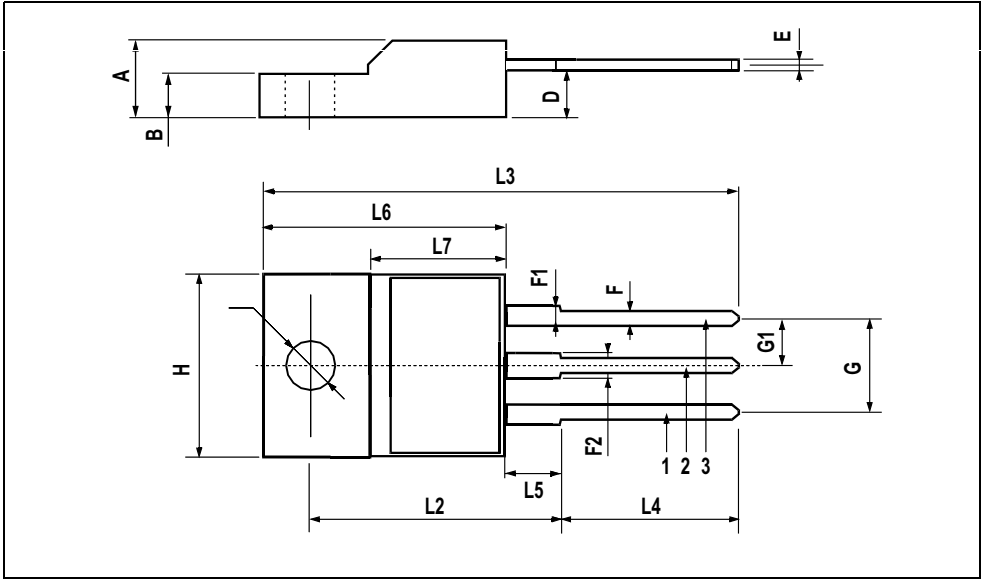
TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
ØP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



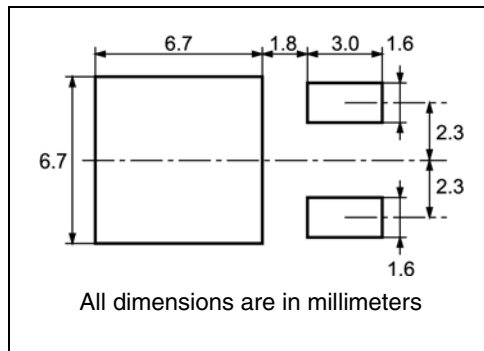
DPAK MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°

The mechanical drawing illustrates the DPAK package geometry. The top view shows dimensions E (total width), b4 (lead width), and L2 (lead length). The side view shows dimensions A (height), A1 (lead height), A2 (lead thickness), B (lead thickness), C (lead thickness), C2 (lead thickness), D (height), D1 (height), E1 (height), e (lead pitch), e1 (lead pitch), H (height), L (lead length), L1 (lead length), L2 (lead length), L4 (lead length), R (radius), and V2 (lead angle). A detail view shows the SEATING PLANE and GAUGE PLANE. A THERMAL PAD is also indicated.

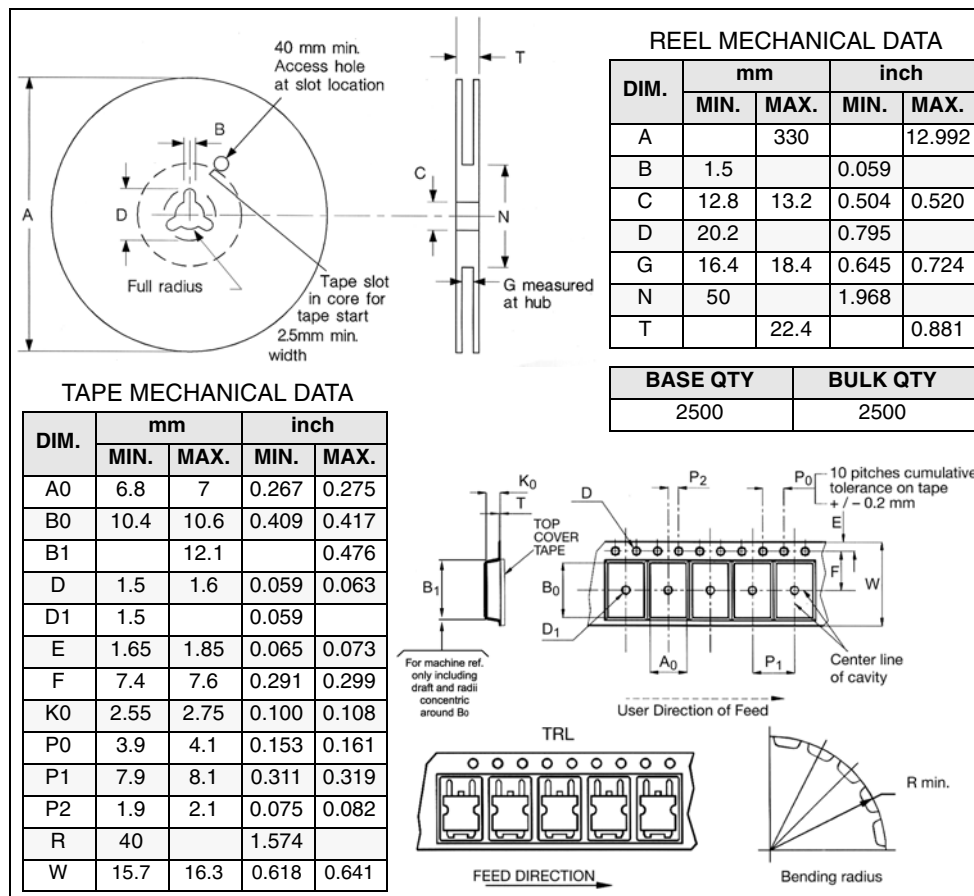
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5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 10. Document revision history

Date	Revision	Changes
17-May-2007	1	First release
18-Oct-2007	2	Added DPAK

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