



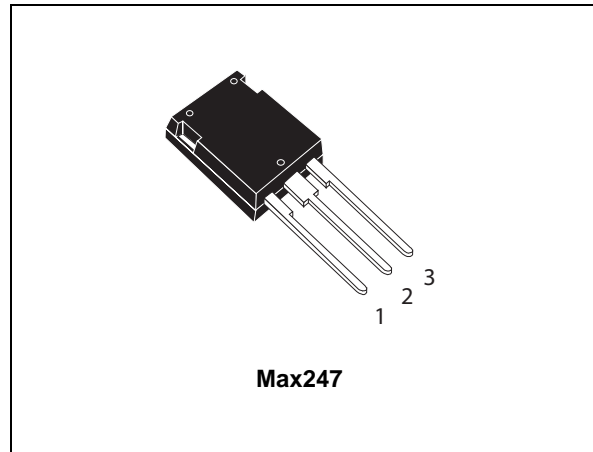
# STY112N65M5

N-channel 650 V, 0.019  $\Omega$ , 96 A, MDmesh™ V Power MOSFET  
Max247

## Features

Order code	V <sub>DSS</sub> @T <sub>JMAX</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STY112N65M5	710 V	< 0.022 $\Omega$	96 A

- Max247 worldwide best R<sub>DS(on)</sub>
- Higher V<sub>DSS</sub> rating
- Higher dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested



## Application

Switching applications

## Description

The device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Figure 1. Internal schematic diagram

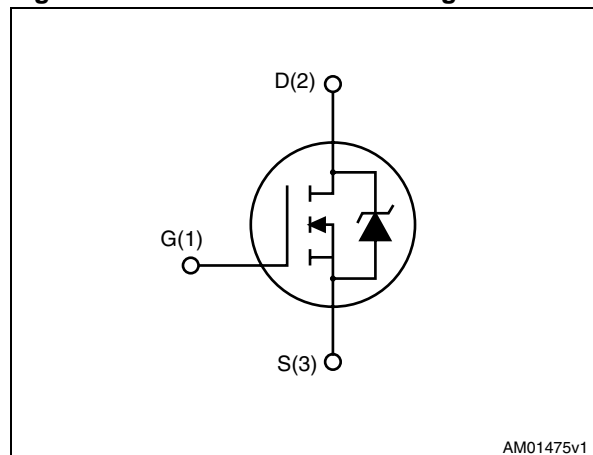


Table 1. Device summary

Order code	Marking	Package	Packaging
STY112N65M5	112N65M5	Max247	Tube

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate- source voltage	25	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	96	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	61	A
$I_{DM}^{(1)}$	Drain current (pulsed)	384	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	625	W
$I_{AR}$	Max current during repetitive or single pulse avalanche (pulse width limited by $T_{JMAX}$ )	17	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{V}$ )	2400	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 96\text{ A}$ ,  $di/dt = 400\text{ A}/\mu\text{s}$ ,  $V_{DD} = 400\text{ V}$ , peak  $V_{DS} < V_{(BR)DSS}$ .

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.2	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	30	$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	650			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$ , $T_C = 125\text{ °C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 48\text{ A}$		0.019	0.022	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$		16870		pF
$C_{oss}$	Output capacitance			365		pF
$C_{rss}$	Reverse transfer capacitance			7		pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }520\text{ V}$		1333		pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }520\text{ V}$		350		pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain		1.26		$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}$ , $I_D = 48\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15</a> )		350		nC
$Q_{gs}$	Gate-source charge			97		nC
$Q_{gd}$	Gate-drain charge			118		nC

- $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 400\text{ V}$ , $I_D = 64\text{ A}$ ,		267		ns
$t_{r(v)}$	Voltage rise time	$R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$		79		ns
$t_{f(i)}$	Current fall time	(see <a href="#">Figure 16</a> )	-	53	-	ns
$t_{c(off)}$	Crossing time	(see <a href="#">Figure 19</a> )		140		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				96	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		384	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 96\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 96\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		570		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100\text{ V}$ (see <a href="#">Figure 16</a> )	-	17		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			60		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 96\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		695		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$	-	26		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 16</a> )		73		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

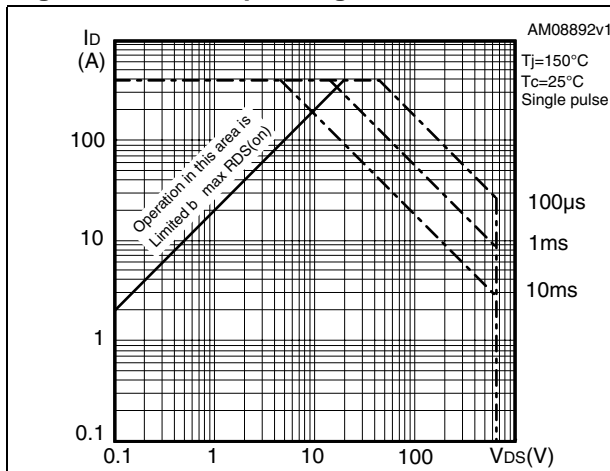


Figure 3. Thermal impedance

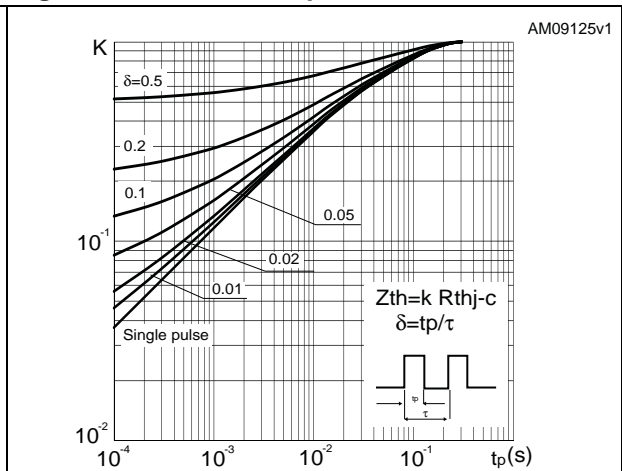


Figure 4. Output characteristics

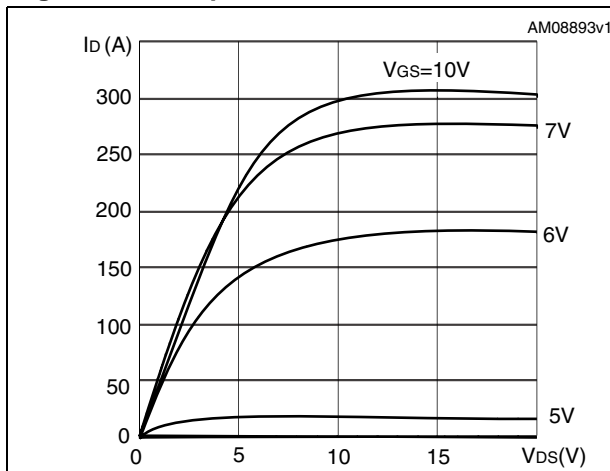


Figure 5. Transfer characteristics

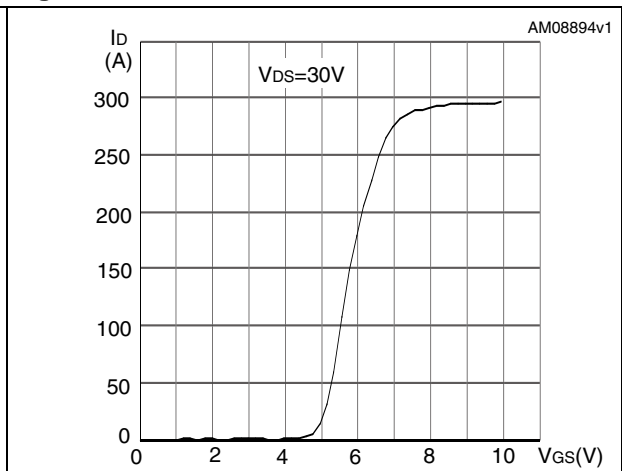


Figure 6. Normalized  $B_{V_{DS}}$  vs temperature

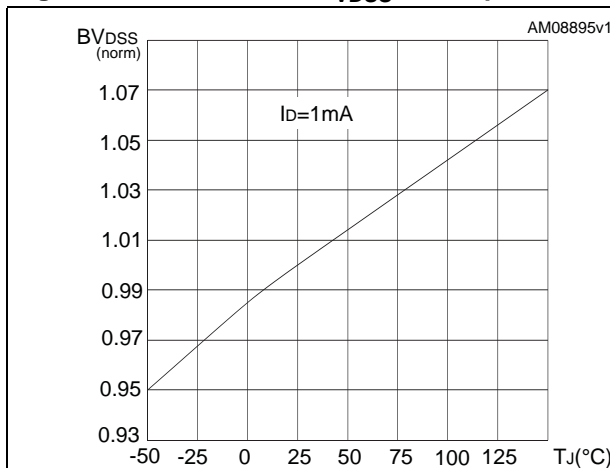


Figure 7. Static drain-source on resistance

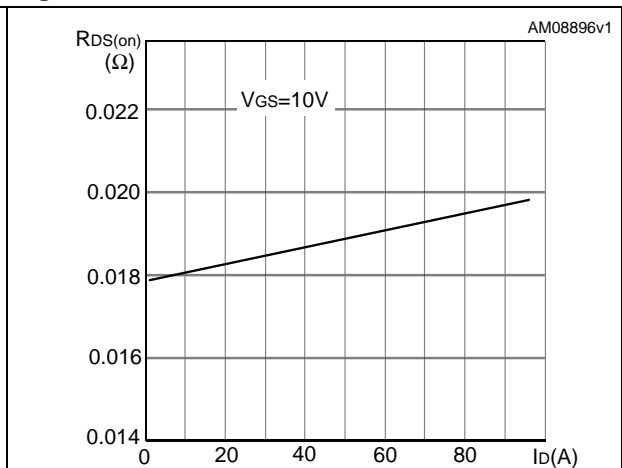


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

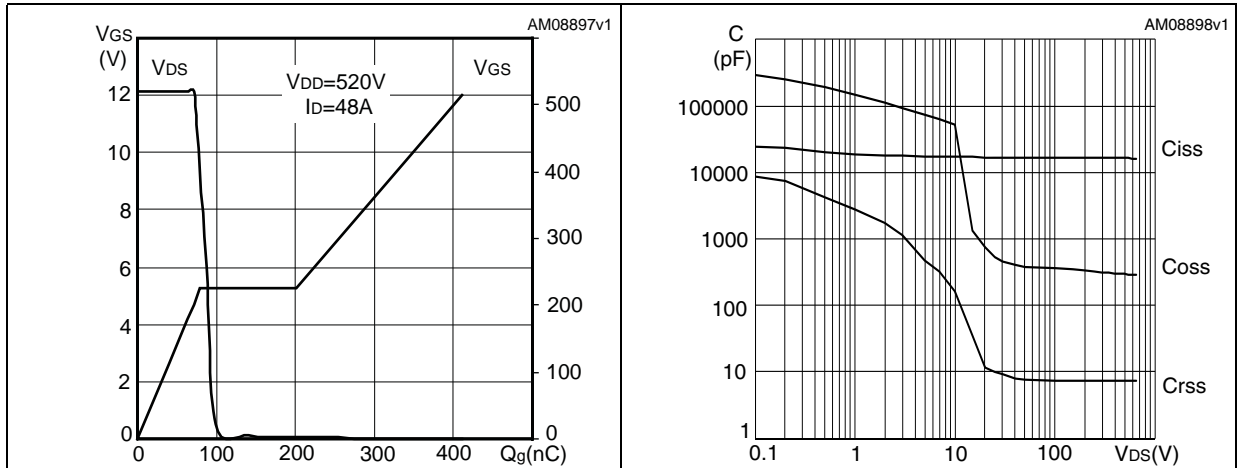


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

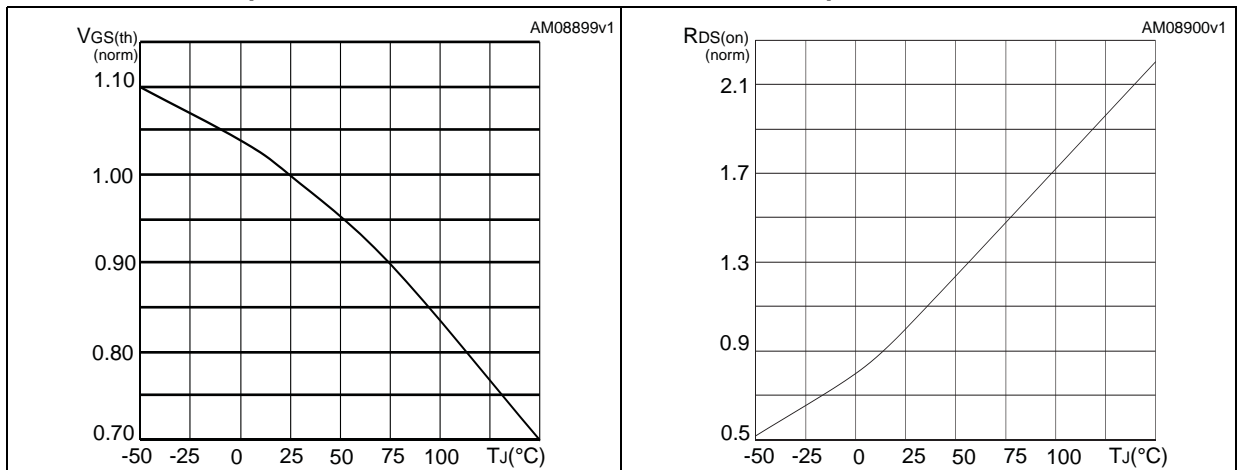
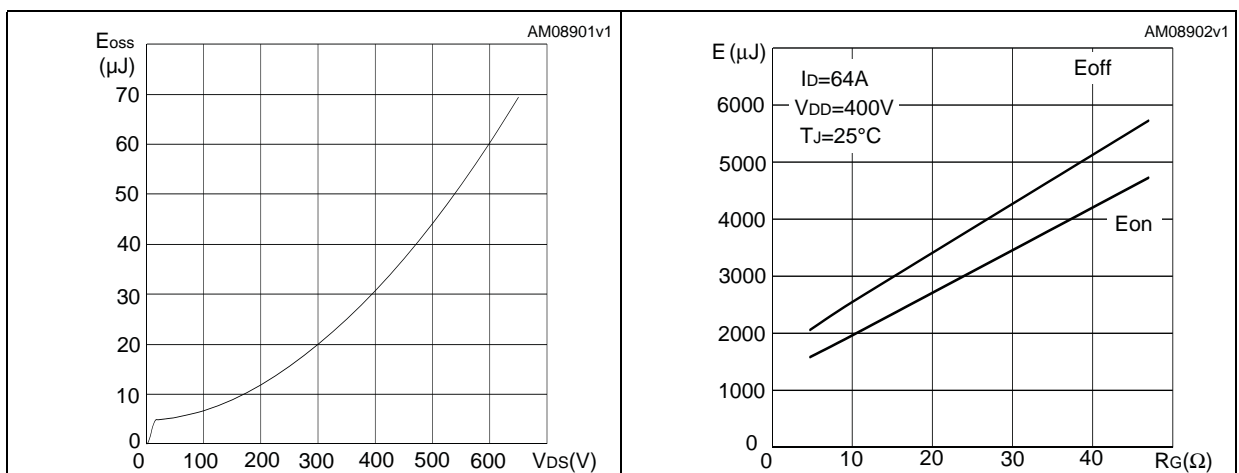


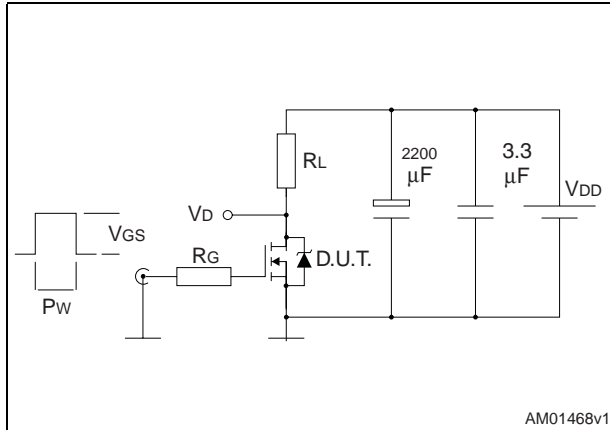
Figure 12. Output capacitance stored energy Figure 13. Switching losses vs gate resistance (1)



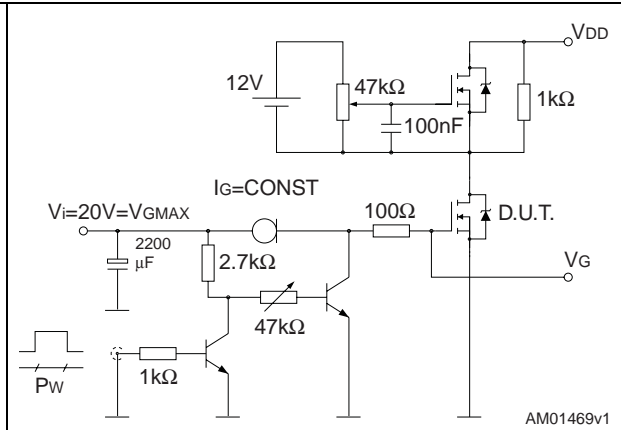
1.  $E_{on}$  including reverse recovery of a SiC diode

### 3 Test circuits

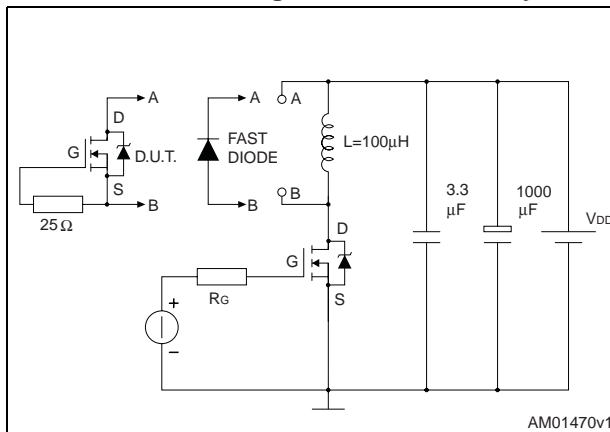
**Figure 14. Switching times test circuit for resistive load**



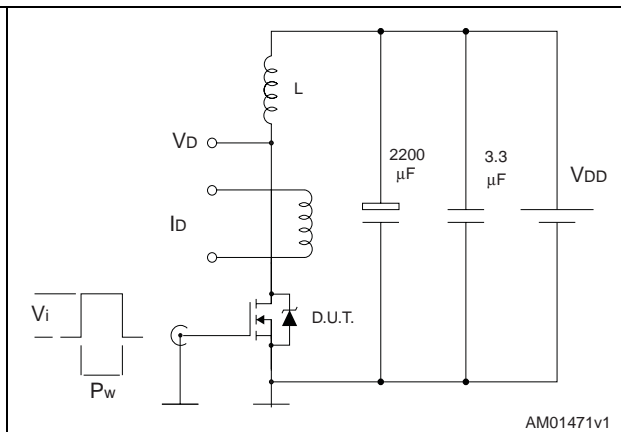
**Figure 15. Gate charge test circuit**



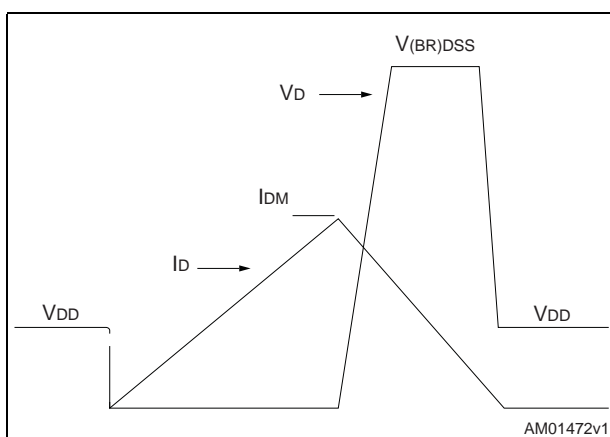
**Figure 16. Test circuit for inductive load switching and diode recovery times**



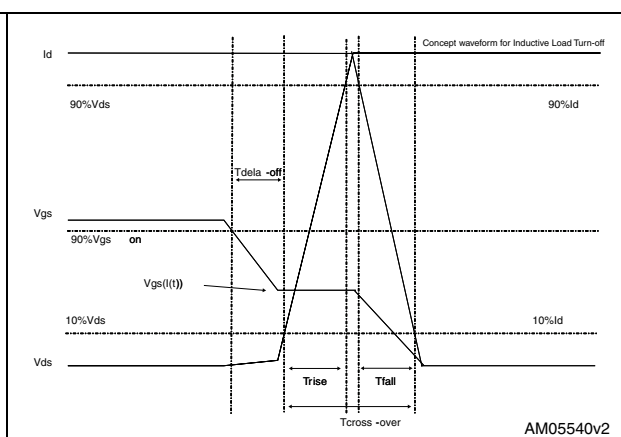
**Figure 17. Unclamped inductive load test circuit**



**Figure 18. Unclamped inductive waveform**



**Figure 19. Switching time waveform**



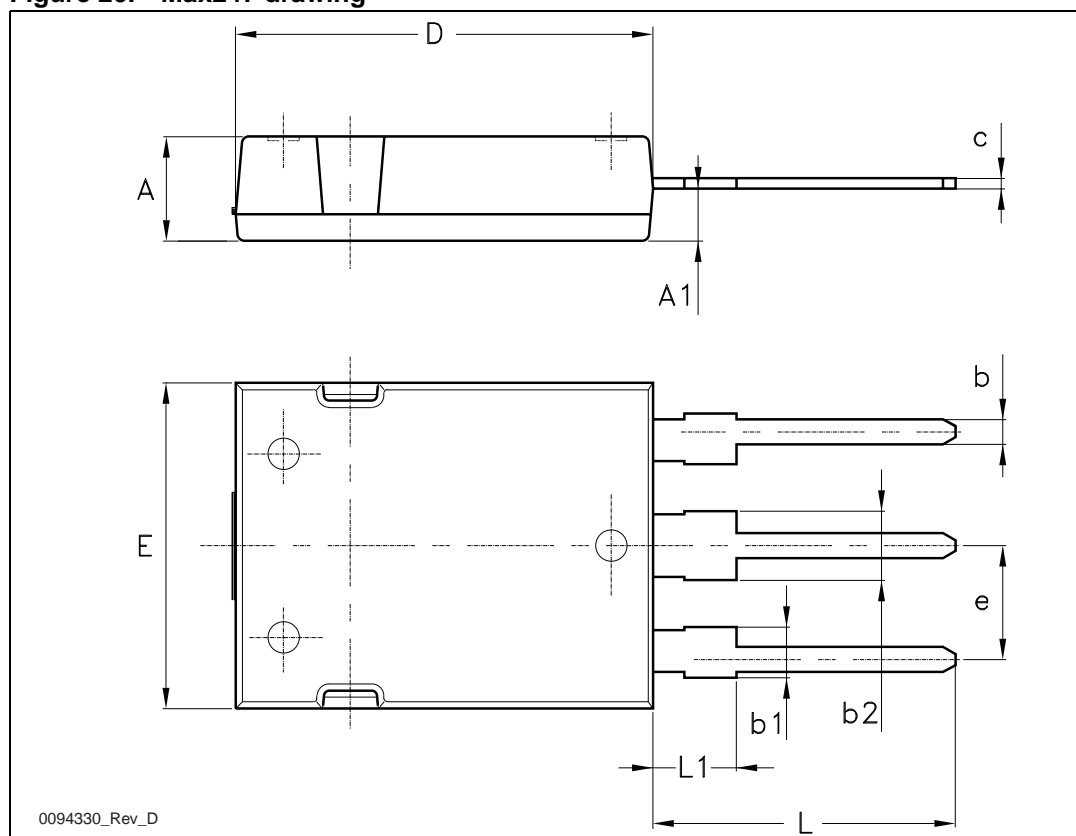
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

Table 8. Max247 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.70		5.30
A1	2.20		2.60
b	1.00		1.40
b1	2.00		2.40
b2	3.00		3.40
c	0.40		0.80
D	19.70		20.30
e	5.35		5.55
E	15.30		15.90
L	14.20		15.20
L1	3.70		4.30

Figure 20. Max247 drawing



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
20-Jan-2009	1	First release.
20-May-2011	2	Document status promoted from preliminary data to datasheet.

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