



# STP40NF10

N-CHANNEL 100V - 0.025Ω - 50A - TO-220  
LOW GATE CHARGE STripFET™II MOSFET

**Table 1: General Features**

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STP40NF10	100 V	< 0.028 Ω	50 A

- TYPICAL R<sub>DS(on)</sub> = 0.025Ω
- EXCEPTIONAL dv/dt CAPABILITY
- LOW GATE CHARGE AT 100°C
- APPLICATION ORIENTED CHARACTERIZATION
- 100% AVALANCHE TESTED

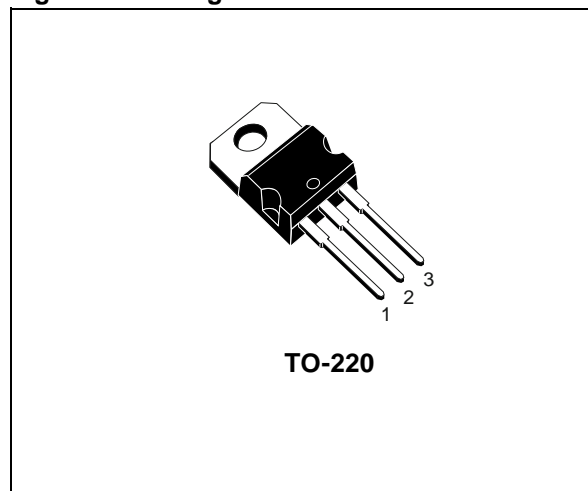
## DESCRIPTION

This MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

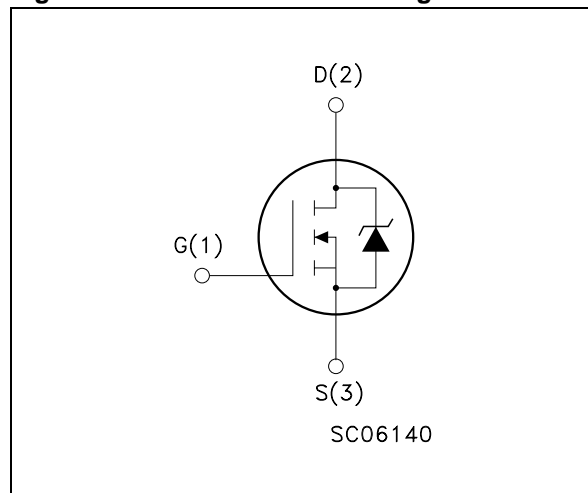
## APPLICATIONS

- DC-DC & DC-AC CONVERTERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- AUTOMOTIVE ENVIRONMENT

**Figure 1: Package**



**Figure 2: Internal Schematic Diagram**



**Table 2: Order Codes**

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP40NF10	P40NF10@	TO-220	TUBE

**Table 3: Absolute Maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source Voltage ( $V_{GS} = 0$ )	100	V
$V_{DGR}$	Drain-gate Voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	100	V
$V_{GS}$	Gate- source Voltage	$\pm 20$	V
$I_D$ (*)	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	50	A
$I_D$	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	35	A
$I_{DM}$ (●)	Drain Current (pulsed)	200	A
$P_{TOT}$	Total Dissipation at $T_C = 25^\circ\text{C}$	150	W
	Derating Factor	1	W/ $^\circ\text{C}$
dv/dt (1)	Peak Diode Recovery voltage slope	27	V/ns
$E_{AS}$ (2)	Single Pulse Avalanche Energy	385	mJ
$T_{stg}$	Storage Temperature	-55 to 175	$^\circ\text{C}$
$T_j$	Operating Junction Temperature		

(1)  $I_{SD} \leq 50\text{A}$ ,  $di/dt \leq 600\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX.}$

(2) Starting  $T_j=25^\circ\text{C}$ ,  $I_D=50\text{A}$ ,  $V_{DD}=25\text{V}$

(●) Pulse width limited by safe operating area

(\*) Pulse with limited by safe operating area

**Table 4: Thermal Data**

Rthj-case	Thermal Resistance Junction-case Max	1	$^\circ\text{C}/\text{W}$
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	$^\circ\text{C}/\text{W}$
$T_l$	Maximum Lead Temperature For Soldering Purpose	300	$^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS** ( $T_{CASE} = 25^\circ\text{C}$  UNLESS OTHERWISE SPECIFIED)**Table 5: Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu\text{A}$ , $V_{GS} = 0$	100			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ , $T_C = 125^\circ\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{V}$			$\pm 100$	nA

**Table 6: On**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{V}$ , $I_D = 25 \text{ A}$		0.025	0.028	$\Omega$

## ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}$ (1)	Forward Transconductance	$V_{DS} = 15V, I_D = 25A$		22		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V, f = 1\text{ MHz}, V_{GS} = 0$		2180 298 83.7		pF pF pF

Table 8: Switching On

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 50V, I_D = 25A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 16)		21 46		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 80V, I_D = 50A,$ $V_{GS} = 10V$ (see Figure 19)		57.6 13.3 17.5	76	nC nC nC

Table 9: Switching Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ $t_f$	Turn-off-Delay Time Fall Time	$V_{DD} = 50V, I_D = 25A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 16)		54 13		ns ns

Table 10: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				50	A
$I_{SDM}$ (2)	Source-drain Current (pulsed)				200	A
$V_{SD}$ (1)	Forward On Voltage	$I_{SD} = 50A, V_{GS} = 0$			1.3	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 50A, di/dt = 100A/\mu s,$ $V_{DD} = 25V, T_j = 150^\circ C$ (see test circuit, Figure 5)		90 333 7.4		ns nC A

(1) Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

Figure 3: Safe Operating Area

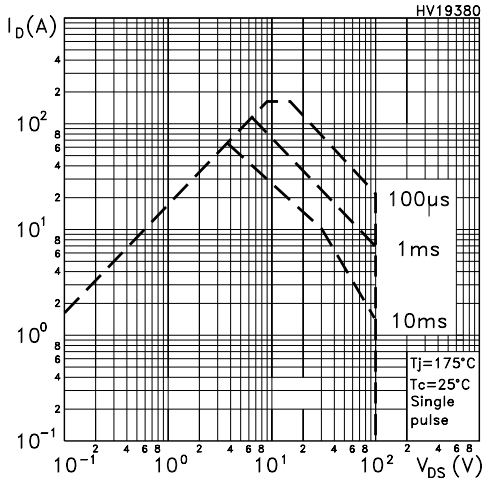


Figure 4: Output Characteristics

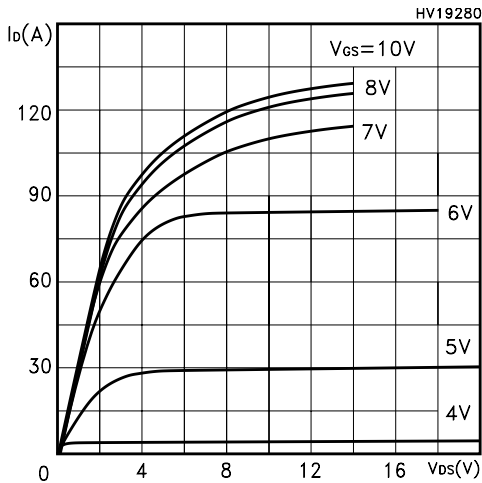


Figure 5: Transconductance

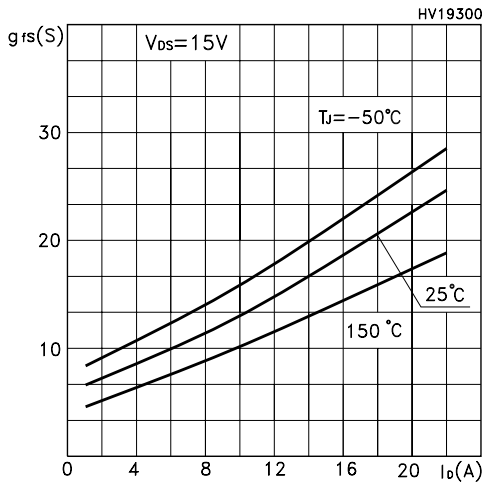


Figure 6: Thermal Impedance

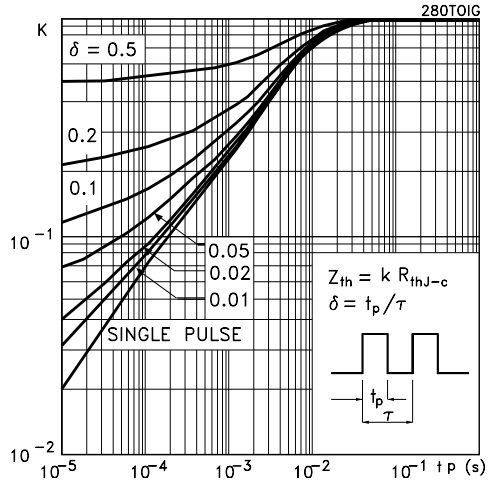


Figure 7: Transfer Characteristics

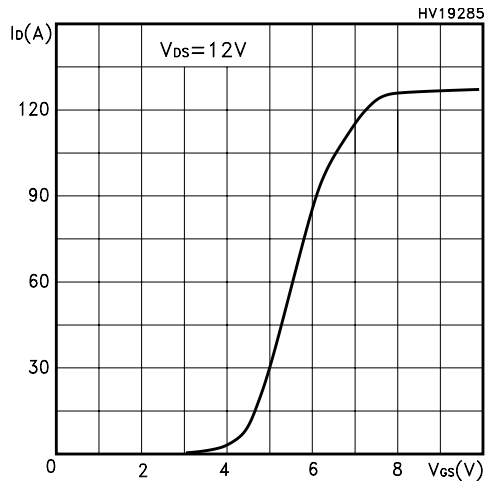


Figure 8: Static Drain-source On Resistance

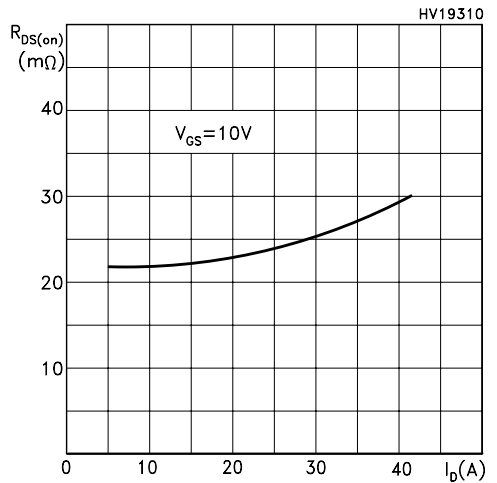


Figure 9: Gate Charge vs Gate-source Voltage

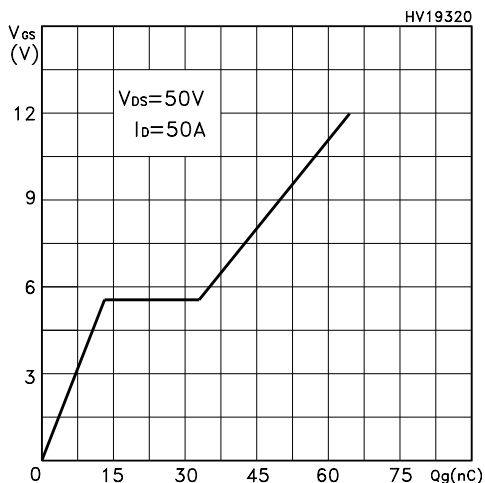


Figure 10: Normalized Gate Threshold Voltage vs Temperature

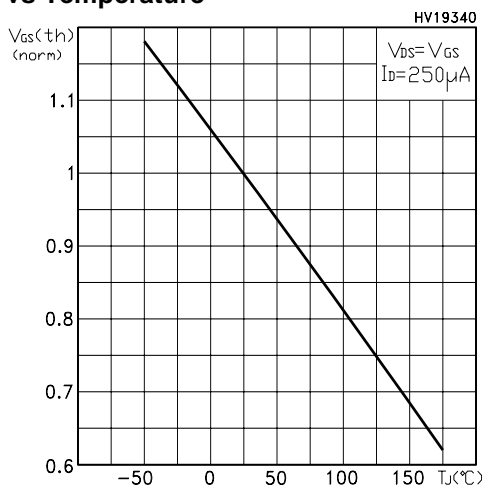


Figure 11: Source-Drain Diode Forward Characteristics

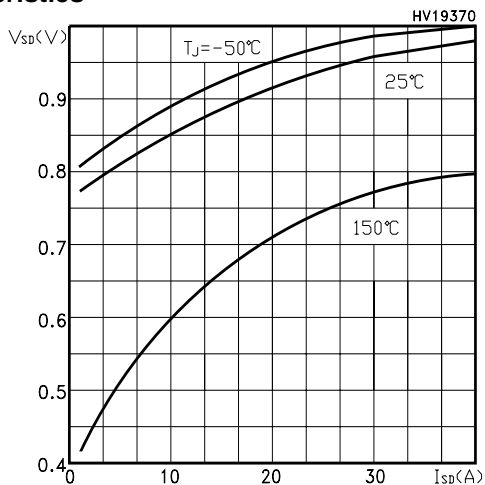


Figure 12: Capacitance Variations

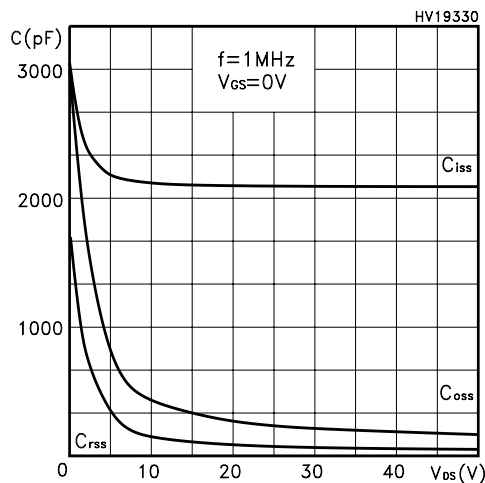


Figure 13: Normalized On Resistance vs Temperature

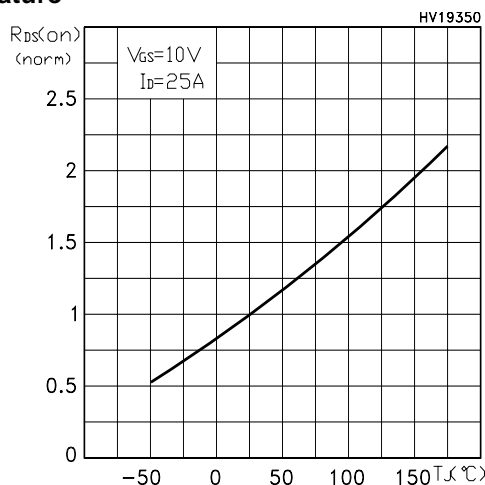


Figure 14: Normalized Breakdown Voltage vs Temperature

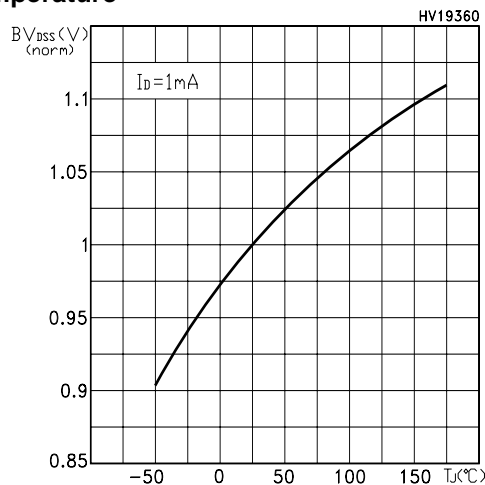


Figure 15: Unclamped Inductive Load Test Circuit

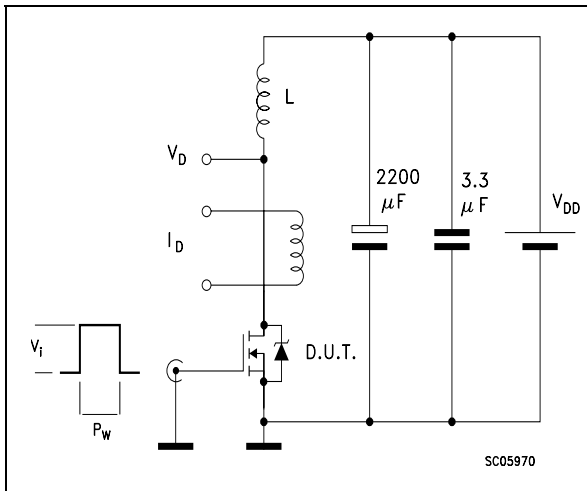


Figure 16: Switching Times Test Circuit For Resistive Load

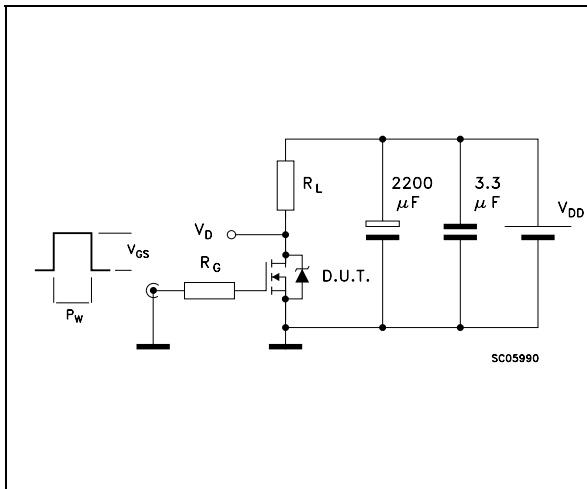


Figure 17: Test Circuit For Inductive Load Switching and Diode Recovery Times

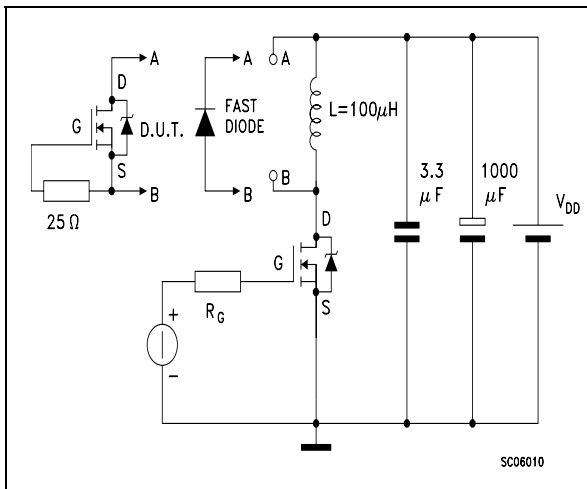


Figure 18: Unclamped Inductive Waferform

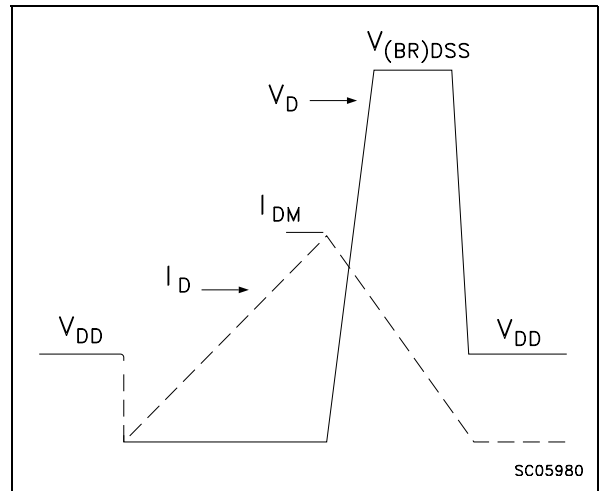
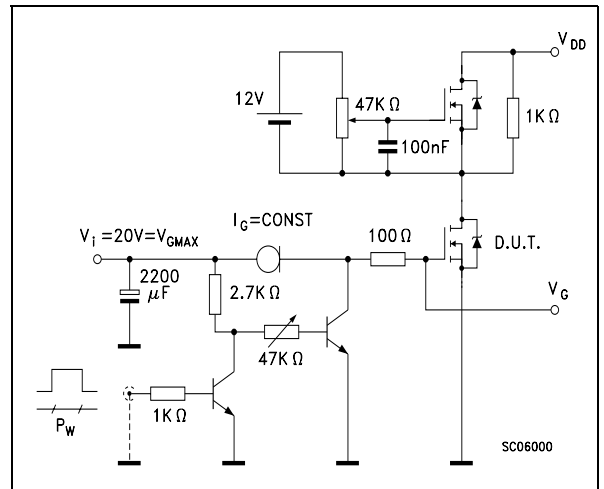
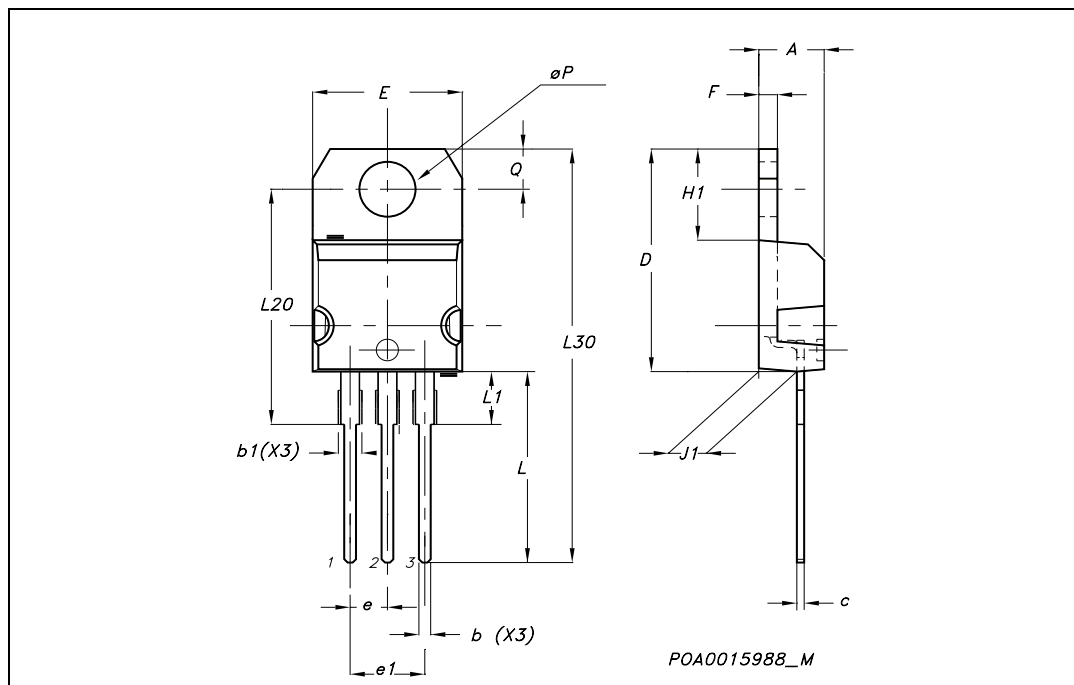


Figure 19: Gate Charge Test Circuit



## TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
$\phi P$	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



**Table 11: Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
14-Dec-2004	2	New Stylesheet. Datasheet according to PCN DSG-TRA/03/382

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