

Complementary transistor pair in a single package

Features

- Low $V_{CE(sat)}$
- Simplified circuit design
- Reduced component count
- Low spread of dynamic parameters

Application

- Compact fluorescent lamp (CFL) 220 V mains

Description

The STD830CP40 is a hybrid complementary pair of power bipolar transistors manufactured by using the high voltage multi-epitaxial planar technology for high switching speeds and medium voltage capability.

The STD830CP40 is housed in dual island DIP-8 package with separated terminals for higher assembly flexibility, specifically recommended to be used in a new solution for compact fluorescent lamp (CFL).

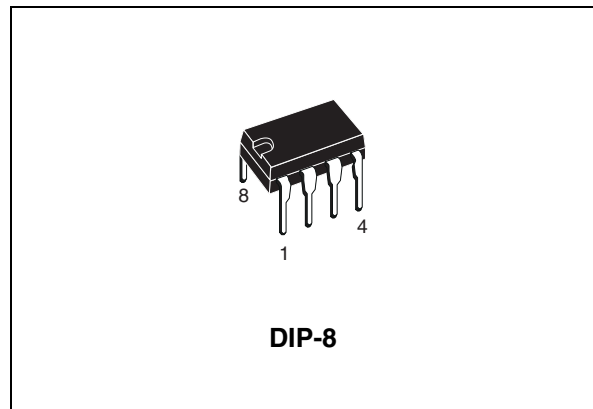


Figure 1. Internal schematic diagram

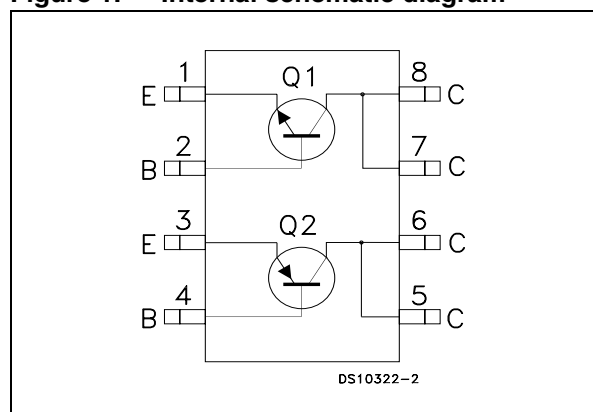


Table 1. Device summary

Order code	Marking	Package	Packing
STD830CP40	D830CP40	DIP-8	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		NPN	PNP	
V_{CBO}	Collector-base voltage ($I_E = 0$)	700	500	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	400		V
V_{EBO}	Emitter-base voltage ($I_C = 0, I_B = 1.5 \text{ A}, t_p < 10 \text{ ms}$)	$V_{(BR)EBO}$		V
I_C	Collector current	3		A
I_{CM}	Collector peak current ($t_p < 5 \text{ ms}$)	6		A
I_B	Base current	1.5		A
I_{BM}	Base peak current ($t_p < 1 \text{ ms}$)	3		A
P_{TOT}	Total dissipation at $T_{amb} = 25 \text{ °C}$ single transistor	3		W
P_{TOT}	Total dissipation at $T_{amb} = 25 \text{ °C}$ both transistors	2.2		W
T_{STG}	Storage temperature	-65 to 150		°C
T_J	Max. operating junction temperature	150		°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJA}^{(1)}$	Thermal resistance junction-ambient (Single transistor)	42	°C/W
$R_{thJA}^{(1)}$	Thermal resistance junction-ambient (Both transistors)	57	°C/W

1. When mounted on 25mm square pad of 2 oz. copper, $t \leq 10 \text{ sec}$.

Note: For PNP types voltage and current values are negative

2 Electrical characteristics

$T_{\text{case}} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector cut-off current ($V_{\text{BE}} = 0$)	For NPN: $V_{\text{CE}} = 700\text{ V}$ $V_{\text{CE}} = 700\text{ V}$ $T_{\text{C}} = 125^{\circ}\text{C}$			0.1 0.5	mA mA
		For PNP: $V_{\text{CE}} = 500\text{ V}$ $V_{\text{CE}} = 500\text{ V}$ $T_{\text{C}} = 125^{\circ}\text{C}$			0.1 0.5	mA mA
$V_{(\text{BR})\text{EBO}}$	Emitter-base breakdown voltage ($I_{\text{C}} = 0$)	$I_{\text{E}} = 10\text{ mA}$ For NPN: For PNP:	10 5		18 10	V V
$V_{\text{CEO(sus)}}^{(1)}$	Collector-emitter sustaining voltage ($I_{\text{B}} = 0$)	$I_{\text{C}} = 5\text{ mA}$	400			V
$V_{\text{CE(sat)}}^{(1)}$	Collector-emitter saturation voltage	$I_{\text{C}} = 0.7\text{ A}$ $I_{\text{B}} = 0.1\text{ A}$			0.5	V
		$I_{\text{C}} = 1\text{ A}$ $I_{\text{B}} = 0.2\text{ A}$			0.5	V
$V_{\text{BE(sat)}}^{(1)}$	Base-emitter saturation voltage	$I_{\text{C}} = 0.5\text{ A}$ $I_{\text{B}} = 0.1\text{ A}$			1.1	V
		$I_{\text{C}} = 1\text{ A}$ $I_{\text{B}} = 0.2\text{ A}$			1.2	V
$h_{\text{FE}}^{(1)}$	DC current gain	$I_{\text{C}} = 10\text{ mA}$ $V_{\text{CE}} = 5\text{ V}$	10			
		$I_{\text{C}} = 0.7\text{ A}$ $V_{\text{CE}} = 5\text{ V}$	18		34	
		$I_{\text{C}} = 2\text{ A}$ $V_{\text{CE}} = 5\text{ V}$	4			
t_{r} t_{s} t_{f}	Resistive load					
	Rise time	$I_{\text{C}} = 0.7\text{ A}$ $V_{\text{CC}} = 250\text{ V}$		100		ns
	Storage time	$I_{\text{B1}} = 0.14\text{ A}$ $I_{\text{B2}} = -0.14\text{ A}$		2.4		μs
t_{f}	Fall time	$t_{\text{p}} = 30\text{ }\mu\text{s}$		100		ns
t_{s} t_{f}	Inductive load					
	Storage time	$I_{\text{C}} = 1\text{ A}$ $I_{\text{B1}} = 0.2\text{ A}$ $V_{\text{BE(off)}} = -5\text{ V}$ $R_{\text{BB}} = 0$		450		ns
	Fall time	$V_{\text{clamp}} = 200\text{ V}$ $L = 1\text{ mH}$		100		ns

1. Pulse test: pulse duration $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Note: For PNP types voltage and current values are negative

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

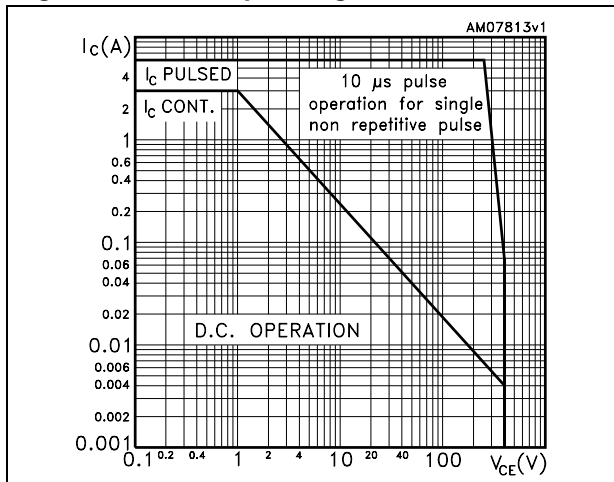


Figure 3. Derating curve

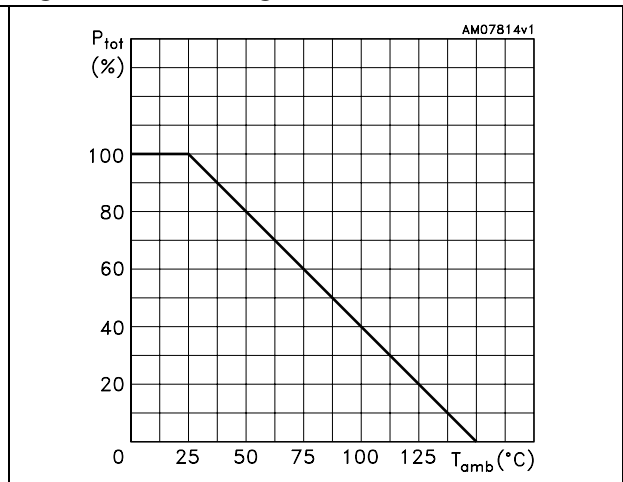


Figure 4. DC current gain NPN ($V_{CE} = 5\text{ V}$)

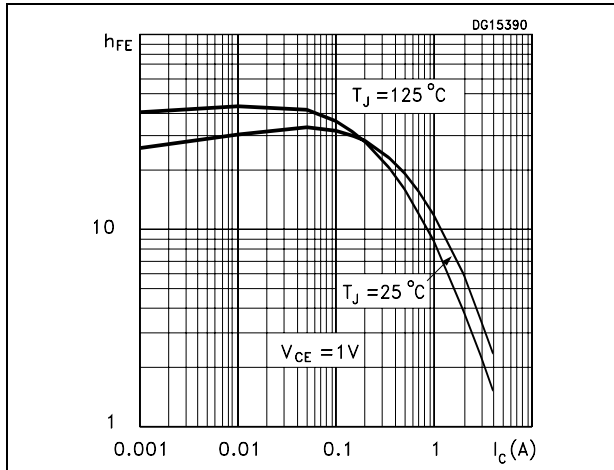


Figure 5. DC current gain PNP ($V_{CE} = -5\text{ V}$)

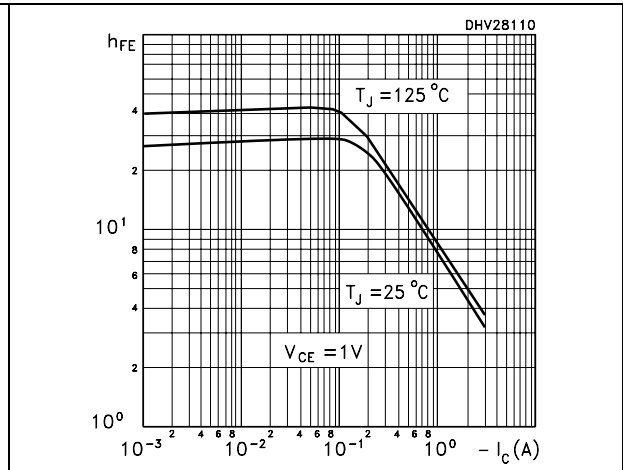


Figure 6. DC current gain NPN ($V_{CE} = 1\text{ V}$)

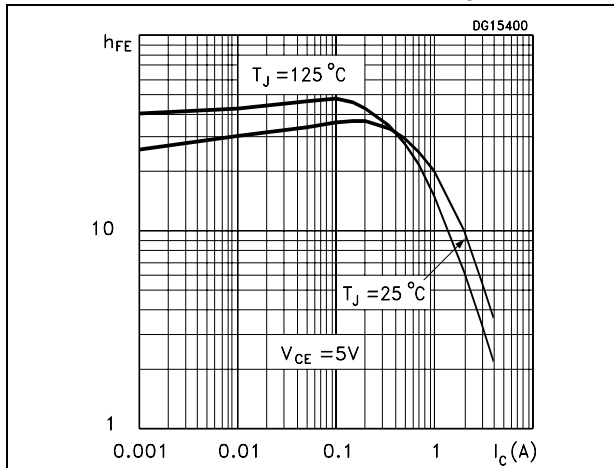


Figure 7. DC current gain PNP ($V_{CE} = -1\text{ V}$)

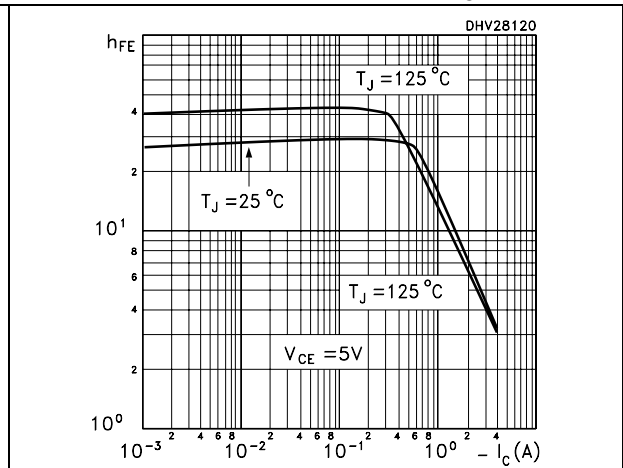


Figure 8. Collector emitter saturation voltage NPN

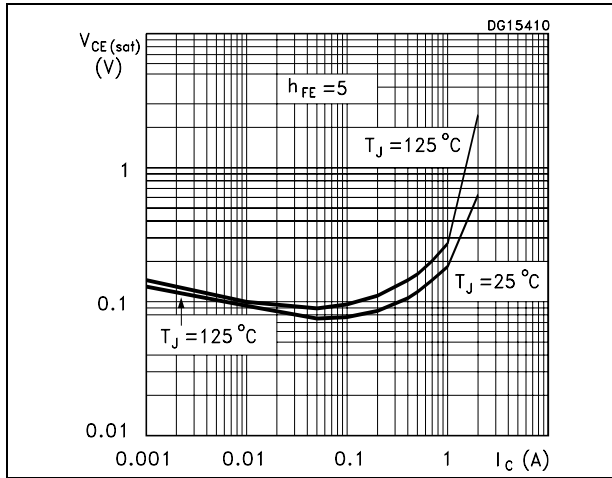


Figure 9. Collector emitter saturation voltage PNP

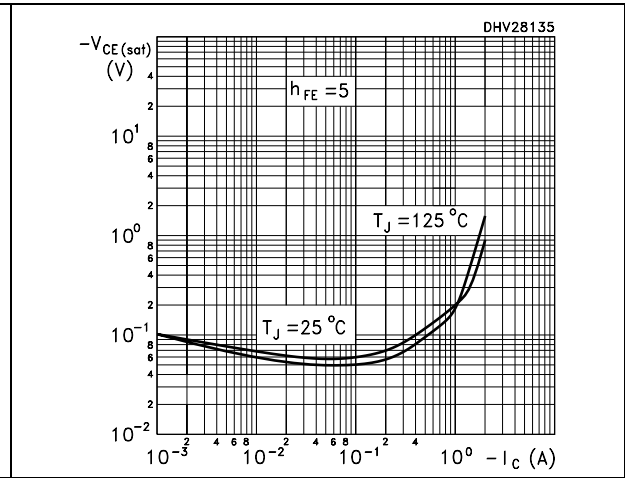


Figure 10. Base emitter saturation voltage NPN

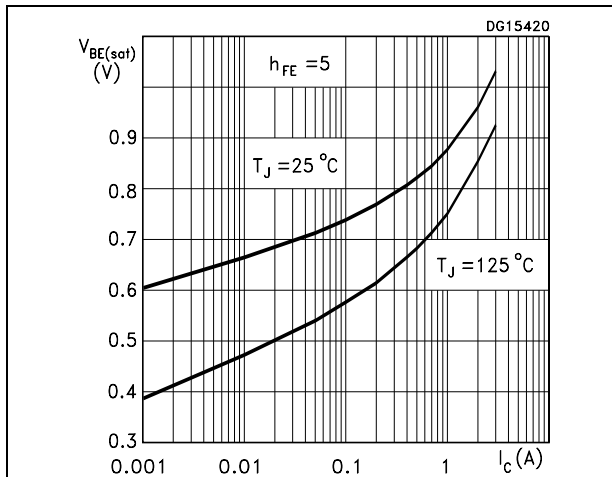


Figure 11. Base emitter saturation voltage PNP

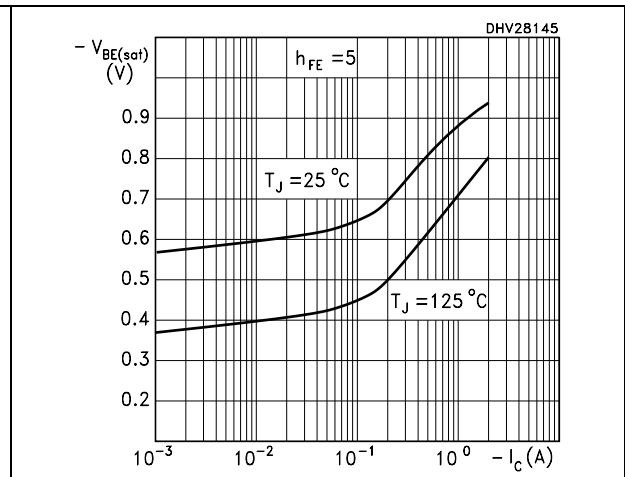


Figure 12. Resistive load fall time NPN

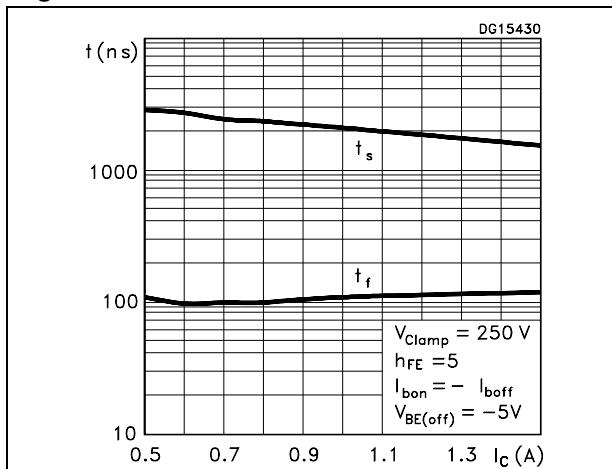


Figure 13. Resistive load fall time PNP

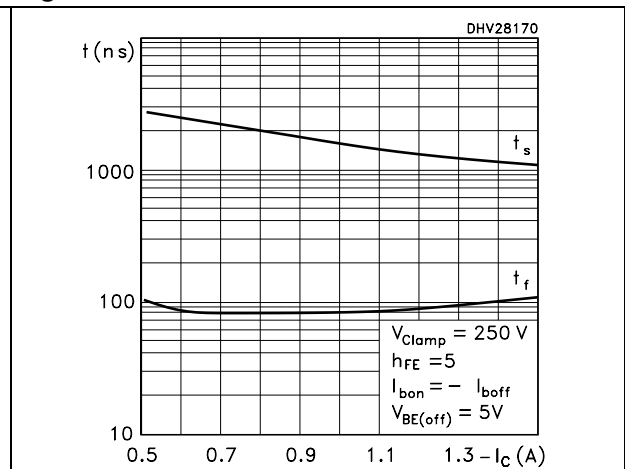


Figure 14. Resistive load storage time NPN

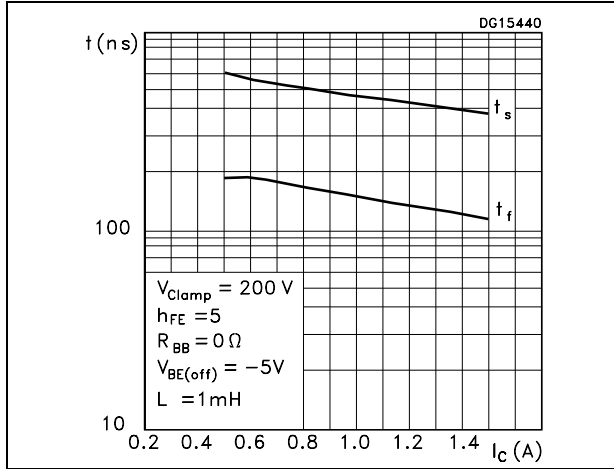


Figure 15. Resistive load storage time PNP

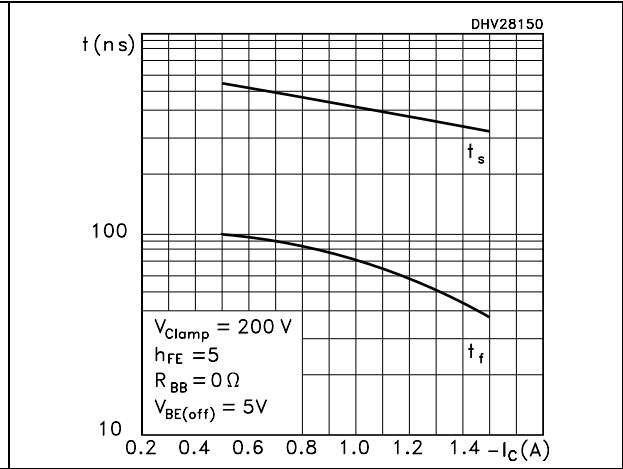


Figure 16. Reverse biased SOA (NPN)

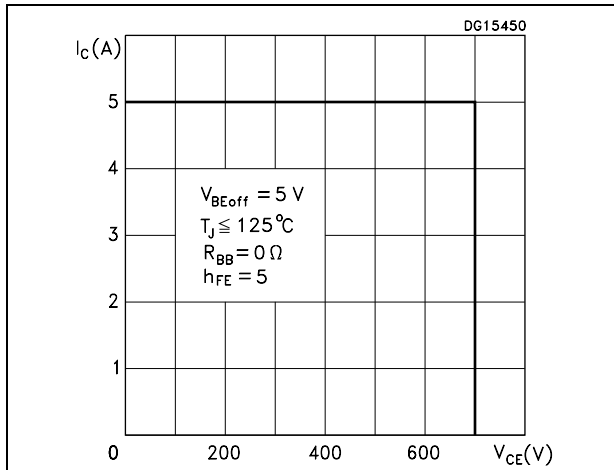
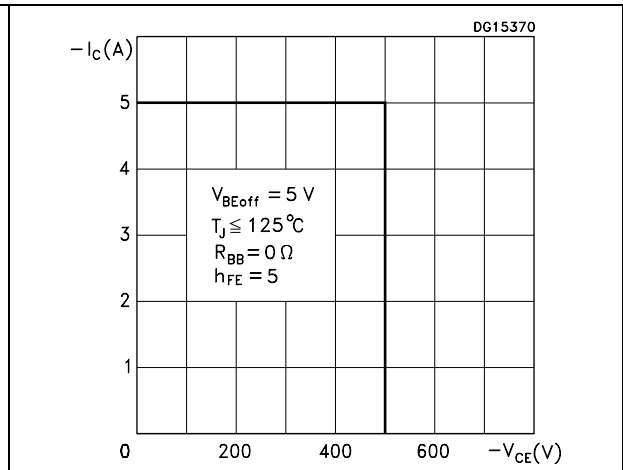


Figure 17. Reverse biased SOA (PNP)



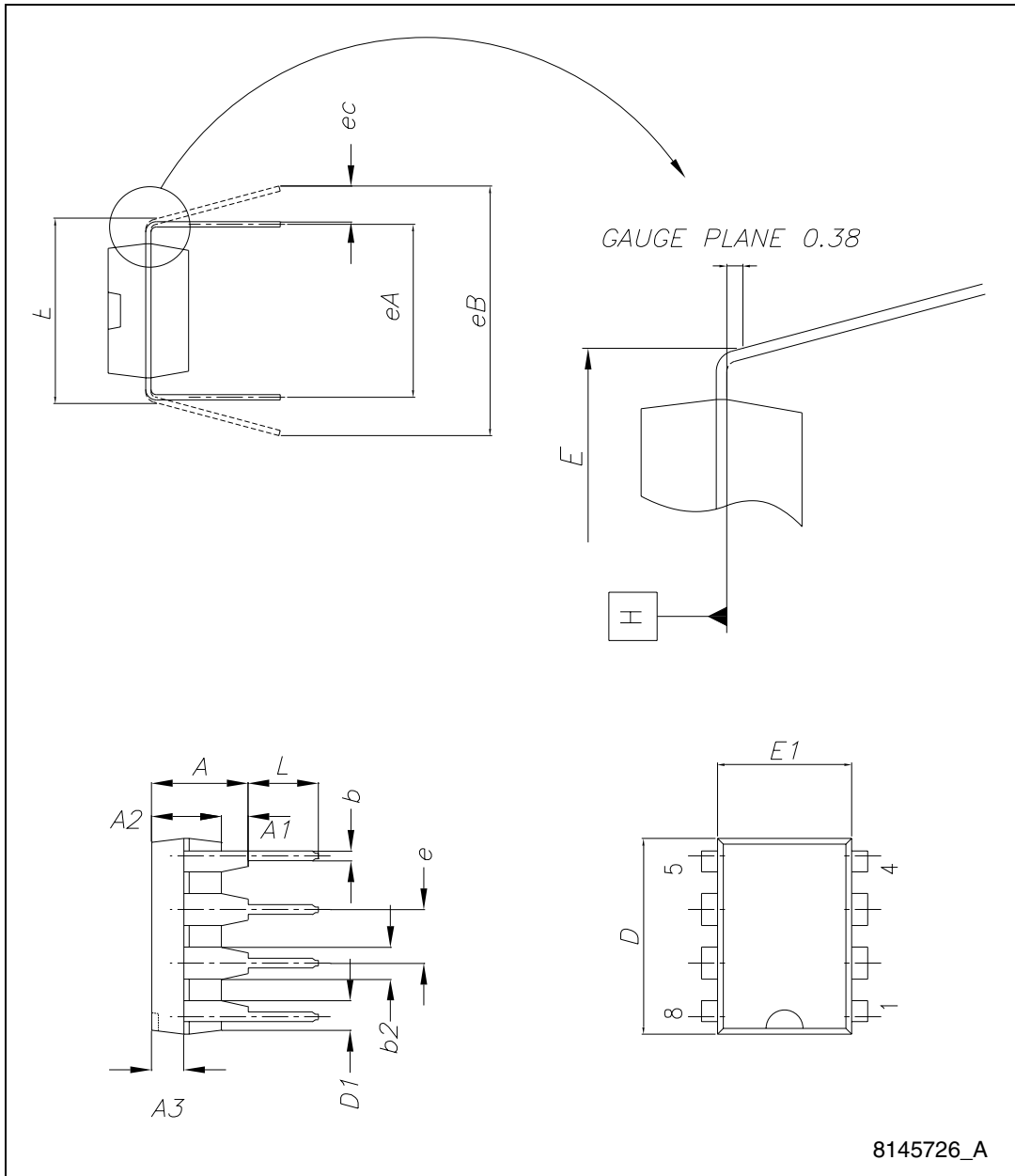
3 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 5. DIP-8 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A			4.80
A1	0.50		
A2	3.10		3.50
A3	1.40		1.60
b	0.38		0.55
b1	0.38		0.51
b2	1.47		1.57
b3	0.89		1.09
c	0.21		0.35
c1	0.20		0.30
D	9.10		9.30
D1	0.13		
E	7.62		8.25
E1	6.25		6.45
e		2.54	
eA		7.62	
eB	7.62		10.90
eC	0		1.52
L	2.92		3.81

Figure 18. Drawing dimension DIP-8



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4 Revision history

Table 6. Document revision history

Date	Revision	Changes
27-May-2009	1	Initial release.
29-Jun-2010	2	Modified: <i>Table 2</i> and <i>Table 3 on page 2</i> , added <i>Section 2.1: Electrical characteristics (curves)</i> .

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