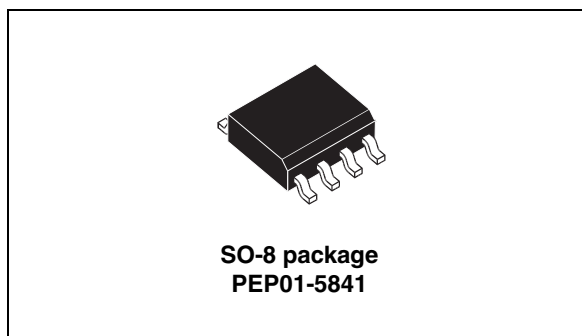


### Features

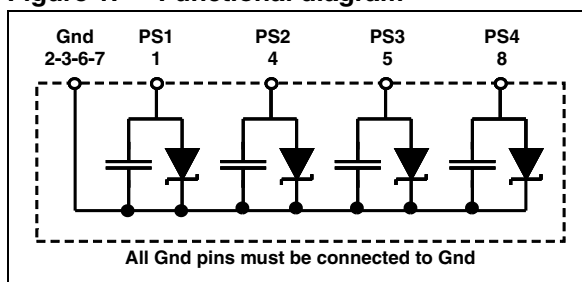
- Peak pulse power: up to 2.7 kW (8/20  $\mu$ s)
- Stand-off voltage: 58 V
- 4 unidirectional Transils™ and 4 decoupling capacitances
- Low clamping voltage: 100 V
- Low leakage current:
  - 0.2  $\mu$ A at 25 °C
  - 1  $\mu$ A at 85 °C
- Operating  $T_j$  max: 150 °C
- JEDEC registered package outline

### Complies with the following standards

- IEC61000-4-2 level 4
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- IEC61000-4-5 level 2
  - $\pm$ 1 kV 42  $\Omega$
- IEEE 802.3af-2003
- IEEE 802.3at-2008



**Figure 1. Functional diagram**



### Description

The PEP01-5841 has been designed to protect power over Ethernet PSE equipment against line overvoltages. It embeds 4 decoupling capacitors to stabilize power supplies.

It is compatible with IEEE 802.3af-2003 and IEEE 802.3at-2008 requirements and it allows PoE based systems to be protected against both electrical overstress (EOS) and electrostatic discharges (ESD) according to IEC61000-4-5 and IEC61000-4-2.

The low clamping voltage (100 V) makes it compatible with PMOS and PSE controller technologies. Developed in Planar technology, it provides high reliability level.

Packaged in SO-8, this minimizes PCB consumption (footprint in accordance with the IPC 7531 standard).

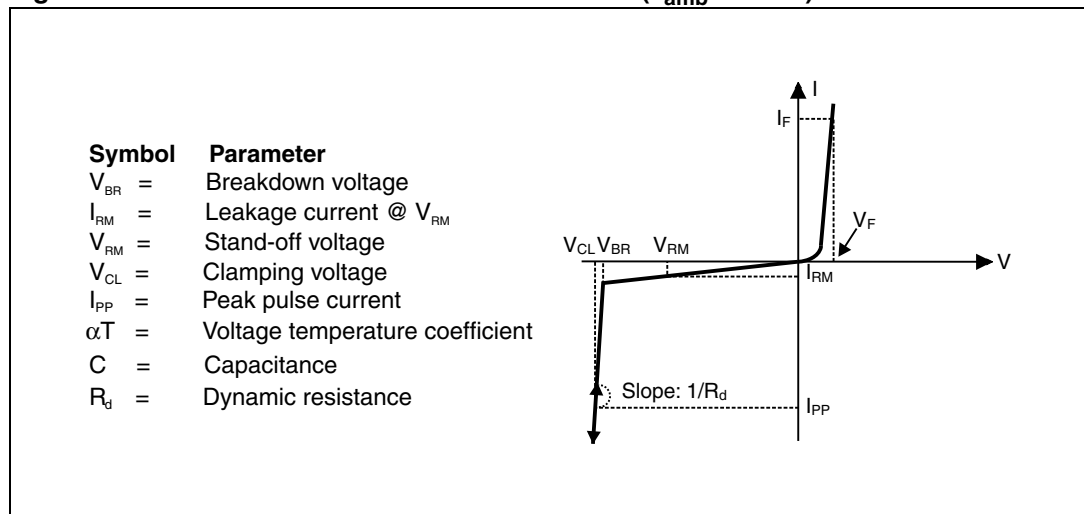
TM: Transil is a trademark of STMicroelectronics

# 1 Characteristics

**Table 1. Absolute ratings ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

Symbol	Parameter	Value	Unit
$V_{PP}$	Peak pulse voltage (IEC61000-4-2 contact discharge)	30	kV
$P_{PP}$	Peak pulse power dissipation	$T_j$ initial = $T_{amb}$ 2700	W
$T_{stg}$	Storage temperature range	-65 to + 150	$^{\circ}\text{C}$
$T_j$	Operating junction temperature range	-55 to + 150	$^{\circ}\text{C}$
$T_L$	Maximum lead temperature for soldering during 10 s.	260	$^{\circ}\text{C}$

**Figure 2. Electrical characteristics - definitions ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**



**Table 2. Electrical characteristics - values ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

Type	$I_{RM}$ max @ $V_{RM}$			$V_{BR}$ @ $I_R$ <sup>(1)</sup>				8/20 $\mu\text{s}$		C	$\alpha T$ <sup>(3)</sup>	
	25 $^{\circ}\text{C}$	85 $^{\circ}\text{C}$		min.	typ.	max.		$V_{CL}$ @ $I_{PP}$	$R_D$ <sup>(2)</sup>			
	$\mu\text{A}$	$\mu\text{A}$	V	V			mA	V	A	$\Omega$	pF	$10^{-4}\text{ }^{\circ}\text{C}$
PEP01-5841	0.2	1	58	64.4	67.8	71.2	1	100	24	1.2	55	10.4

1. Pulse test:  $t_p < 50\text{ ms}$
2. To calculate maximum clamping voltage at other surge level, use the following formula:  
 $V_{CLmax} = R_D \times I_{PP} + V_{BRmax}$
3. To calculate  $V_{BR}$  versus junction temperature, use the following formula:  
 $V_{BR @ T_J} = V_{BR @ 25\text{ }^{\circ}\text{C}} \times (1 + \alpha T \times (T_J - 25))$

Figure 3. Pulse waveform

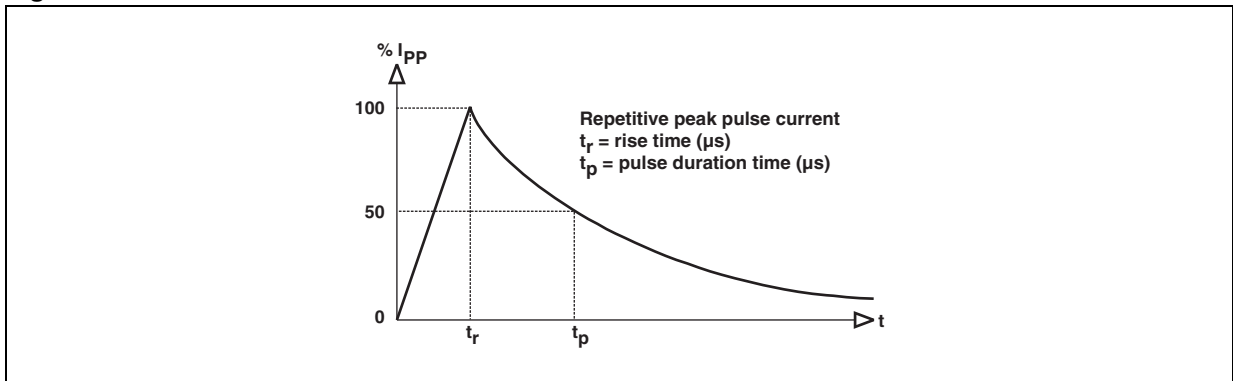


Figure 4. Peak power dissipation versus initial junction temperature

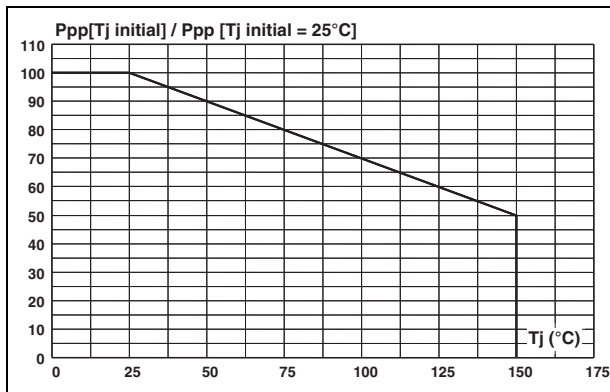


Figure 5. Peak pulse power versus exponential pulse duration ( $T_j$  initial = 25 °C)

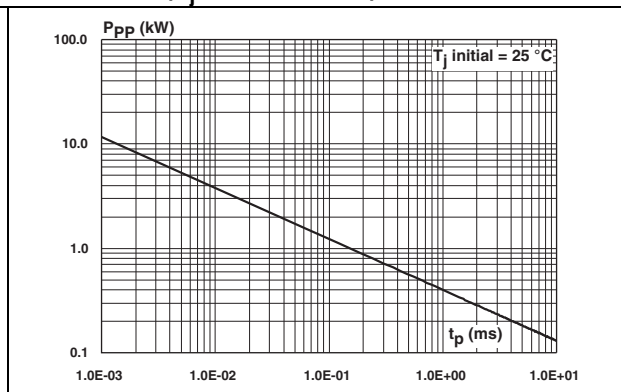


Figure 6. Clamping voltage versus peak pulse current (exponential waveform, maximum values)

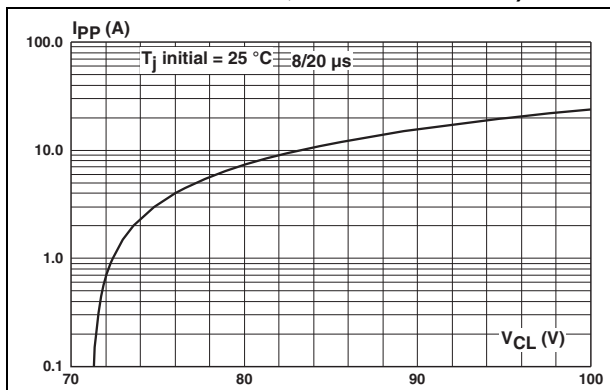
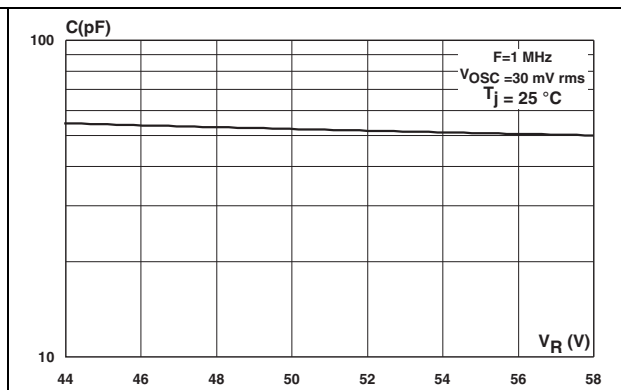
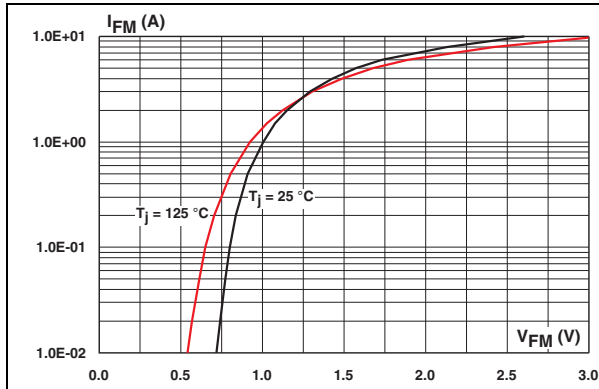


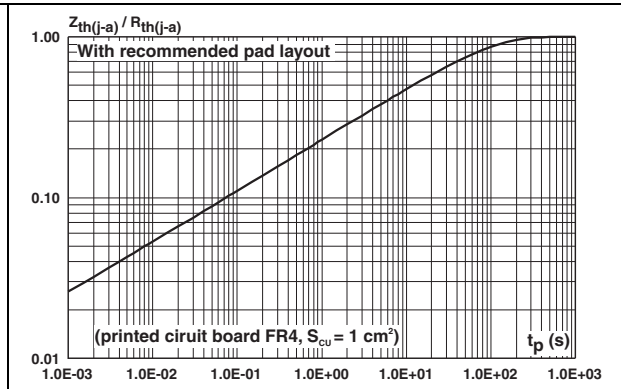
Figure 7. Capacitance versus voltage (typical values)



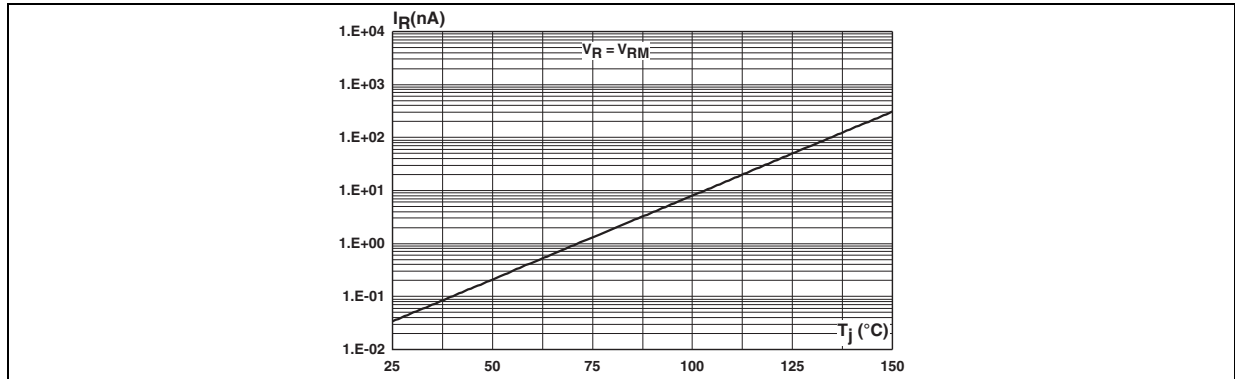
**Figure 8. Peak forward voltage drop versus peak forward current (typical values)**



**Figure 9. Relative variation of thermal impedance junction to ambient versus pulse duration**



**Figure 10. Leakage current versus junction temperature (typical values)**



## 2 Application

Figure 11. Typical application circuit with PMOS integrated in PSE controller

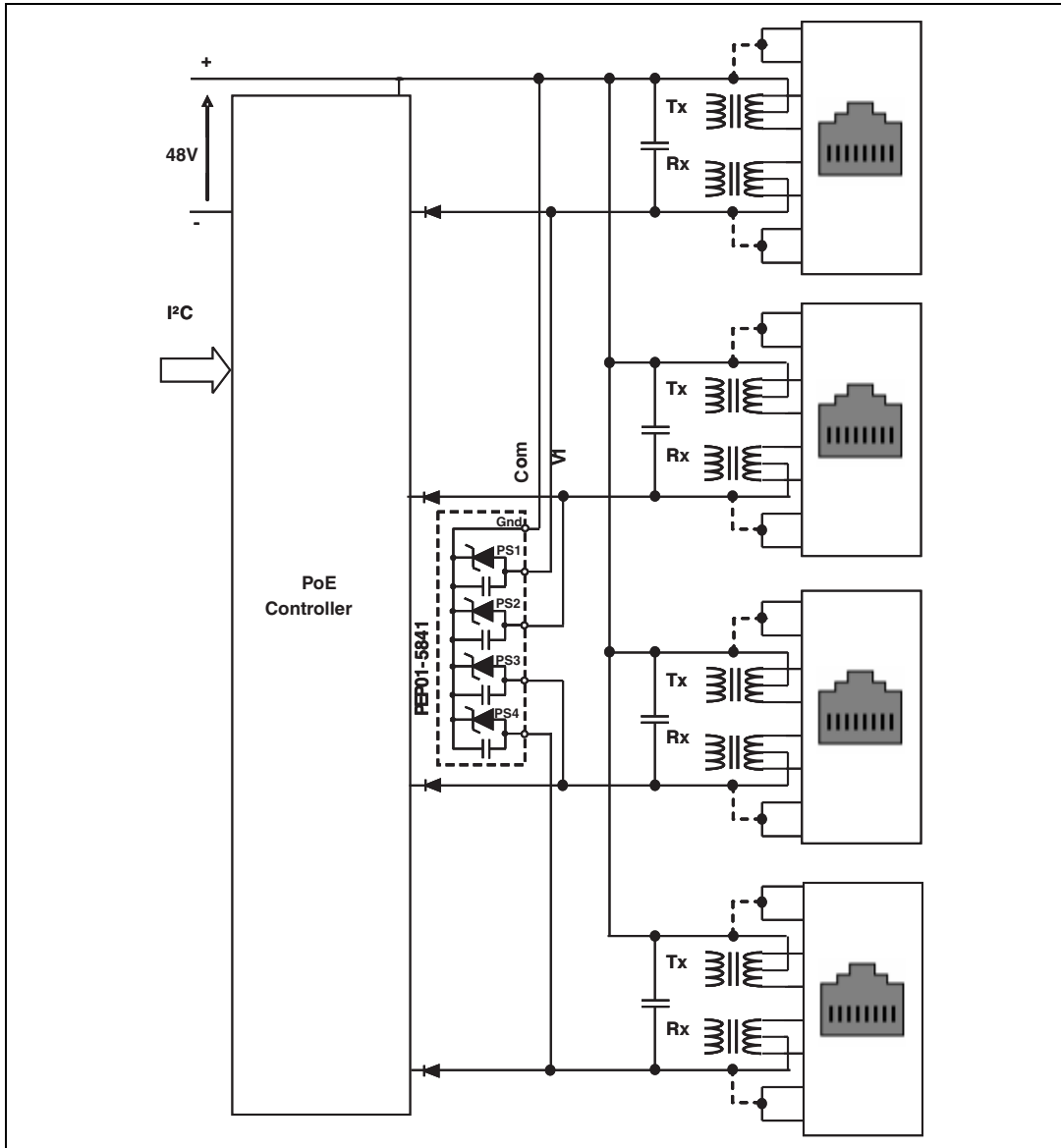


Figure 12. Typical application circuit with external PMOS

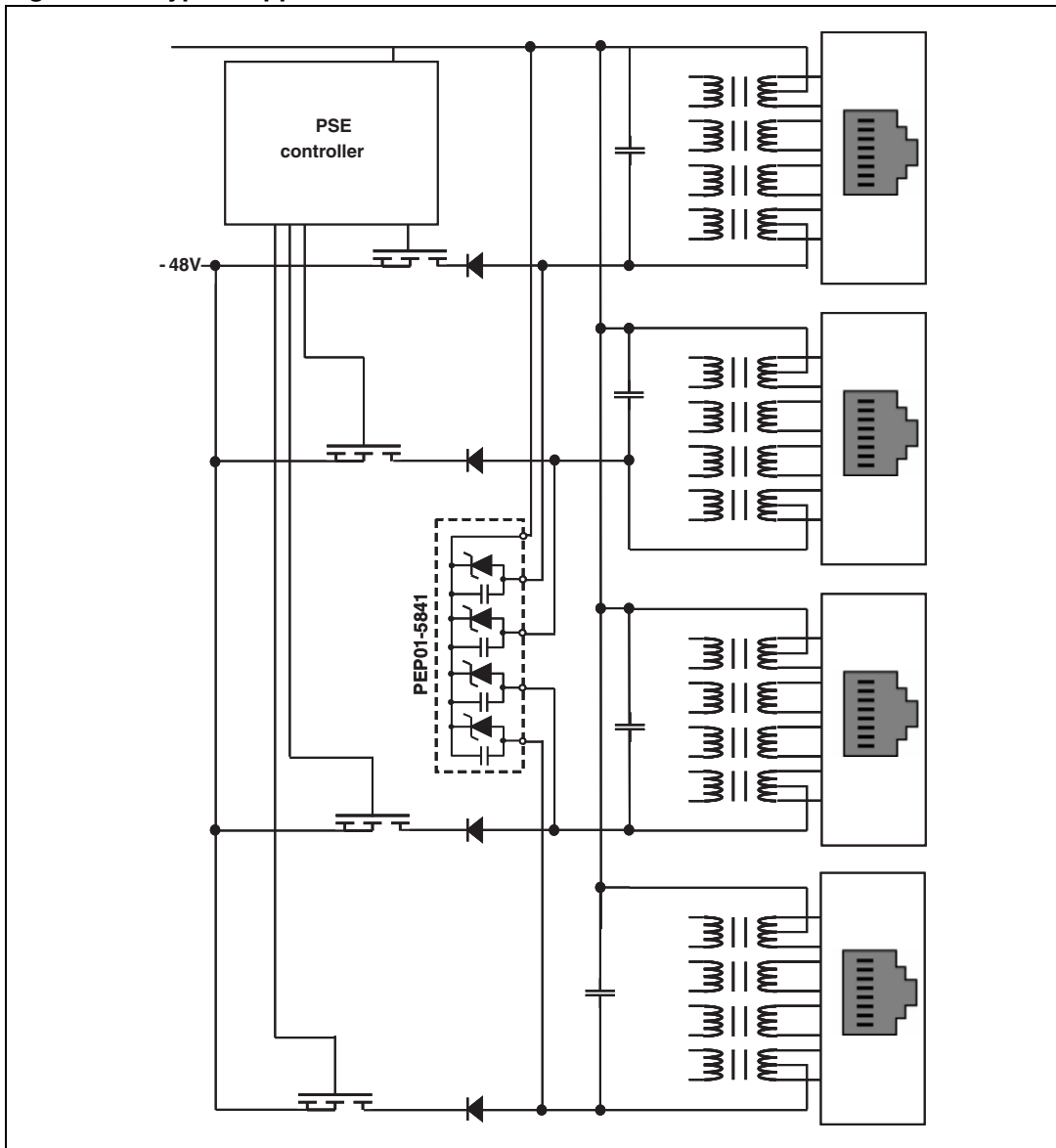
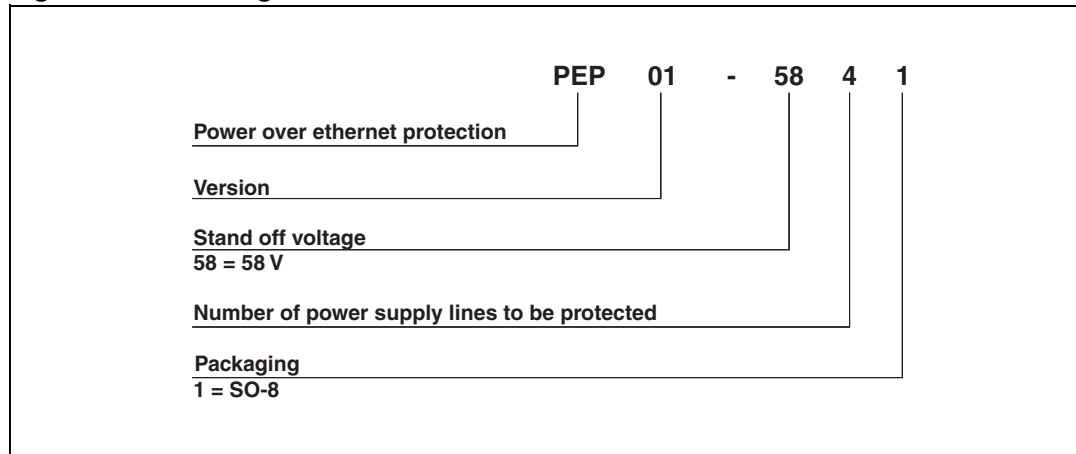


Figure 11 and Figure 12 show typical application schematics of PoE network. Power sourcing equipment (PSE) allows communication and power sourcing for several power devices (PD). The number of ways is generally a multiple of 4, this optimizes the PEP01-5841 for track layout and crosstalk, as well as PCB surface occupation. This protection device has been studied to comply with the latest IEEE 802.3af-2003 requirements and to withstand the surge defined in the IEC 61000-4-5 level 4 requirements.

### 3 Ordering information scheme

Figure 13. Ordering information scheme



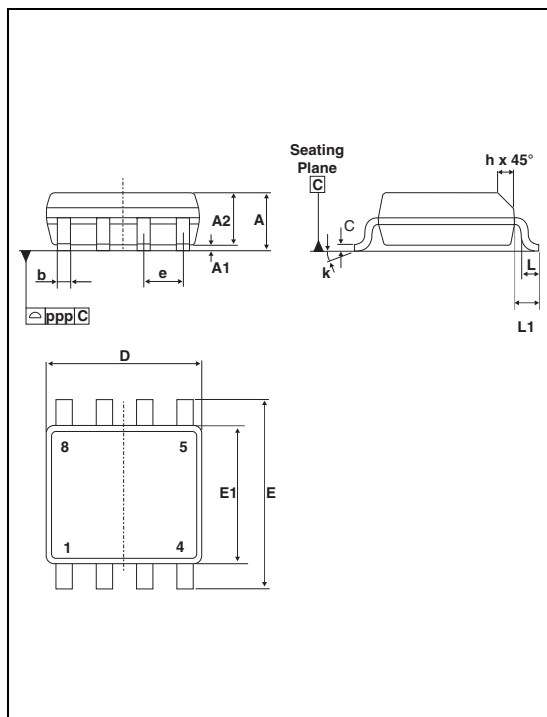
# 4 Package information

- Case: JEDEC SO-8 molded plastic over planar junction
- Terminals: solder plated, solderable according to MIL-STD-750, Method 2026
- Flammability: epoxy is rated UL94V-0
- RoHS package

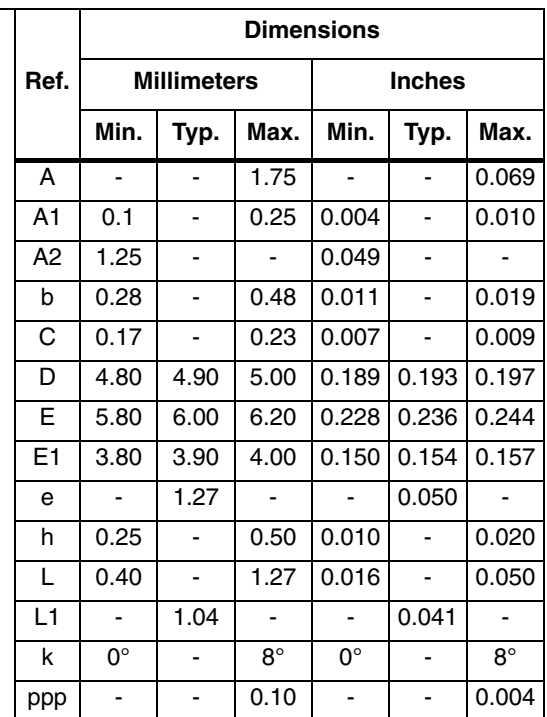
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

**Table 3. SO-8 dimensions**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.75	-	-	0.069
A1	0.1	-	0.25	0.004	-	0.010
A2	1.25	-	-	0.049	-	-
b	0.28	-	0.48	0.011	-	0.019
C	0.17	-	0.23	0.007	-	0.009
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	-	1.27	-	-	0.050	-
h	0.25	-	0.50	0.010	-	0.020
L	0.40	-	1.27	0.016	-	0.050
L1	-	1.04	-	-	0.041	-
k	0°	-	8°	0°	-	8°
ppp	-	-	0.10	-	-	0.004



**Figure 14. Footprint recommendation dimensions in mm (inches)**



**Figure 15. Footprint recommendation for improved clearance dimensions in mm (inches)**

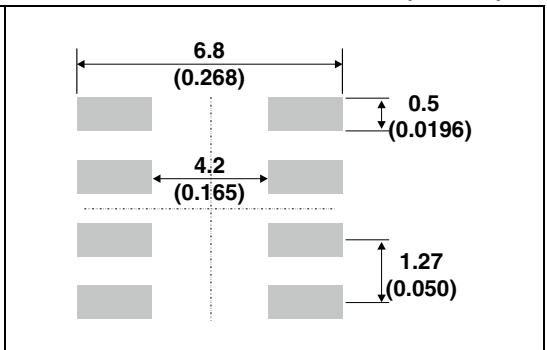
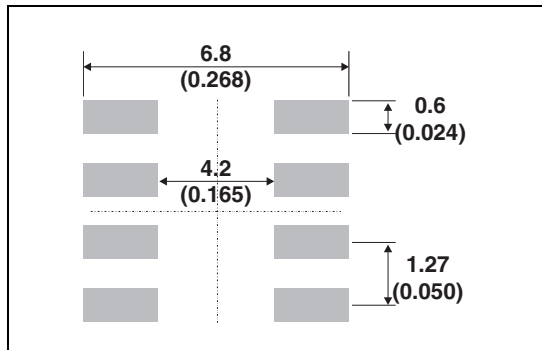
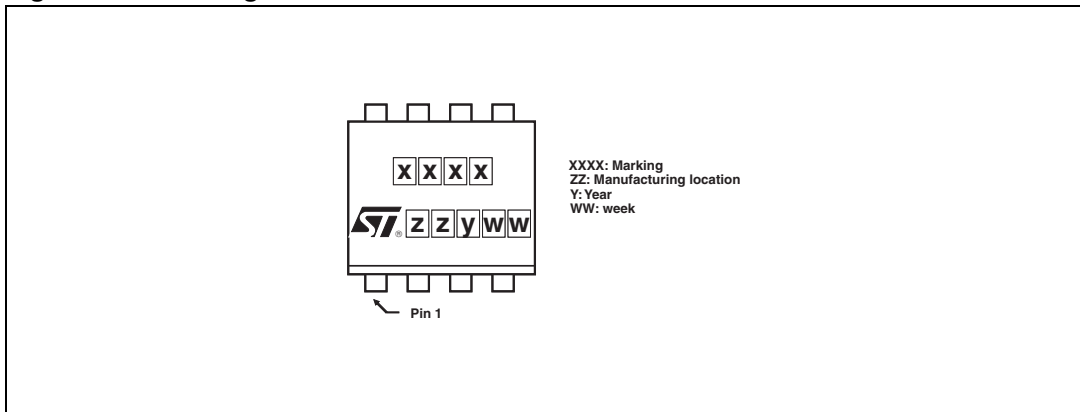


Figure 16. Marking



## 5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
PEP01-5841	58E1	SO-8	78 mg	2000	Tape and reel

## 6 Revision history

Table 5. Document revision history

Date	Revision	Changes
06-May-2009	1	Initial release.
14-May-2009	2	Standards compliance updated.
17-Jan-2013	3	Added note on Gnd pins in <a href="#">Figure 1</a> and added <a href="#">Figure 15</a> .

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