# LCP1521S/LCP152DEE

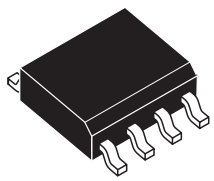
A.S.D.™

## PROGRAMMABLE TRANSIENT VOLTAGE SUPPRESSOR FOR SLIC PROTECTION

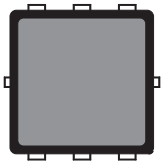
**PRELIMINAY DATASHEET**

### FEATURES

- Dual programmable transient suppressor
- Wide negative firing voltage range: $V_{MGL}$ = -150 V max.
- Low dynamic switching voltages: $V_{FP}$ and $V_{DGL}$
- Low gate triggering current: $I_{GT}$ = 5 mA max
- Peak pulse current: $I_{PP}$ = 30 A (10/1000 µs)
- Holding current: $I_H$ = 150 mA min
- Low space consuming package



**SO-8**
**LCP1521S**



**QFN 3x3**
**LCP152DEE**

### DESCRIPTION

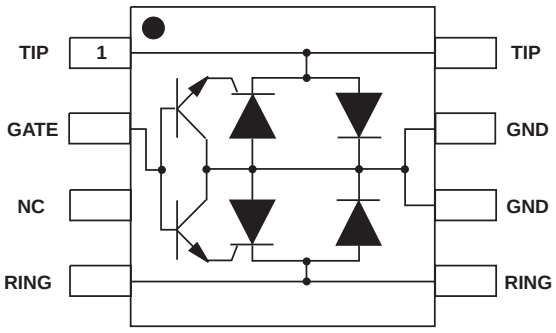
These devices have been especially designed to protect new high voltage, as well as classical SLICs, against transient overvoltages.

Positive overvoltages are clamped by 2 diodes. Negative surges are suppressed by 2 thyristors, their breakdown voltage being referenced to $-V_{BAT}$ through the gate.

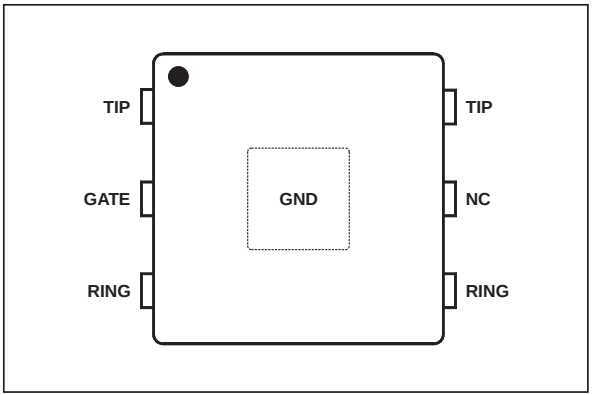
These components present a very low gate triggering current ($I_{GT}$) in order to reduce the current consumption on printed circuit board during the firing phase.

A particular attention has been given to the internal wire bonding. The Kelvin method configuration ensures reliable protection, reducing the overvoltage introduced by the parasitic inductances of the wiring, especially for very fast transients.

### FUNCTIONAL DIAGRAM (LCP1521S)




### FUNCTIONAL DIAGRAM (LCP152DEE)




### BENEFITS

Trisils are not subject to ageing and provide a fail safe mode in short circuit for a better protection. Trisils are used to help equipment to meet various standards such as UL1950, IEC950 / CSA C22.2, UL1459 and FCC part68. Trisils have UL94 V0 resin approved (Trisils are UL497B approved (file: E136224)).

**TM:** ASD is a trademark of STMicroelectronics

## IN COMPLIANCES WITH THE FOLLOWING STANDARDS

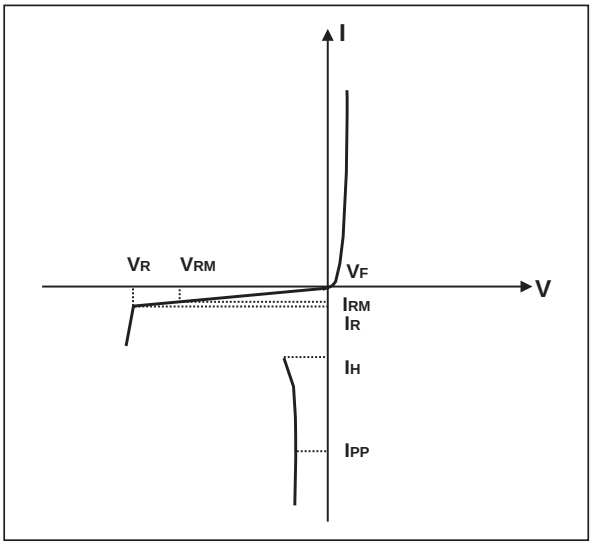
| STANDARD | Peak Surge Voltage (V) | Voltage Waveform | Required peak current (A) | Current Waveform | Minimum serial resistor to meet standard (Ω) |
|---|---|---|---|---|---|
| **GR-1089 Core First level** | 2500<br>1000 | 2/10µs<br>10/1000µs | 500<br>100 | 2/10µs<br>10/1000µs | 10<br>24 |
| **GR-1089 Core Second level** | 5000 | 2/10µs | 500 | 2/10µs | 20 |
| **GR-1089 Core Intra-building** | 1500 | 2/10µs | 100 | 2/10µs | 0 |
| **ITU-T-K20/K21** | 6000<br>1500 | 10/700µs | 150<br>37.5 | 5/310µs | 110<br>0 |
| **ITU-T-K20 (IEC61000-4-2)** | 8000<br>15000 | 1/60 ns | ESD contact discharge<br>ESD air discharge | | 0<br>0 |
| **VDE0433** | 4000<br>2000 | 10/700µs | 100<br>50 | 5/310µs | 60<br>10 |
| **VDE0878** | 4000<br>2000 | 1.2/50µs | 100<br>50 | 1/20µs | 0<br>0 |
| **IEC61000-4-5** | 4000<br>4000 | 10/700µs<br>1.2/50µs | 100<br>100 | 5/310µs<br>8/20µs | 60<br>0 |
| **FCC Part 68, lightning surge type A** | 1500<br>800 | 10/160µs<br>10/560µs | 200<br>100 | 10/160µs<br>10/560µs | 22.5<br>15 |
| **FCC Part 68, lightning surge type B** | 1000 | 9/720µs | 25 | 5/320µs | 0 |

## THERMAL RESISTANCE

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| Rth (j-a) | Junction to ambient | SO-8 | 130 | °C/W |
| | | QFN 3x3 | 170 | |

## ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C)

| Symbol | Parameter |
|---|---|
| $I_{GT}$ | Gate triggering current |
| $I_H$ | Holding current |
| $I_{RM}$ | Reverse leakage current LINE / GND |
| $I_{RG}$ | Reverse leakage current GATE / LINE |
| $V_{RM}$ | Reverse voltage LINE / GND |
| $V_{GT}$ | Gate triggering voltage |
| $V_F$ | Forward drop voltage LINE / GND |
| $V_{FP}$ | Peak forward voltage LINE / GND |
| $V_{DGL}$ | Dynamic switching voltage GATE / LINE |
| $V_{GATE}$ | GATE / GND voltage |
| $V_{RG}$ | Reverse voltage GATE / LINE |
| C | Capacitance LINE / GND |

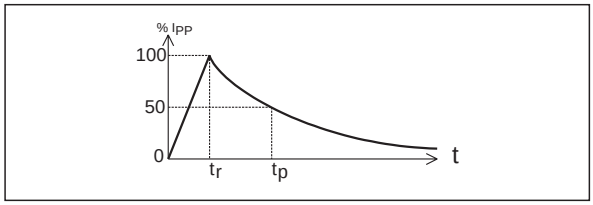


**ABSOLUTE RATINGS** ($T_{amb}$ = 25°C, unless otherwise specified).

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $I_{PP}$ | Peak pulse current (see note1) | 10/1000µs<br>8/20µs<br>10/560µs<br>5/310µs<br>10/160µs<br>1/20µs<br>2/10µs | 30<br>100<br>35<br>40<br>50<br>100<br>170 | A |
| $I_{TSM}$ | Non repetitive surge peak on-state current<br>(50Hz sinusoidal) | t = 10ms<br>t = 1s | 10<br>3 | A |
| $I_{GSM}$ | Maximum gate current<br>(50Hz sinusoidal) | t = 10ms | 2 | A |
| $V_{MLG}$<br>$V_{MGL}$ | Maximum voltage LINE/GND<br>Maximum voltage GATE/LINE | -40°C < Tamb < +85°C<br>-40°C < Tamb < +85°C | -150<br>-150 | V |
| $T_{stg}$<br>Tj | Storage temperature range<br>Maximum junction temperature | | - 55 to + 150<br>150 | °C |
| $T_L$ | Maximum lead temperature for soldering during 10s | | 260 | °C |

**Repetitive peak pulse current**

tr: rise time (µs)
tp: pulse duration (µs)
ex: Pulse waveform 10/1000µs
tr = 10µs tp = 1000µs




**1- PARAMETERS RELATED TO THE DIODE LINE / GND** ($T_{amb}$ = 25°C)

| Symbol | Test conditions | | | Max | Unit |
|---|---|---|---|---|---|
| $V_F$ | $I_F$ = 5A | | t = 500µs | 2 | V |
| $V_{FP}$<br>(note 1) | 10/700µs<br>1.2/50µs<br>2/10µs | 1.5kV<br>1.5kV<br>2.5kV | $R_S$ = 10Ω<br>$R_S$ = 10Ω<br>$R_S$ = 62Ω | 5<br>9<br>30 | V |

Note 1: see test circuit for $V_{FP}$; $R_S$ is the protection resistor located on the line card.

**2 - PARAMETERS RELATED TO THE PROTECTION THYRISTOR** ($T_{amb}$ = 25°C unless otherwise specified)

| Symbol | Test conditions | | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{GT}$ | $V_{GND / LINE}$ = -48V | | 0.1 | 5 | mA |
| $I_H$ | $V_{GATE}$ = -48V (note 2) | | 150 | | mA |
| $V_{GT}$ | at $I_{GT}$ | | | 2.5 | V |
| $I_{RG}$ | $V_{RG}$ = -150V<br>$V_{RG}$ = -150V | Tc=25°C<br>Tc=85°C | | 5<br>50 | µA |
| $V_{DGL}$ | $V_{GATE}$ = -48V (note 3) | | | | |
| | 10/700µs 1.5kV $R_S$ = 10Ω $I_{PP}$ = 30A<br>1.2/50µs 1.5kV $R_S$ = 10Ω $I_{PP}$ = 30A<br>2/10µs 2.5kV $R_S$ = 62Ω $I_{PP}$ = 38A | | | 7<br>10<br>25 | V |

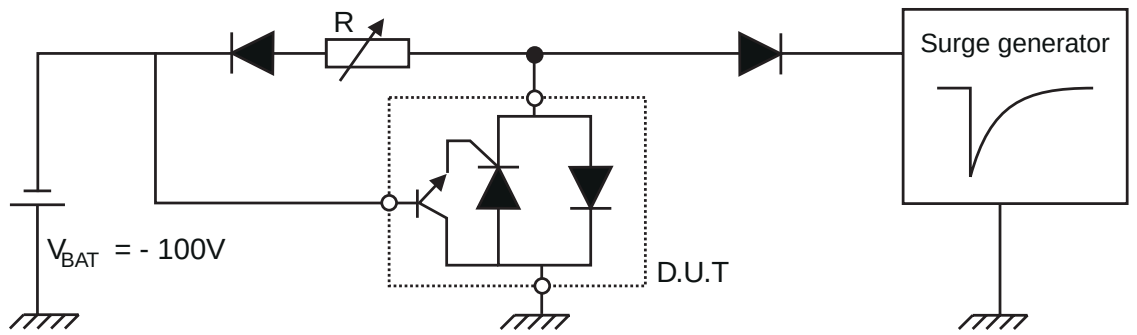
Note 2: see functional holding current ($I_H$) test circuit

Note 3: see test circuit for $V_{DGL}$
The oscillations with a time duration lower than 50ns are not taken into account

**3 - PARAMETERS RELATED TO DIODE AND PROTECTION THYRISTOR** ($T_{amb}$ = 25°C, unless otherwise specified)

| Symbol | Test conditions | | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{RM}$ | $V_{GATE / LINE}$ = -1V $V_{RM}$ = -150V<br>$V_{GATE / LINE}$ = -1V $V_{RM}$ = -150V | Tc=25°C<br>Tc=85°C | | 5<br>50 | µA |
| C | $V_R$ = 50V bias, $V_{RMS}$ = 1V, F = 1MHz<br>$V_R$ = 2V bias, $V_{RMS}$ = 1V, F = 1MHz | | 15<br>35 | | pF |

## FUNCTIONAL HOLDING CURRENT ($I_H$) TEST CIRCUIT : GO-NO GO TEST

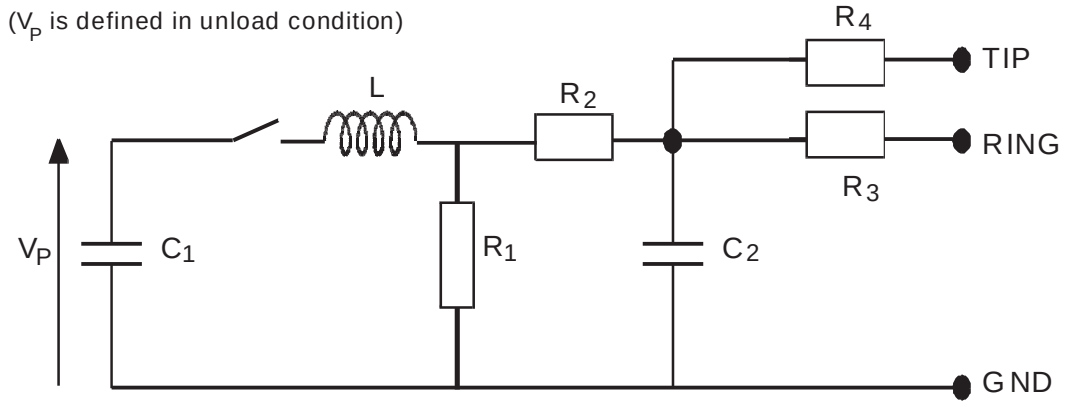



This is a GO-NO GO test which allows to confirm the holding current ($I_H$) level in a functional test circuit.

**TEST PROCEDURE :**

- Adjust the current level at the $I_H$ value by short circuiting the D.U.T.
- Fire the D.U.T. with a surge current : $I_{PP}$ = 10A, 10/1000µs.
- The D.U.T. will come back to the off-state within a duration of 50ms max.

## TEST CIRCUIT FOR $V_{FP}$ AND $V_{DGL}$ PARAMETERS




| Pulse (µs) | | $V_p$ | $C_1$ | $C_2$ | L | $R_1$ | $R_2$ | $R_3$ | $R_4$ | $I_{PP}$ | $R_s$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_r$ | $t_p$ | (V) | (µF) | (nF) | (µH) | (Ω) | (Ω) | (Ω) | (Ω) | (A) | (Ω) |
| 10 | 700 | 1500 | 20 | 200 | 0 | 50 | 15 | 25 | 25 | 30 | 10 |
| 1.2 | 50 | 1500 | 1 | 33 | 0 | 76 | 13 | 25 | 25 | 30 | 10 |
| 2 | 10 | 2500 | 10 | 0 | 1.1 | 1.3 | 0 | 3 | 3 | 38 | 62 |

## TECHNICAL INFORMATION

**Fig. A1:** LCP152 concept behavior.

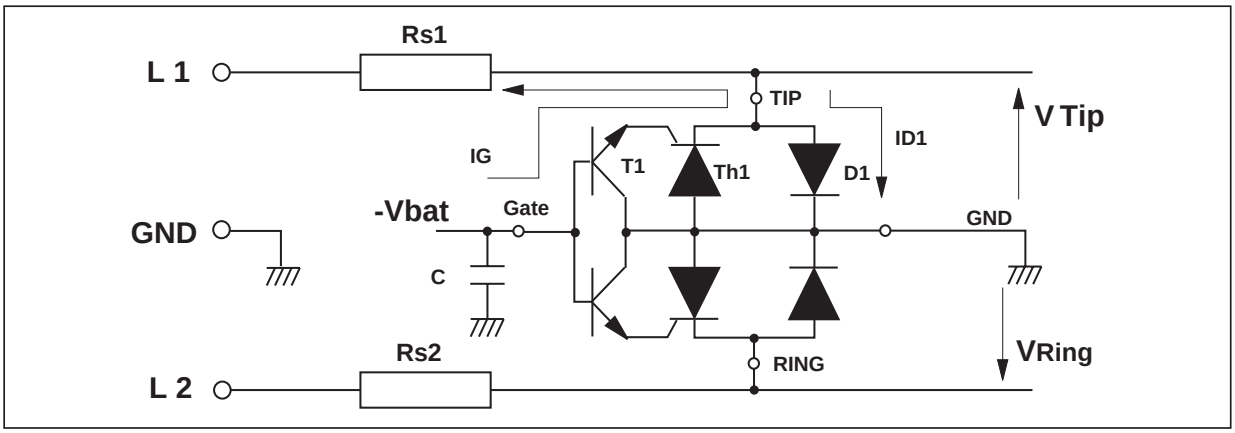
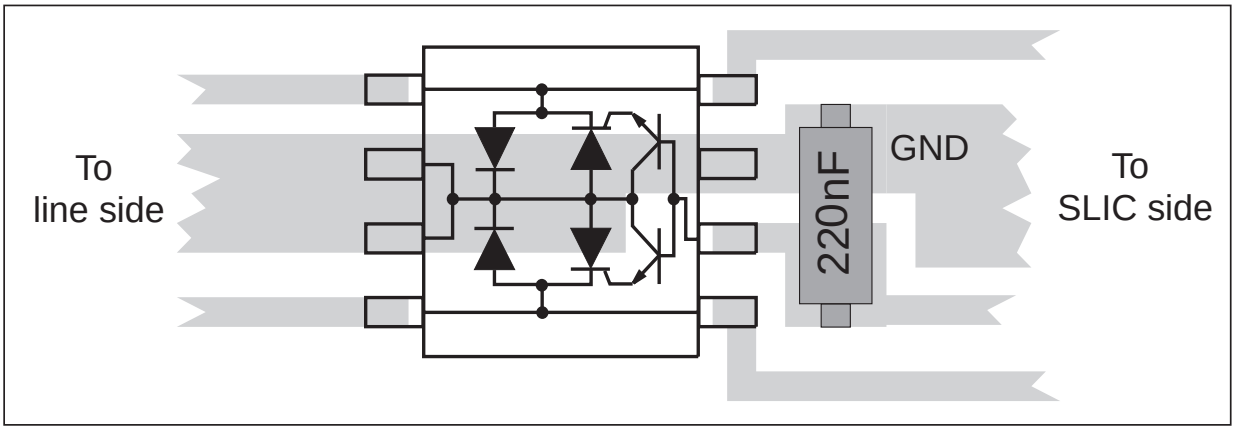



Figure A1 shows the classical protection circuit using the LCP152 crowbar concept. This topology has been developed to protect the new high voltage SLIC's. It allows to program the negative firing threshold while the positive clamping value is fixed at GND.

When a negative surge occurs on one wire (L1 for example) a current IG flows through the base of the transistor T1 and then injects a current in the gate of the thyristor Th1. Th1 fires and all the surge current flows through the ground. After the surge when the current flowing through Th1 becomes less negative than the holding current $I_H$, then Th1 switches off.

When a positive surge occurs on one wire (L1 for example) the diode D1 conducts and the surge current flows through the ground.

**Fig. A2:** Example of PCB layout based on LCP152 protection.




In order to minimize the remaining voltage across the SLIC inputs during the surge, the TIP and RING pins of the LCP152 are doubled (Pins 1 and 8 for TIP / Pins 4 and 5 for RING).
This fact allows the board designer to connect the tracks like in figure A2. With such a PCB design, the extra voltages caused by track stray inductance remain located on the line side of the LCP and do not affects the SLIC side.
The capacitor C is used to speed up the crowbar structure firing during the fast surge edges.
This allows to minimize the dynamical breakover voltage at the SLIC Tip and Ring inputs during fast strikes. Note that this capacitor is generally present around the SLIC - Vbat pin.
So to be efficient it has to be as close as possible from the LCP152 Gate pin and from the reference ground track (or plan) (see Fig. A2). The optimized value for C is 220nF.

The series resitors Rs1 and Rs2 designed in figure A1 represent the fuse resistors or the PTC which are mandatory to withstand the power contact or the power induction tests imposed by the various country standards. Taking into account this fact the actual lightning surge current flowing through the LCP is equal to:

I surge = V surge / (Rg + Rs)

With V surge = peak surge voltage imposed by the standard.
Rg = series resistor of the surge generator
Rs = series resistor of the line card (e.g. PTC)

e.g. For a line card with 30Ω of series resistors which has to be qualified under GR1089 Core 1000V 10/1000µs surge, the actual current through the LCP152 is equal to:

I surge = 1000 / (10 + 30) = **25A**

The LCP152 is particularly optimized for the new telecom applications such as the fiber in the loop, the WLL, the remote central office. In this case, the operating voltages are smaller than in the classical system. This makes the high voltage SLICs particularly suitable. The schematics of figure A3 gives the most frequent topology used for these applications.

**Fig. A3:** Protection of high voltage SLIC.

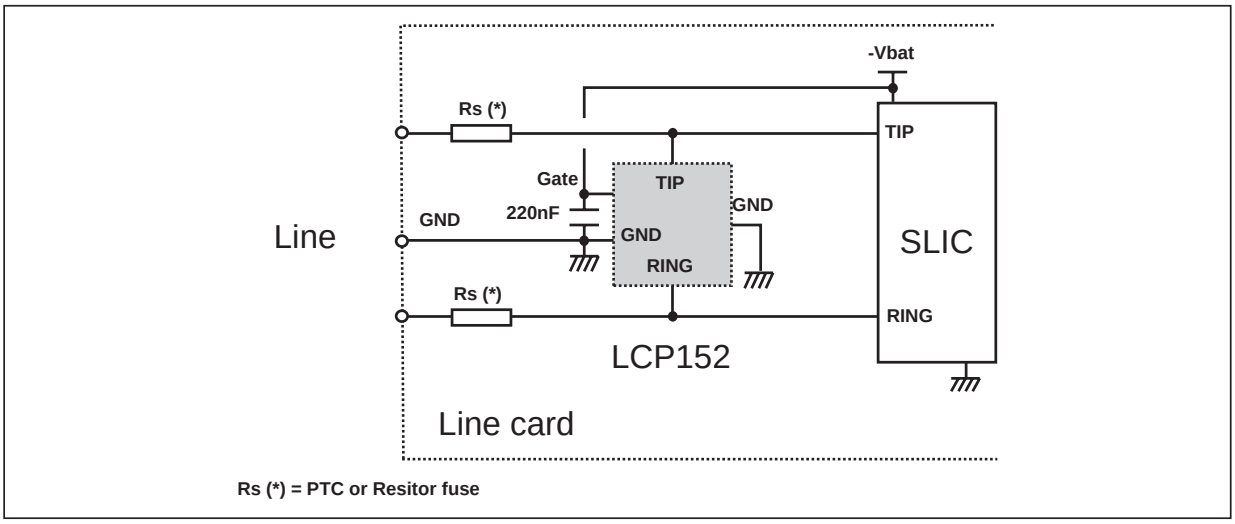
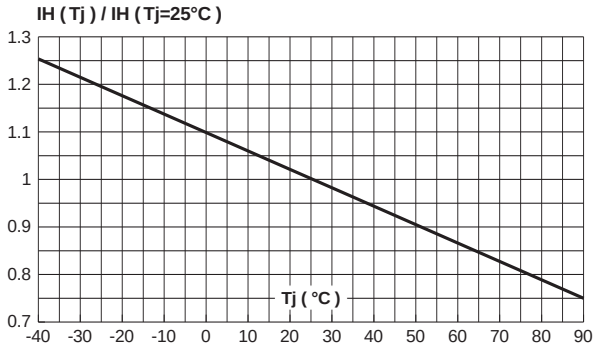


**Fig. 1:** Surge peak current versus overload duration.

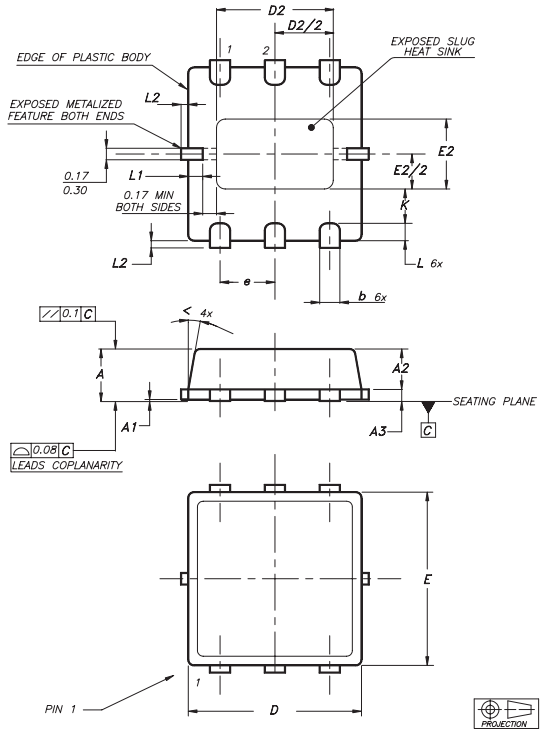
**TO BE DEFINED**

**Fig. 2:** Relative variation of holding current versus junction temperature




## PACKAGE MECHANICAL DATA

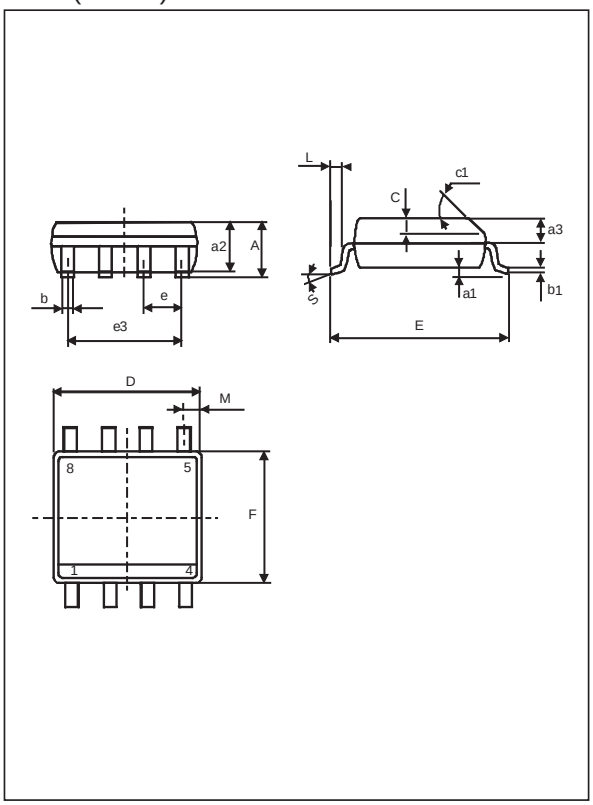
QFN 3x3 (6 Leads)




| REF. | DIMENSIONS | | | | | |
|---|---|---|---|---|---|---|
| | Millimetres | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.80 | | 1 | 0.031 | | 0.040 |
| A1 | 0 | | 0.05 | 0 | | 0.002 |
| A2 | 0.65 | | 0.75 | 0.026 | | 0.030 |
| A3 | | 20 | | | 0.787 | |
| b | 0.33 | | 0.43 | 0.013 | | 0.017 |
| D | 2.90 | 3 | 3.10 | 0.114 | 0.118 | 0.122 |
| D2 | 1.92 | | 2.12 | 0.076 | | 0.083 |
| E | 2.90 | 3 | 3.10 | 0.114 | 0.118 | 0.122 |
| E2 | 1.11 | | 1.31 | 0.044 | | 0.051 |
| e | | 0.95 | | | 0.037 | |
| L | 0.20 | | 0.45 | 0.008 | | 0.018 |
| L1 | | 0.24 | | | 0.009 | |
| L2 | | | 0.13 | | | 0.005 |
| K | 0.20 | | | 0.008 | | |
| < | 0° | | 12° | 0° | | 12° |

## PACKAGE MECHANICAL DATA

SO-8 (Plastic)




| REF. | DIMENSIONS | | | | | |
|---|---|---|---|---|---|---|
| | Millimetres | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 1.75 | | | 0.069 |
| a1 | 0.1 | | 0.25 | 0.004 | | 0.010 |
| a2 | | | 1.65 | | | 0.065 |
| a3 | 0.65 | | 0.85 | 0.025 | | 0.033 |
| b | 0.35 | | 0.48 | 0.014 | | 0.019 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | 0.25 | 0.50 | 0.50 | 0.010 | | 0.020 |
| c1 | 45° (typ) | | | | | |
| D | 4.8 | | 5.0 | 0.189 | | 0.197 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 3.81 | | | 0.150 | |
| F | 3.8 | | 4.0 | 0.15 | | 0.157 |
| L | 0.4 | | 1.27 | 0.016 | | 0.050 |
| M | | | 0.6 | | | 0.024 |
| S | 8° (max) | | | | | |

| Order code | Marking | Package | Weight | Base qty | Delivery mode |
|---|---|---|---|---|---|
| LCP1521S | CP152S | SO-8 | 0.08 g | 100 | Tube |
| LCP1521SRL | CP152S | SO-8 | 0.08 g | 2500 | Tape & Reel |
| LCP152DEERL | CP15 | QFN 3x3 | 0.022 g | 3000 | Tape & Reel |