

High voltage resonant controller

- High voltage rail up to 600 V
- dV/dt immunity ± 50 V/ns in full temperature range
- Driver current capability: 250 mA source
450 mA sink
- Switching times 80/40 ns rise/fall with 1 nF load
- CMOS shutdown input
- Undervoltage lock-out
- Soft-start frequency shifting timing
- Sense op amp for closed loop control or protection features
- High accuracy current controlled oscillator
- Integrated bootstrap diode
- Clamping on Vs
- SO16, DIP16 packages



The device is manufactured with the BCD OFF LINE technology, able to ensure voltage ratings up to 600 V, making it perfectly suited for AC/DC Adapters and wherever a resonant topology can be beneficial. The device is intended to drive two power MOSFET, in the classical half bridge topology. A dedicated timing section allows the designer to set soft start time, soft start and minimum frequency. An error amplifier, together with the two enable inputs, are made available. In addition, the integrated bootstrap diode and the zener clamping on low voltage supply, reduces to a minimum the external parts needed in the applications.

The diagram illustrates the internal architecture of the AM02284-01 motor driver. It features a central CONTROL LOGIC block that interfaces with a VCO (Voltage-Controlled Oscillator) and a DEAD TIME block. The CONTROL LOGIC also manages the DRIVING LOGIC, which in turn controls the LVG DRIVER and the HVG DRIVER. The LVG DRIVER is connected to the LVG pin (pin 11) and the BOOTSTRAP DRIVER. The HVG DRIVER is connected to the HVG pin (pin 15) and the BOOTSTRAP DRIVER. The BOOTSTRAP DRIVER is connected to the V_BOOT pin (pin 16) and the OUT pin (pin 14). The OUT pin is connected to the LOAD. The OP AMP (Operational Amplifier) is connected to the OPIN+ (pin 7) and OPIN- (pin 6) pins, with its output (pin 5) connected to the OPAMP pin (pin 5). The UV DETECTION block is connected to the V_S pin (pin 12). The CONTROL LOGIC also interfaces with the EN1 (pin 8) and EN2 (pin 9) pins via Vthe1 and Vthe2 comparators. The CONTROL LOGIC is also connected to the VCO, which is connected to the Rfmin (pin 4) and Rfstart (pin 2) pins. The VCO is also connected to the C_T pin (pin 3). The CONTROL LOGIC is connected to the C_SS pin (pin 1) via the I_SS pin (pin 1).

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1 Maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
IS	Supply current at $V_{cl}^{(1)}$	25	mA
VLVG	Low side output	14.6	V
VOU	High side reference	-1 to VBOOT -18	V
VHVG	High side output	-1 to VBOOT	V
VBOOT	Floating supply voltage	618	V
dVBOOT/dt	VBOOT pin slew rate (repetitive)	±50	V/ns
dVOU/dt	OUT pin slew rate (repetitive)	±50	V/ns
Vir	Forced input voltage (pins Rfmin, Rfstart)	-0.3 to 5	V
Vic	Forced input voltage (pins Css, Cf)	-0.3 to 5	V
VEN1, VEN2	Enable input voltage	-0.3 to 5	V
IEN1, IEN2	Enable input current	±3	mA
Vopc	Sense op amp common mode range	-0.3 to 5	V
Vopd	Sense op amp differential mode range	-5 to 5	V
Vopo	Sense op amp output voltage (forced)	4.6	V
Tstg	Storage temperature	-40 to +150	°C
Tj	Junction temperature	-40 to +150	°C
Tamb	Ambient temperature	-40 to +125	°C

1. The device is provided of an internal clamping zener between GND and the Vs pin, It must not be supplied by a low impedance voltage source.

Note: ESD immunity for pins 14, 15 and 16 is guaranteed up to 900 (human body model).

Table 2. Thermal data

Symbol	Parameter	SO16N	DIP16	Unit
R _{thJA}	Thermal resistance junction to ambient	120	80	°C/W

Table 3. Recommended operating conditions

Symbol	Parameter	Value	Unit
V _S	Supply voltage	10 to V _{cl}	V
V _{out} ⁽¹⁾	High side reference	-1 to Vboot-V _{cl}	V
V _{boot} ⁽¹⁾	Floating supply rail	500	V
f _{max}	Maximum switching frequency	400	kHz

1. If the condition V_{boot} - V_{out} < 18 is guaranteed, V_{out} can range from -3 to 580 V.

2 Electrical characteristics

$V_S = 12\text{ V}$; $V_{\text{BOOT}} - V_{\text{OUT}} = 12\text{ V}$; $T_A = 25\text{ }^\circ\text{C}$

Table 4. Electrical characteristics

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltage							
V _{suvp}	12	V _S turn on threshold		10	10.7	11.4	V
V _{suvn}		V _S turn off threshold		7.3	8	8.7	V
V _{suvh}		Supply voltage under voltage hysteresis			2.7		V
V _{cl}		Supply voltage clamping		14.6	15.6	16.6	V
I _{su}		Start up current	V _S < V _{suvn}			250	μA
I _q		Quiescent current, f _{out} = 60 kHz, no load	V _S > V _{suvp}		2	3	mA
High voltage section							
I _{bootleak}	16	BOOT pin leakage current	V _{BOOT} = 580 V			5	μA
I _{outleak}	14	OUT pin leakage current	V _{OUT} = 562 V			5	μA
R _{DSon}	16	Bootstrap driver on resistance		100	150	300	Ω
High/low side drivers							
I _{hvgso}	15	High side driver source current	V _{HVG} -V _{OUT} = 0	170	250		mA
I _{hvg si}		High side driver sink current	V _{HVG} -V _{BOOT} = 0	300	450		mA
I _{lvgs o}	11	Low side driver source current	V _{LVG} -GND = 0	170	250		mA
I _{lvgs i}		Low side driver sink current	V _{LVG} -V _S = 0	300	450		mA
t _{rise}	15,11	Low/high side output rise time	C _{load} = 1nF		80	120	ns
t _{fall}				C _{load} = 1nF		40	80
Oscillator							
DC	14	Output duty cycle		48	50	52	%
f _{min}		Minimum output oscillation frequency	C _f = 470pF; R _{fmin} = 50kΩ	58.2	60	61.8	kHz
f _{start}		Soft start output oscillation frequency	C _f = 470pF; R _{fmin} = 50kΩ; R _{fstart} = 47kΩ	114	120	126	kHz

Table 4. Electrical characteristics (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{ref}	2, 4	Voltage to current converters threshold		1.9	2	2.1	V
t_d	14	Dead time between low and high side conduction		0.2	0.27	0.35	μs
IVref	2, 4	Reference current		120			μA
Timing section							
k_{ss}	1	Soft start timing constant	$C_{ss} = 330nF$	0.115	0.15	0.185	s/ μF
Sense op amp							
I_{IB}	6, 7	Input bias current				0.1	μA
V_{io}		Input offset voltage		-10		10	mV
R_{out}	5	Output resistance		200		300	?
I_{out-}		Source output current	$V_{out} = 4.5V$	1			mA
I_{out+}		Sink output current	$V_{out} = 0.2V$	1			mA
V_{ic}	6,7	Op amp input common mode range		-0.2		3	V
GBW		Sense op amp gain band width product ⁽¹⁾		0.5	1		MHz
Gdc		DC open loop gain		60	80		dB
Comparators							
V_{the1}	8	Enabling comparator threshold		0.56	0.6	0.64	V
V_{the2}	9	Enabling comparator threshold		1.05	1.2	1.35	V
t_{pulse}	8,9	Minimum pulse length				200	ns

1. Guaranteed by design

3 Pin connections

Figure 2. Pin connections

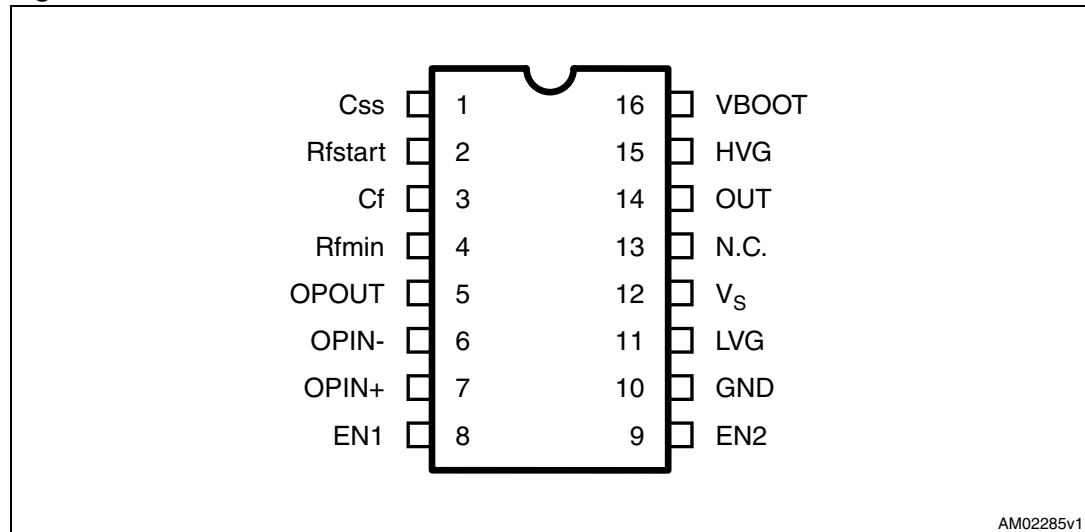


Table 5. Pin description

Pin n°	Name	Function
1	CSS	Soft start timing capacitor
2	R _{fstart}	Soft start frequency setting - low impedance voltage source -see also C _f
3	C _f	Oscillator frequency setting - see also R _{fmin} , R _{fstart}
4	R _{fmin}	Minimum oscillation frequency setting - low impedance voltage source - see also C _f
5	O _{Pout}	Sense op amp output - low impedance
6	O _{Pon-}	Sense op amp inverting input -high impedance
7	O _{Pon+}	Sense op amp non inverting input - high impedance
8	EN1	Half bridge latched enable
9	EN2	Half bridge unlatched enable
10	GND	Ground
11	LVG	Low side driver output
12	V _s	Supply voltage with internal zener clamp
13	N.C.	Not connected
14	OUT	High side driver reference
15	HVG	High side driver output
16	V _{boot}	Bootstrapped supply voltage

4 Timing diagram

Figure 3. EN2 timing diagrams

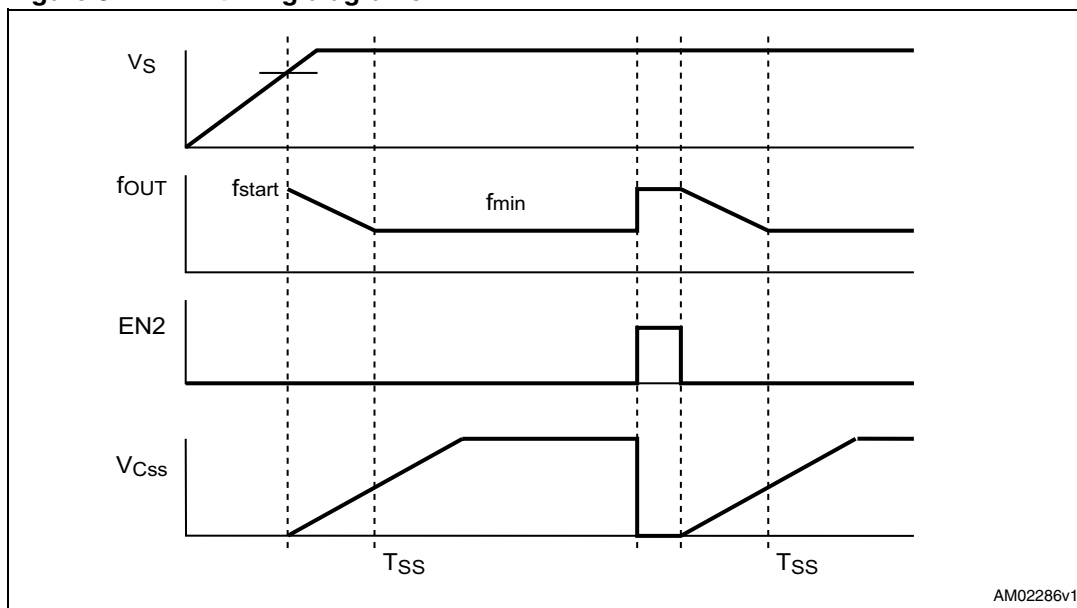


Figure 4. EN1 timing diagrams

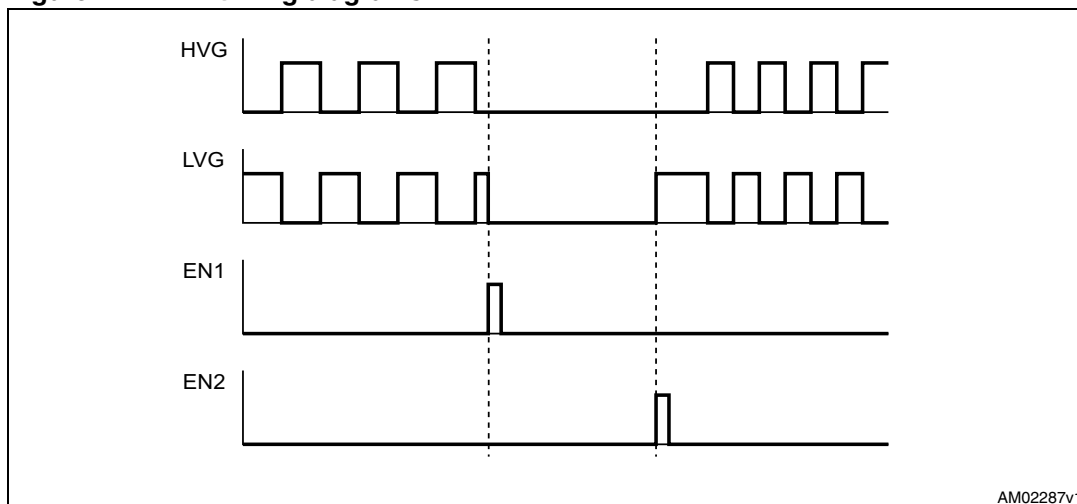
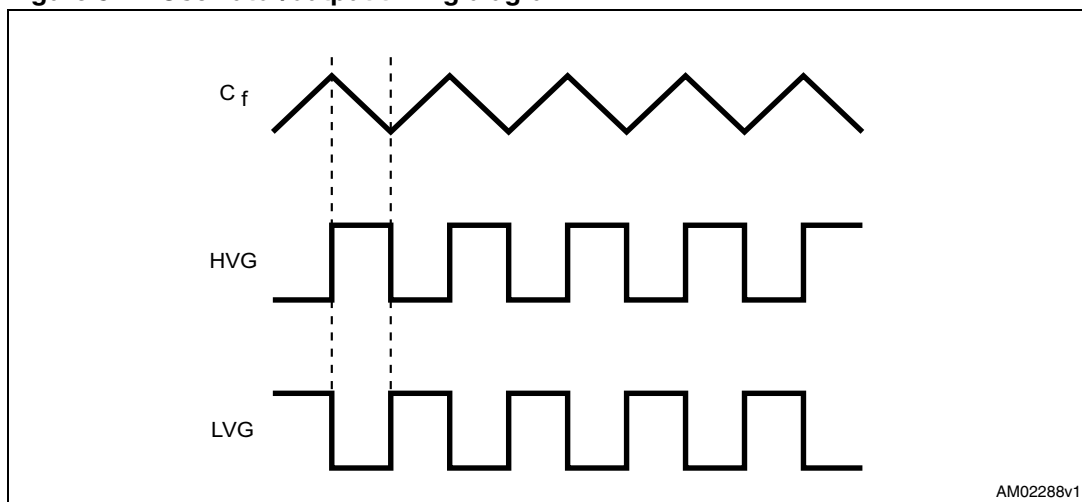


Figure 5. Oscillator/output timing diagram



5 Block diagram description

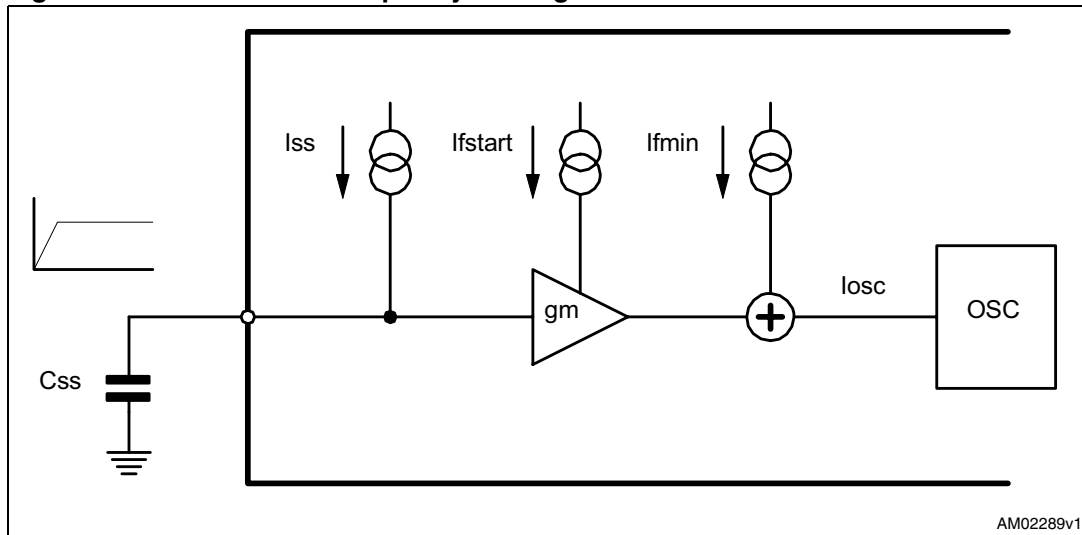
5.1 High/low side driving section

An high and low side driving section provide the proper driving to the external power MOS or IGBT. An high sink/source driving current (450/250 mA typ) ensure fast switching times also when size for power MOS are used. The internal logic ensures a minimum dead time to avoid cross-conduction of the power devices.

5.2 Timing and oscillator section

The device is provided of a soft start function. It consists in a period of time, T_{SS} , in which the switching frequency shifts from f_{start} to f_{min} . This feature is explained in the following description (ref. fig.7 and fig.8).

Figure 6. Soft start and frequency shifting block



During the soft start time the current I_{SS} charges the capacitor C_{SS} , generating a voltage ramp which is delivered to a transconductance amplifier, as shown in fig. 7. Thus this voltage signal is converted in a growing current which is subtracted to I_{fstart} . Therefore the current which drives the oscillator to set the frequency during the soft start is equal to:

Equation 1

$$I_{osc} = I_{fmin} + (I_{fstart} - g_m V_{C_{SS}}(t)) = I_{fmin} + \left(I_{fstart} - \frac{g_m I_{SS}}{C_{SS}} \right)$$

Equation 2

$$\text{where } I_{fmin} = \frac{V_{REF}}{R_{fmin}}, I_{fstart} = \frac{V_{REF}}{R_{fstart}}, V_{REF} = 2V$$

At the start-up ($t = 0$) the oscillator frequency is set by:

Equation 3

$$I_{OSC}(0) = I_{fmin} + I_{fstart} = V_{REF} \left(\frac{1}{R_{fmin}} + \frac{1}{R_{fstart}} \right)$$

At the end of soft start ($t = T_{SS}$) the second term of eq.1 decreases to zero and the switching frequency is set only by I_{min} (i.e. R_{fmin}):

Equation 4

$$I_{OSC}(T_{SS}) = I_{fmin} = \frac{V_{REF}}{R_{fmin}}$$

Since the second term of eq.1 is equal to zero, we have:

Equation 5

$$I_{fstart} - \frac{g_m I_{SS}}{C_{SS}} T_{SS} = 0 \rightarrow T_{SS} = \frac{C_{SS} I_{fstart}}{g_m I_{SS}}$$

Note that there is not a fixed threshold of the voltage across C_{SS} in which the soft start finishes (i.e. the end of the frequency shifting), and T_{SS} depends on C_{SS} , I_{fstart} , g_m , and I_{SS} (eq. 5). Making T_{SS} independent of I_{fstart} , the I_{SS} current has been designed to be a fraction of I_{fstart} , so:

Equation 6

$$I_{SS} = \frac{I_{fstart}}{K} \rightarrow T_{SS} = \frac{C_{SS} I_{fstart}}{g_m I_{fstart} K} \rightarrow T_{SS} = \frac{C_{SS}}{g_m K} \rightarrow T_{SS} = k_{SS} C_{SS}$$

In this way the soft start time depends only on the capacitor C_{SS} . The typical value of the k_{SS} constant (Soft start timing constant) is 0.15 s/ μ F.

The current I_{OSC} is fed to the oscillator as shown in fig. 7. It is twice mirrored (x4 and x8) generating the triangular wave on the oscillator capacitor C_f . Referring to the internal structure of the oscillator (fig.7), a good relationship to compute an approximate value of the oscillator frequency in normal operation is:

Equation 7

$$f_{min} = \frac{1.41}{R_{fmin} C_f}$$

The degree of approximation depends on the frequency value, but it remains very good in the range from 30 kHz to 100 kHz (figg.9-13)

Figure 7. Oscillator block

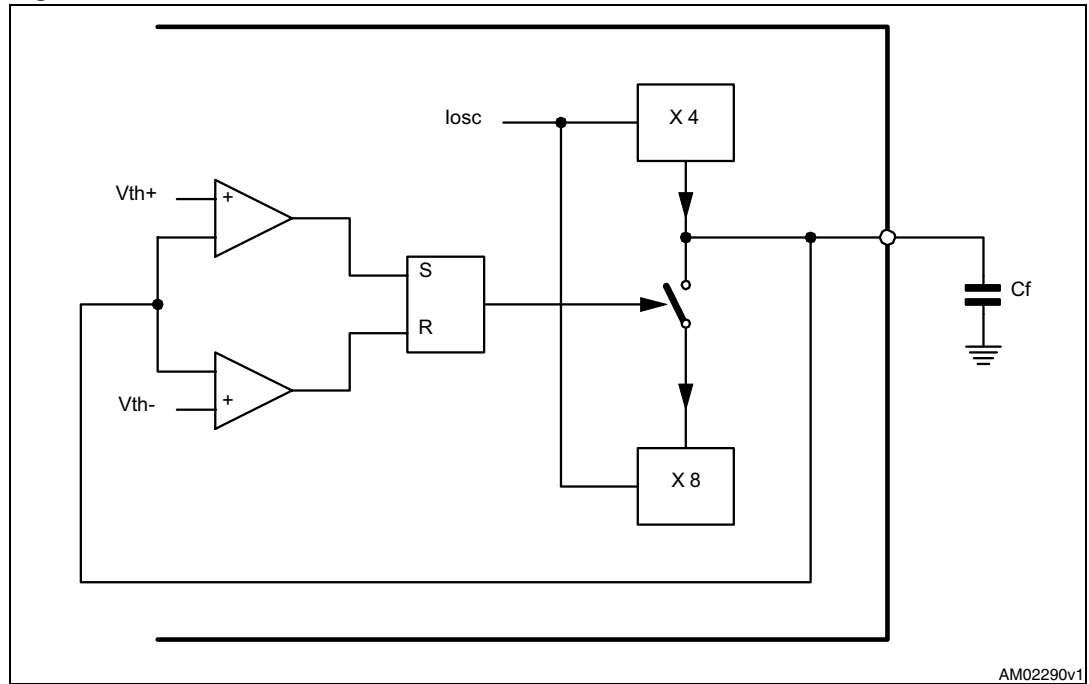


Figure 8. Typ. f_{min} vs. R_{fmin} @ $C_f = 470\text{ pF}$

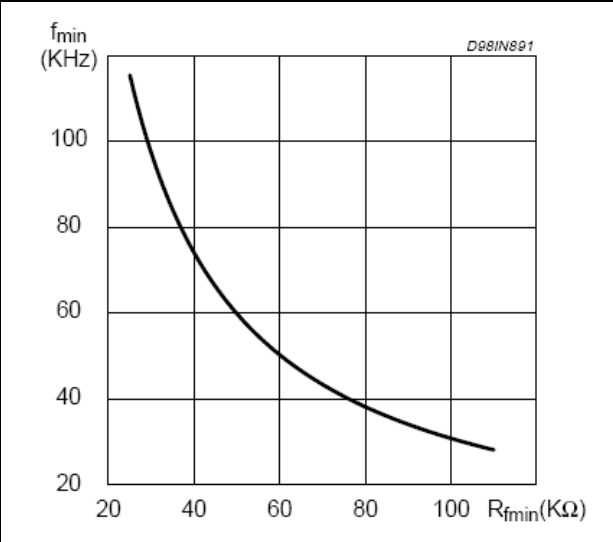


Figure 9. Typ. $(f_{start}-f_{min})$ vs. R_{fstar} @ $C_f = 470\text{ pF}$

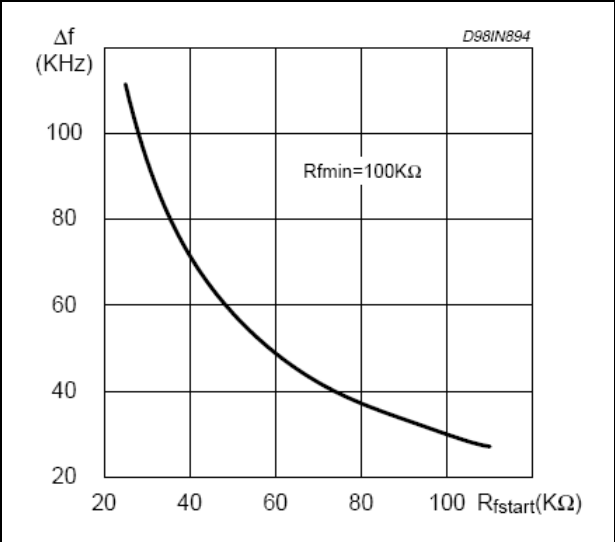


Figure 10. Typ. $(f_{start}-f_{min})$ vs. R_{fstar} @ $C_f = 470\text{ pF}$

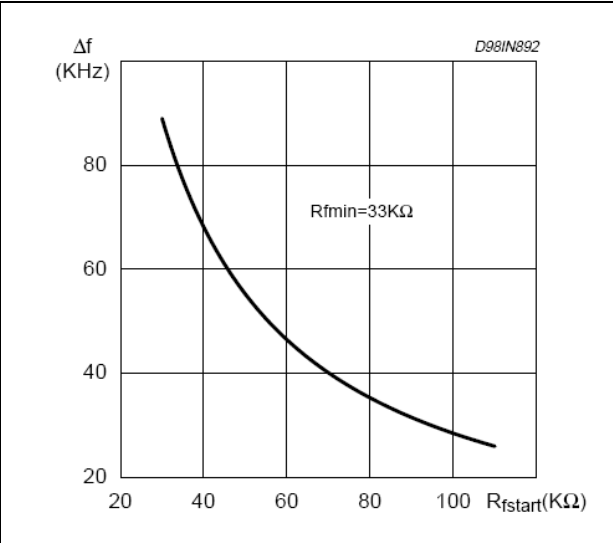


Figure 11. f_{min} @ different R_f vs C_f

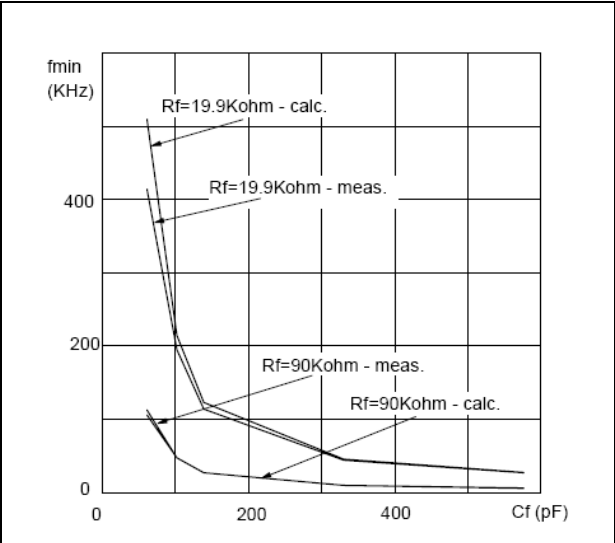
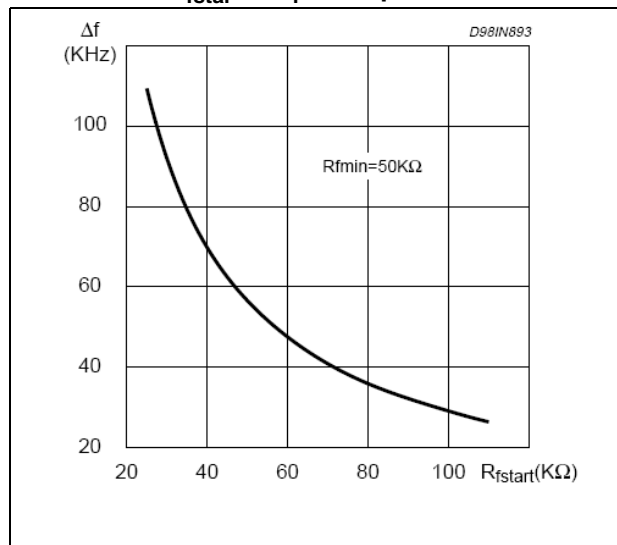


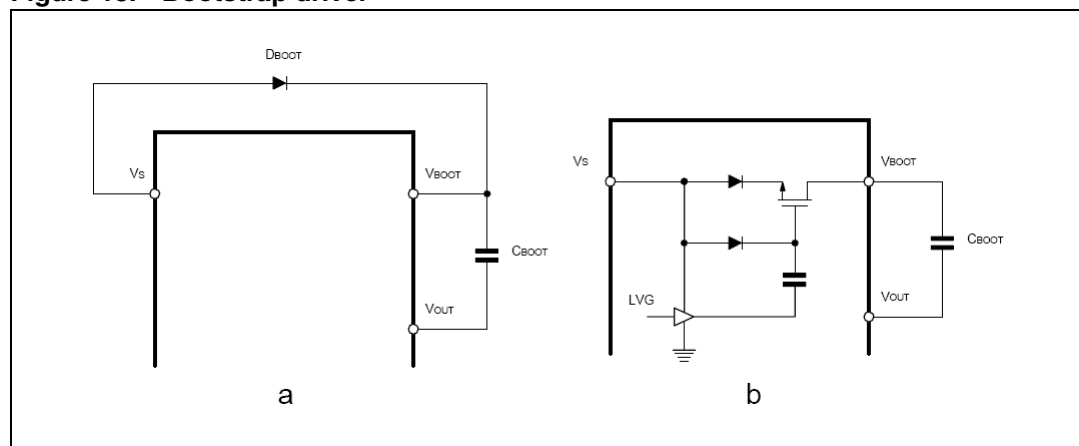
Figure 12. Typ. ($f_{\text{start}} - f_{\text{min}}$) vs. R_{fstar} @ $C_f = 470 \text{ pF}$



5.3 Bootstrap section

The supply of the high voltage section is obtained by means of a bootstrap circuitry. This solution normally requires an high voltage fast recovery diode for charging the bootstrap capacitor (fig. 14a). In the device a patented integrated structure, replaces this external diode. It is released by means of a high voltage DMOS, driven synchronously with the low side driver (LVG), with in series a diode, as shown in fig. 14b.

Figure 13. Bootstrap driver



To drive the synchronized DMOS it is necessary a voltage higher than the supply voltage V_s . This voltage is obtained by means of an internal charge pump (fig. 14b).

The diode connected in series to the DMOS has been added to avoid undesirable turn on of it. The introduction of the diode prevents any current can flow from the V_{boot} pin to the V_s one in case that the supply is quickly turned off when the internal capacitor of the pump is not fully discharged.

The bootstrap driver introduces a voltage drop during the recharging of the capacitor C_{boot} (i.e. when the low side driver is on), which increases with the frequency and with the size of the external power MOS. It is the sum of the drop across the R_{DSON} and of the diode threshold voltage. At low frequency this drop is very small and can be neglected. Anyway increasing the frequency it must be taken in to account. In fact the drop, reducing the amplitude of the driving signal, can significantly increase the R_{DSON} of the external power MOS (and so the dissipation).

To be considered that in resonant power supplies the current which flows in the power MOS decreases increasing the switching frequency and generally the increases of R_{DSON} is not a problem because power dissipation is negligible. The following equation is useful to compute the drop on the bootstrap driver:

Equation 8

$$V_{drop} = I_{charge} R_{dson} + V_{diode} \rightarrow V_{drop} = \frac{Q_g}{T_{charge}} R_{dson} + V_{diode}$$

where Q_g is the gate charge of the external power MOS, R_{dson} is the on resistance of the bootstrap DMOS, and T_{charge} is the time in which the bootstrap driver remains on (about the semi-period of the switching frequency minus the dead time). The typical resistance value of the bootstrap DMOS is 150Ω . For example using a power MOS with a total gate charge of 30 nC the drop on the bootstrap driver is about 3 V , at a switching frequency of 200 kHz . In fact:

Equation 9

$$V_{drop} = \frac{30 \text{ nC}}{2.23 \mu\text{s}} 150 \Omega + 0.6 \text{ V} \sim 2.6 \text{ V}$$

To summaries, if a significant drop on the bootstrap driver (at high switching frequency when large power MOS are used) represents a problem, an external diode can be used, avoiding the drop on the R_{DSON} of the DMOS.

5.4 Op amp section

The integrated op amp is designed to offer low output impedance, wide band, high input impedance and wide common mode range. It can be readily used to implement protection features or a closed loop control. For this purpose the op amp output can be properly connected to R_{fmin} pin to adjust the oscillation frequency.

5.5 Comparators

Two CMOS comparators are available to perform protection schemes.

Short pulses (≥ 200 ns) on comparators input are recognized. The EN1 input (active high), has a threshold of 0.6 V (typical value) forces the device in a latched shut down state (e.g. LVG low, HVG low, oscillator stopped), as in the under voltage conditions. Normal operating conditions are resumed after a power-off power-on sequence. The EN2 input (active high), with a threshold of 1.2 V (typical value) restarts a Soft Start sequence (see timing diagrams). In addition the EN2 comparator, when activated, removes a latched shutdown caused by EN1.

Figure 14. Switching time waveform definitions

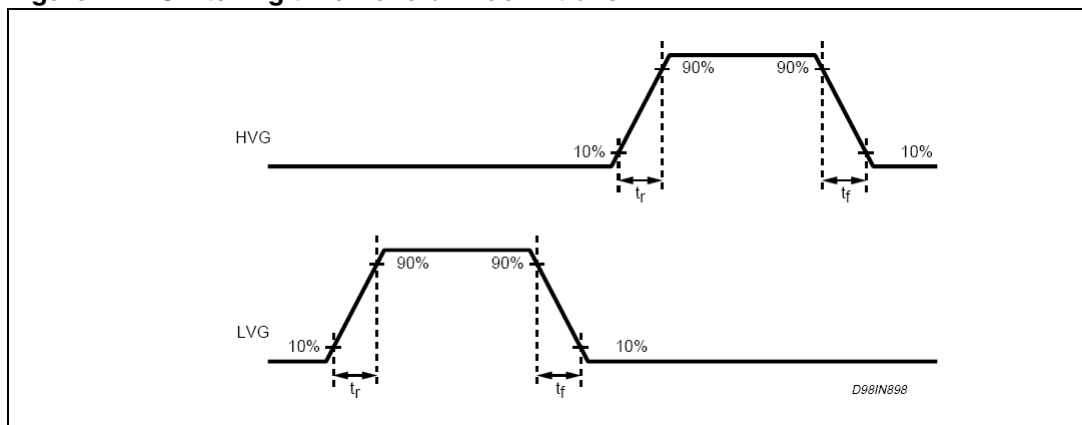


Figure 15. Dead time and duty cycle waveform definition

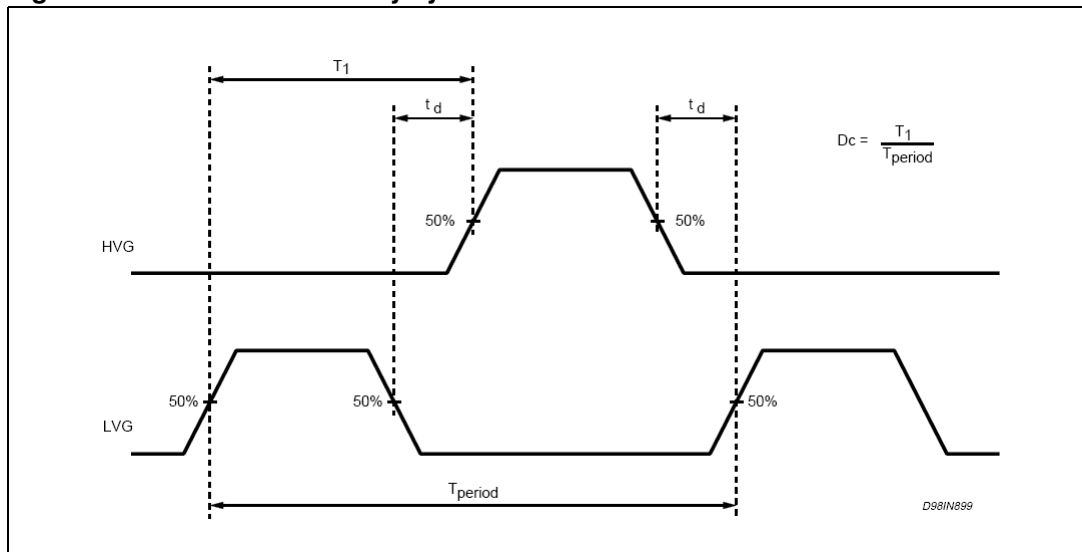


Figure 16. Typ. fmin vs. temperature

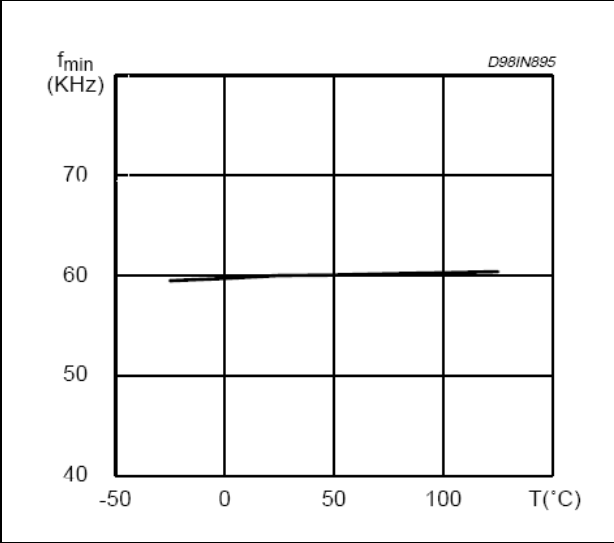


Figure 17. Start-up current vs temperature

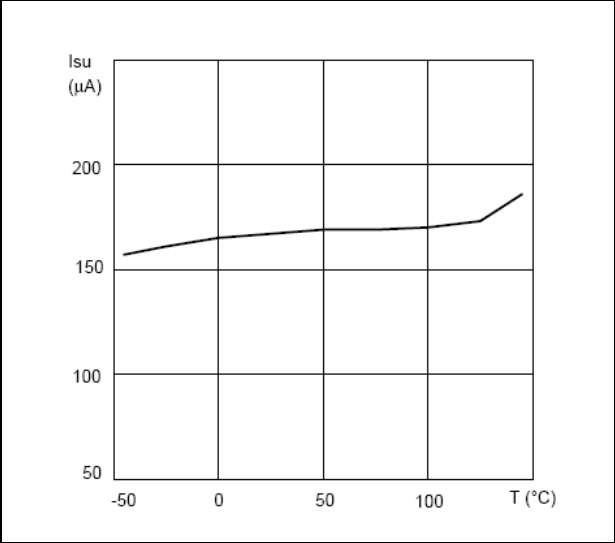


Figure 18. Typ. fstart vs. temperature

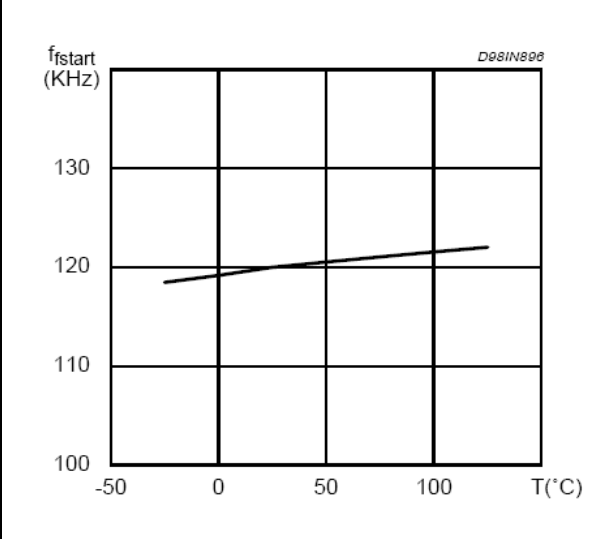


Figure 19. Quiescent current vs temperature

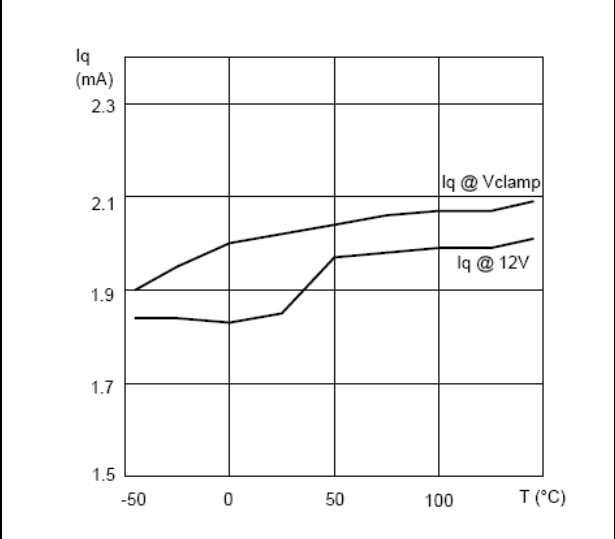


Figure 20. Vs thresholds and clamp vs temp. **Figure 21. HVG source and sink current vs. temperature**

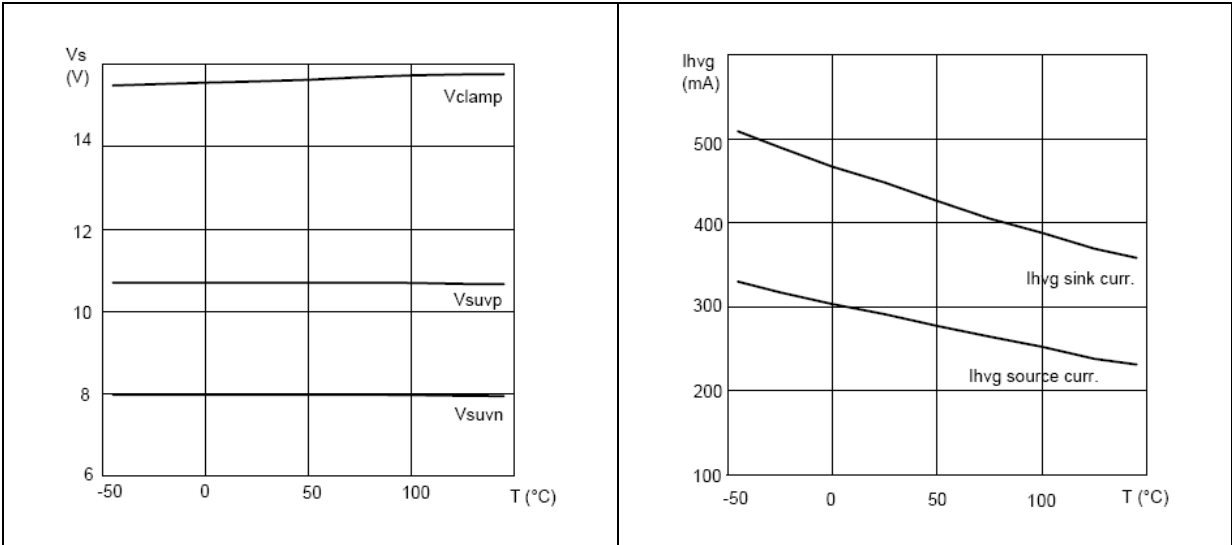


Figure 22. LVG source and sink current vs. temperature **Figure 23. Soft-start timing constant vs. temperature**

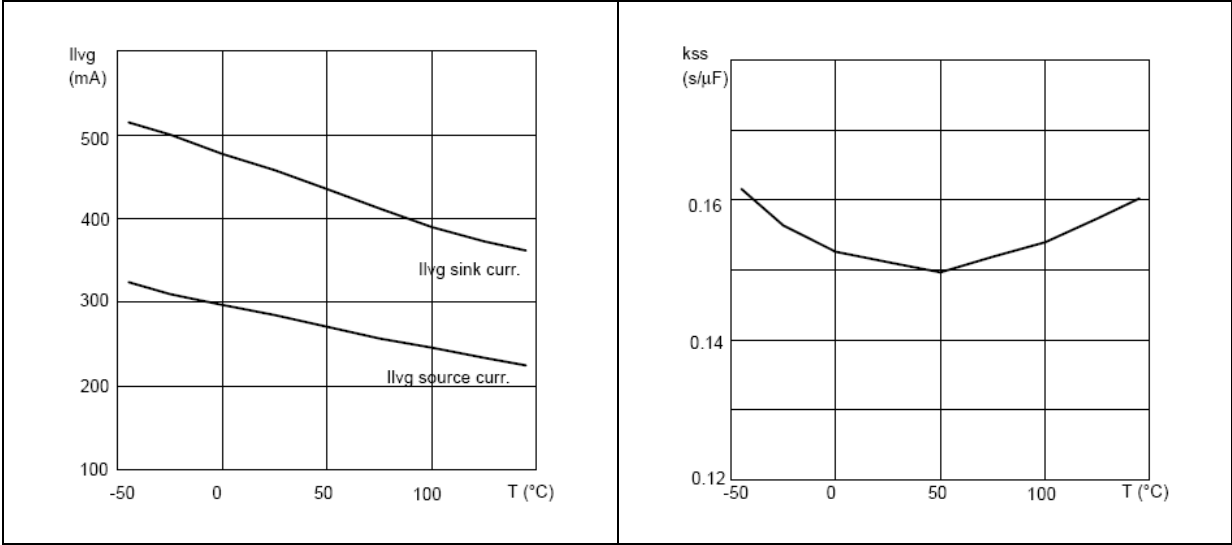
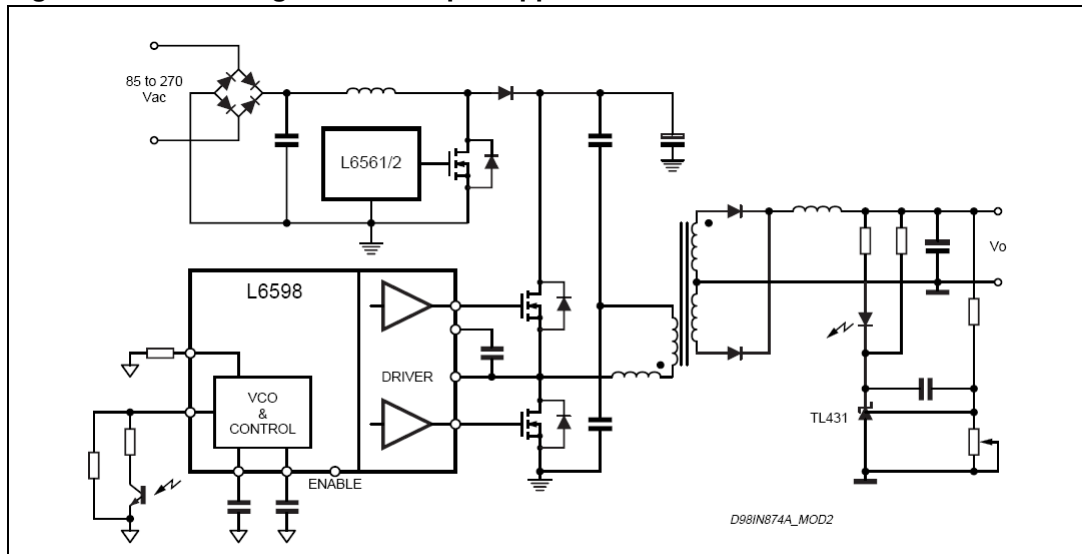


Figure 24. Wide range AC/DC adapter application

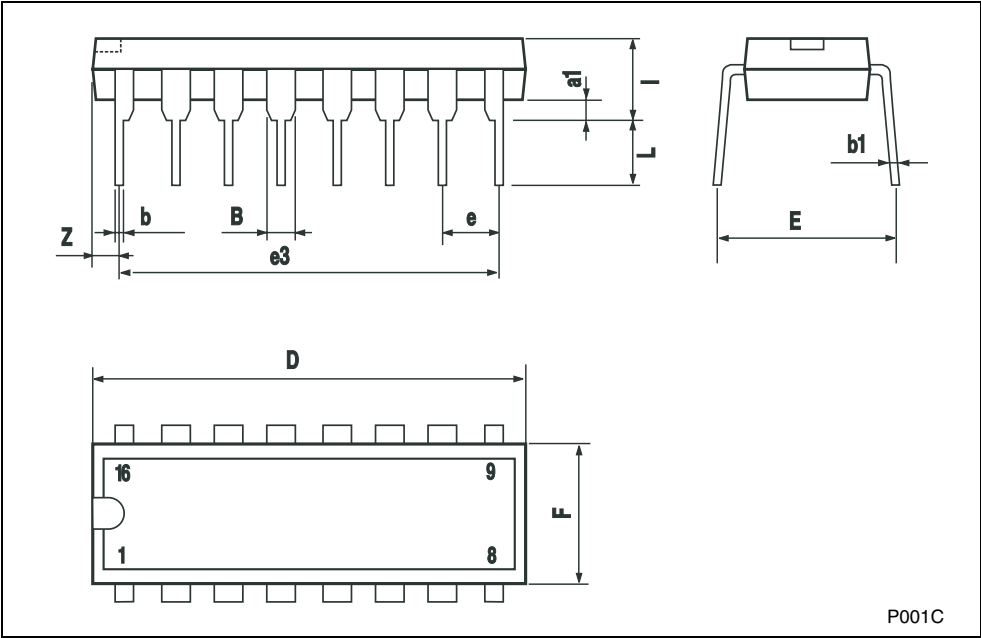


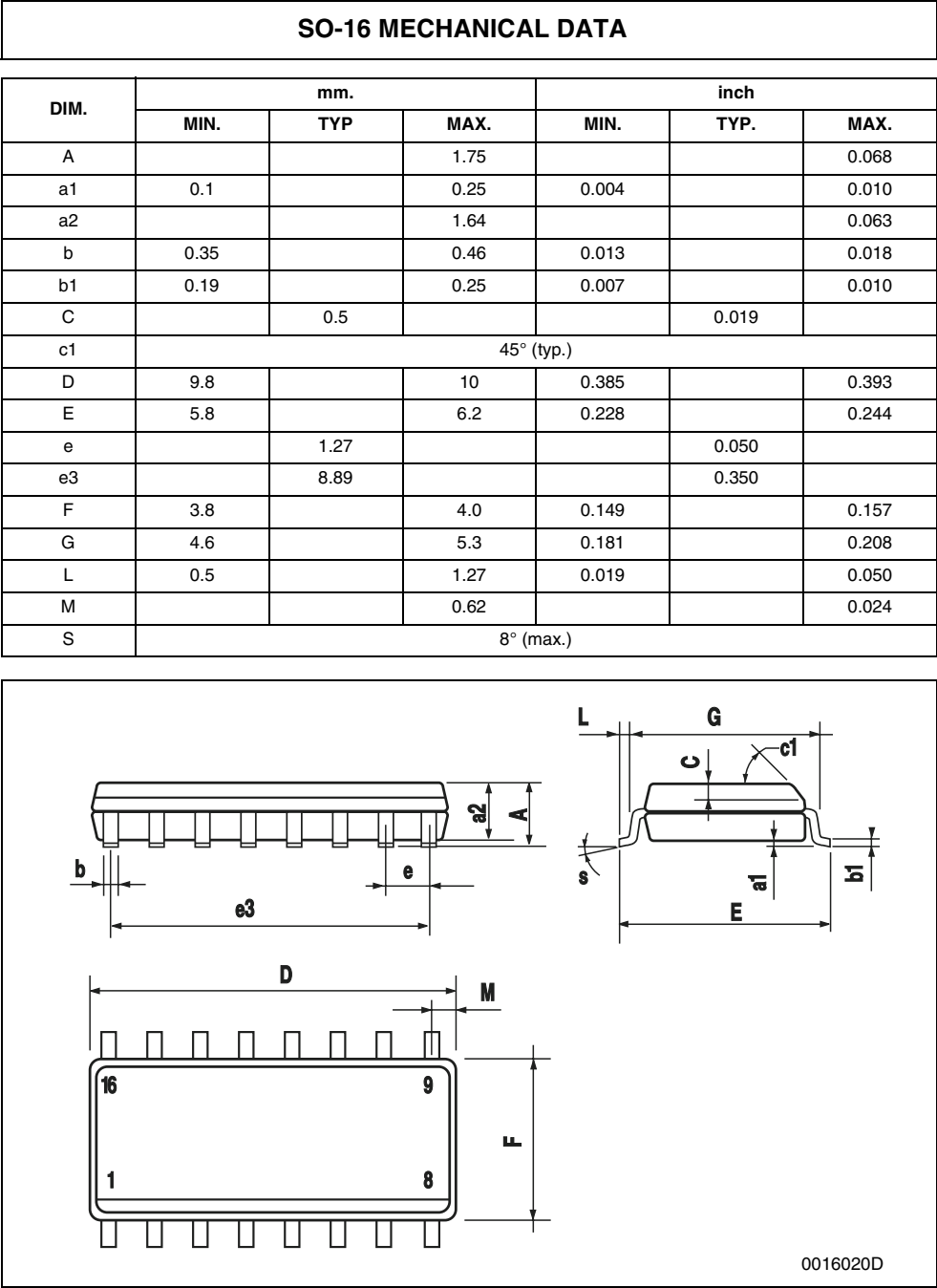
6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050





7 Ordering codes

Table 6. Ordering information

Order codes	Package	Packing
L6598	DIP16	Tube
L6598D	SO16N	Tube
L6598D016TR		Tape and reel

8 Revision history

Table 7. Document revision history

Date	Revision	Changes
21-Jun-2004	5	Changed the impagination following the new release of “corporate technical publication design guide”. Done a few of corrections in the text.
09-Sep-2004	6	Added ordering number fot the tape and reel version, updated Table 4 on page 4
02-Oct-2009	7	Updated Table 4 on page 4

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