



ESDALC5-1BM2, ESDALC5-1BT2

Single line low capacitance Transil™ for ESD protection

Features

- Single line low capacitance Transil diode
- Bidirectional ESD protection
- Breakdown Voltage $V_{br} = 5\text{ V min.}$
- Low diode capacitance (26 pF typ at 0 V)
- Low leakage current $< 50\text{ nA @ }3\text{ V}$
- Very small PCB area: 0.6 mm^2

Benefits

- High ESD protection level
- High integration
- Suitable for high density boards
- Lead-free
- “Halogen-free” according to ECOPACK®2

Complies with the following standards:

- IEC 61000-4-2 level 4
 - 15 kV (air discharge)
 - 8 kV (contact discharge)
- MIL STD 883G - Method 3015-7: class 3
 - Human body model

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment

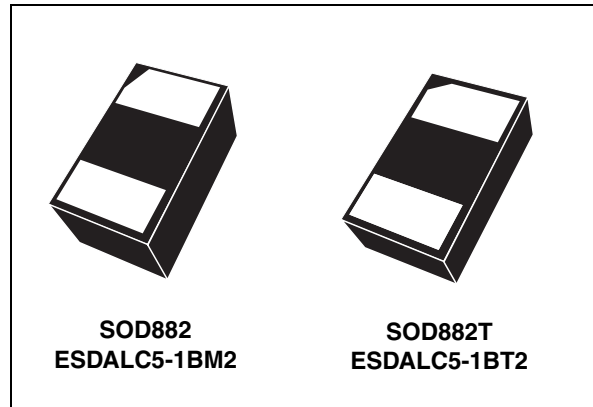
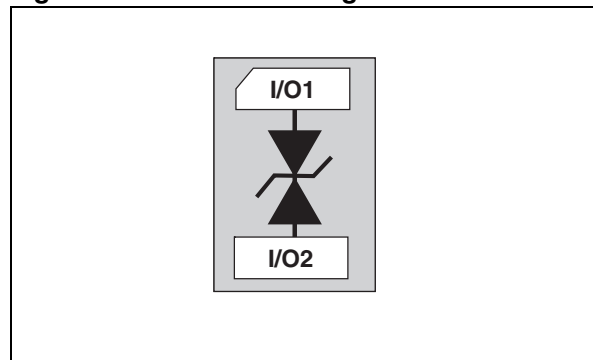


Figure 1. Functional diagram



Description

The ESDALC5-1BM2 and ESDALC5-1BT2 are bidirectional single line TVS diodes designed to protect datalines or other I/O ports against ESD transients.

These devices are ideal for applications where both reduced line capacitance and board space saving are required.

TM: Transil is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute maximum ratings ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Value	Unit
V_{PP}	Peak pulse voltage IEC 61000-4-2 contact discharge	± 30	kV
$P_{PP}^{(1)}$	Peak pulse power dissipation (8/20 μs) T_j initial = T_{amb}	150	W
I_{PP}	Peak pulse current (8/20 μs)	9	A
T_j	Junction temperature	- 55 to + 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	- 65 to + 150	$^{\circ}\text{C}$
T_L	Maximum lead temperature for soldering during 10 s	260	$^{\circ}\text{C}$

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Figure 2. Electrical characteristics (definitions)

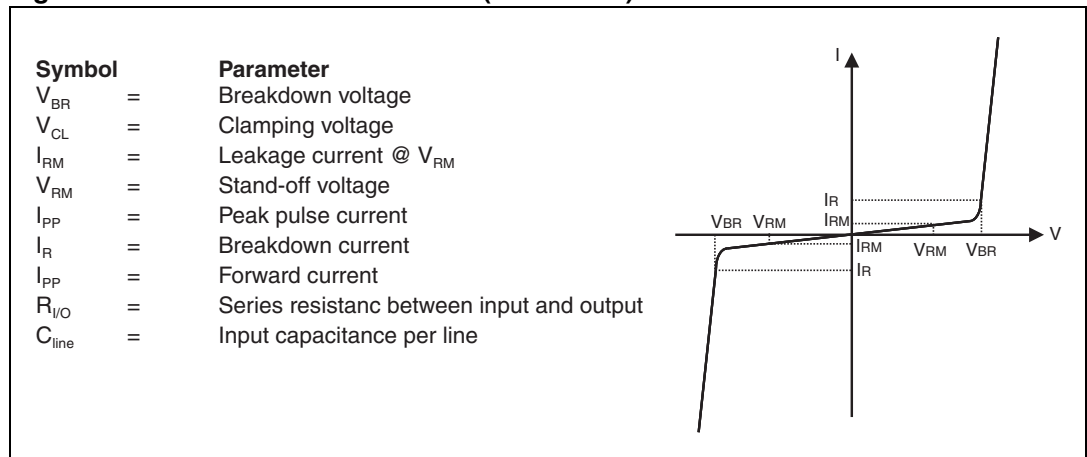


Table 2. Electrical characteristics (values, $T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Test condition	Min.	Typ.	Max.	Unit
V_{BR}	From pin1 to pin2, $I_R = 1\text{ mA}$ (direct)	11	13		V
	From pin2 to pin1, $I_R = 1\text{ mA}$ (reverse)	5	8		
I_{RM}	$V_{RM} = 3\text{ V}$			50	nA
R_d	Square pulse, $I_{PP} = 1\text{ A}$ $t_p = 2.5\text{ }\mu\text{s}$		650		m Ω
C_{line}	$F = 1\text{ MHz}$, $V_R = 0\text{ V}$		26	30	pF

Figure 3. Relative variation of peak pulse power versus initial junction temperature

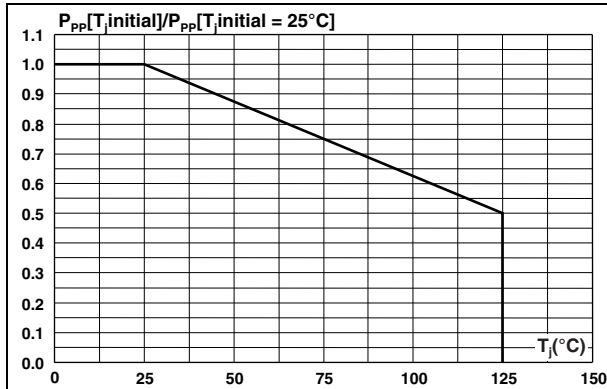


Figure 4. Relative variation of leakage current versus junction temperature (typical values)

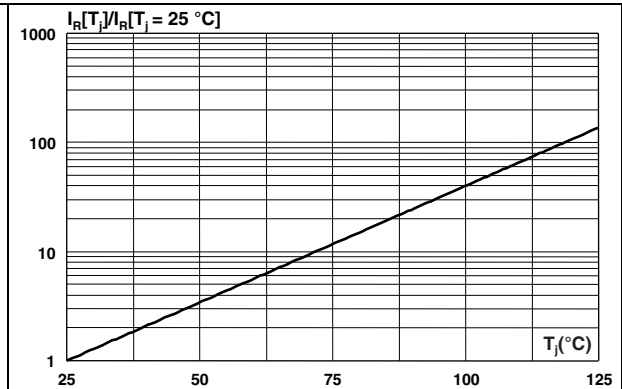


Figure 5. Peak pulse power versus exponential pulse duration (direct)

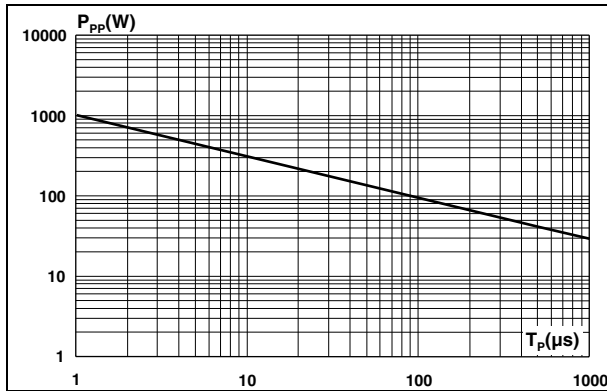


Figure 6. Peak pulse power versus exponential pulse duration (reverse)

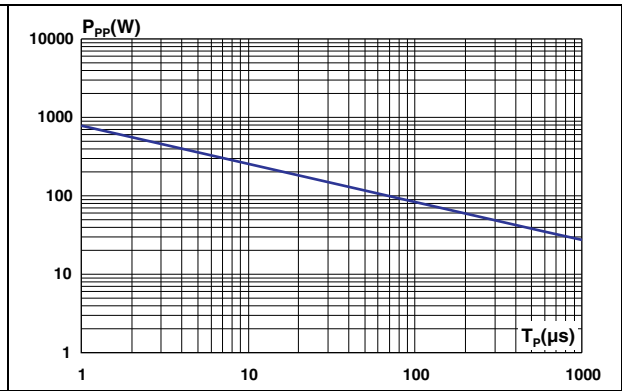


Figure 7. Clamping voltage versus peak pulse current (typical values, exponential waveform, direct)

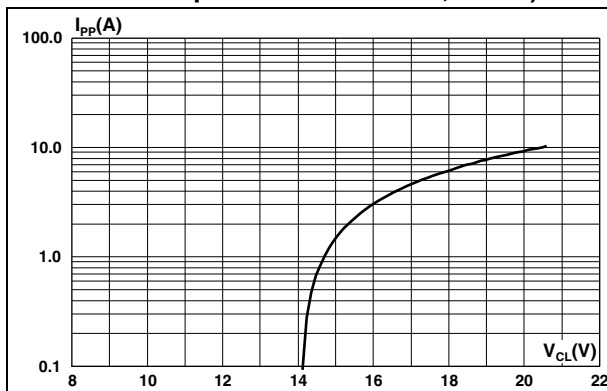


Figure 8. Clamping voltage versus peak pulse current (typical values, exponential waveform, reverse)

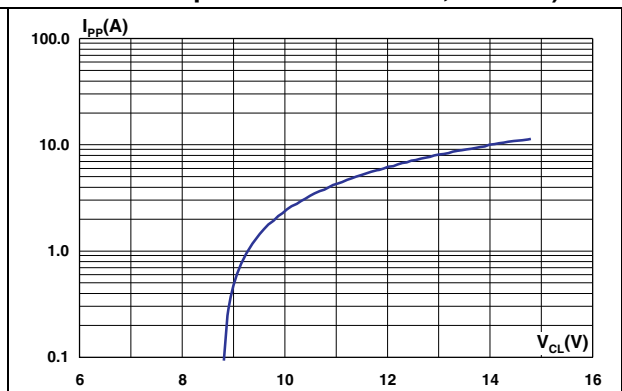


Figure 9. Junction capacitance versus reverse applied voltage (typical values, direct)

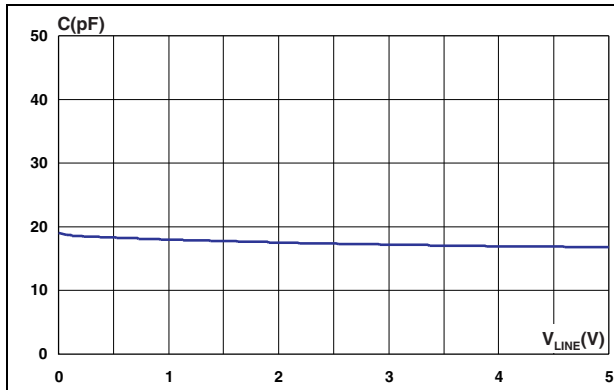


Figure 10. Junction capacitance versus reverse applied voltage (typical values, reverse)

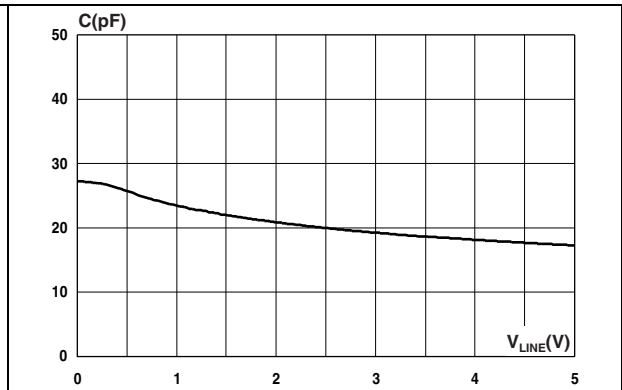


Figure 11. ESD response to IEC 61000-4-2 (+15kV air discharge)

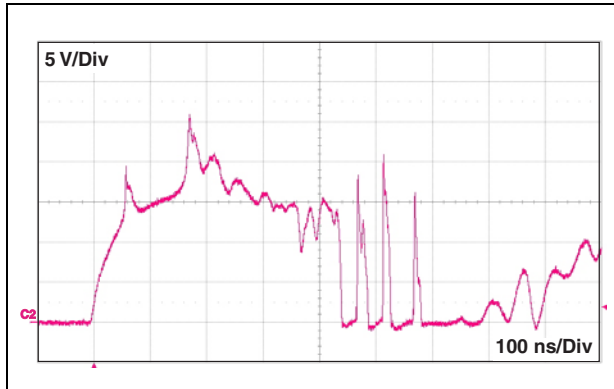


Figure 12. ESD response to IEC 61000-4-2 (-15kV air discharge)

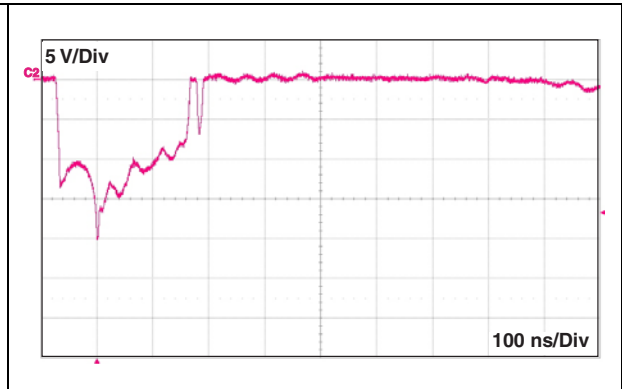


Figure 13. S21 attenuation measurement result

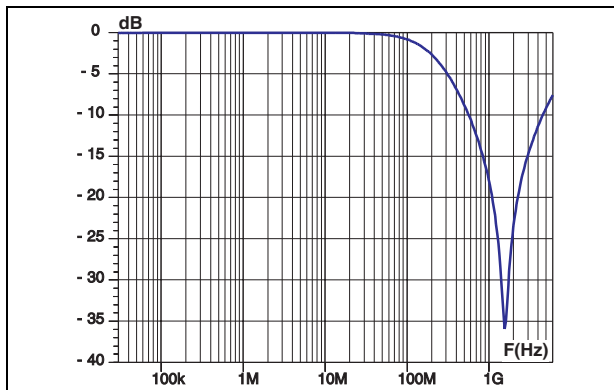
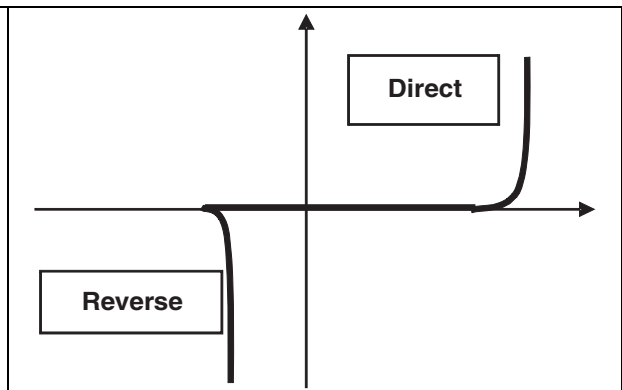
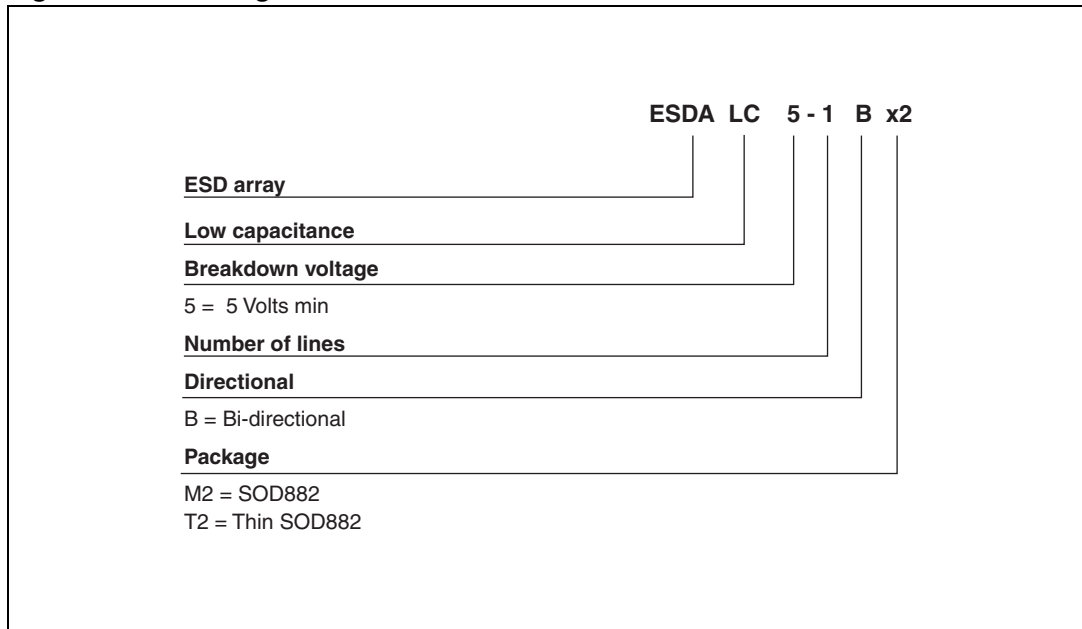


Figure 14. Static characteristic



2 Ordering information scheme

Figure 15. Ordering information scheme



3 Package information

- Epoxy meets UL94, V0
- Lead-free packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 16. SOD882 dimension definitions

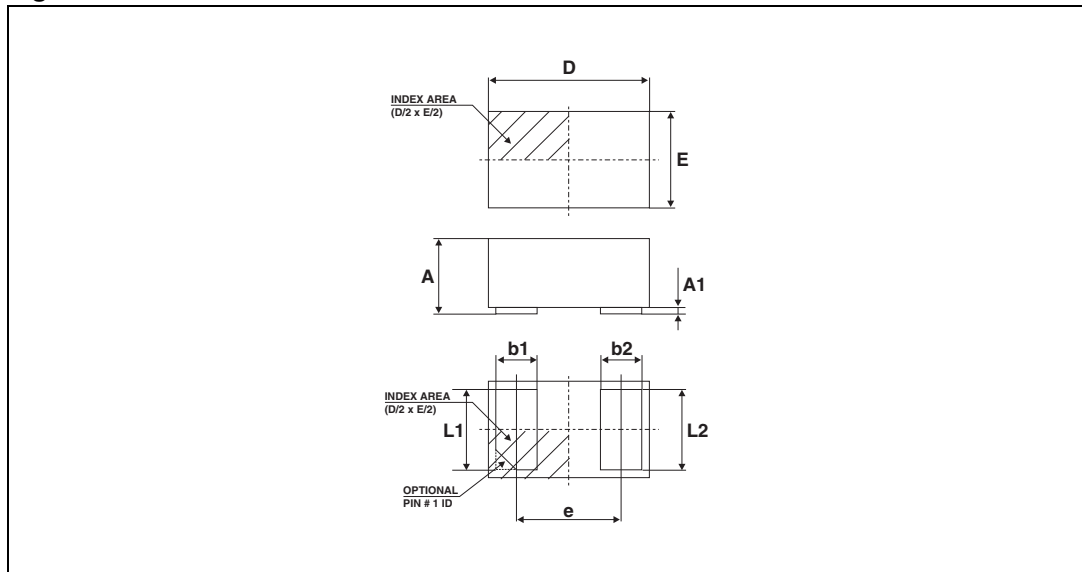


Table 3. SOD882 dimension values

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.40	0.47	0.50	0.016	0.019	0.020
A1	0.00		0.05	0.000		0.002
b1	0.20	0.25	0.30	0.008	0.010	0.012
b2	0.20	0.25	0.30	0.008	0.010	0.012
D		1.00			0.039	
E		0.60			0.024	
e		0.65			0.026	
L1	0.45	0.50	0.55	0.018	0.020	0.022
L2	0.45	0.50	0.55	0.018	0.020	0.022

Figure 17. SOD882 footprint in mm (inches)

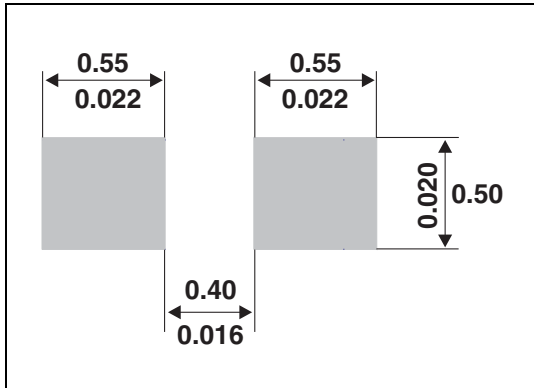
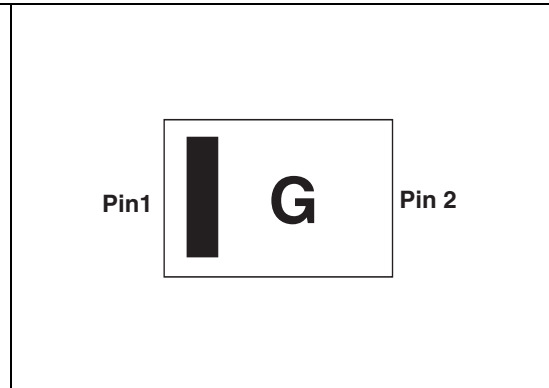


Figure 18. SOD882 marking



Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 19. SOD882 tape and reel specifications

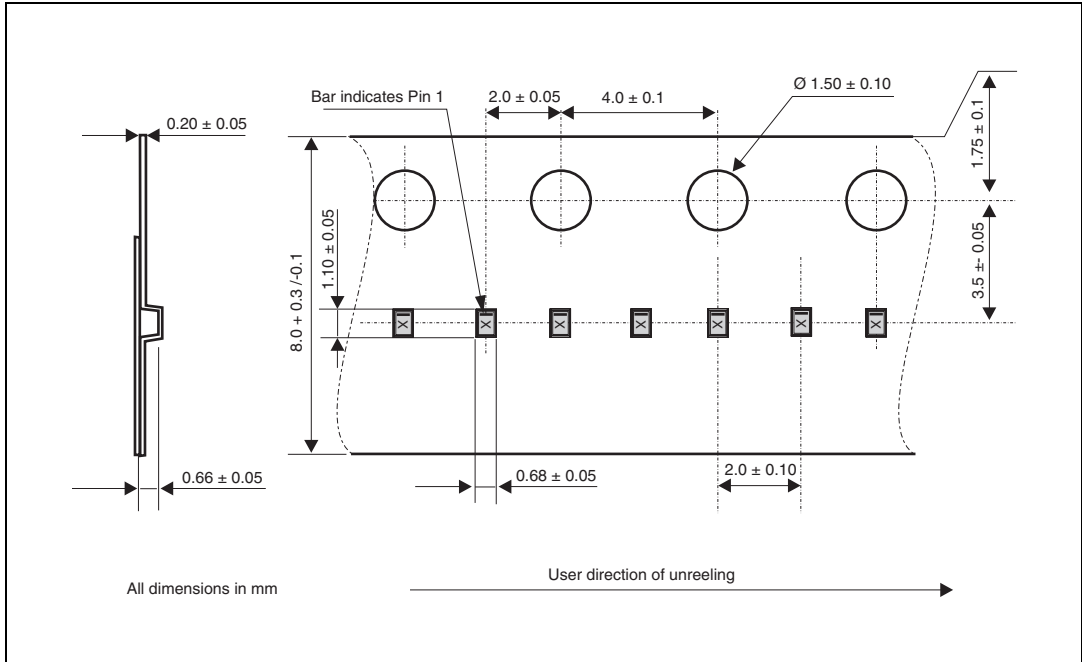


Figure 20. SOD882T dimension definitions

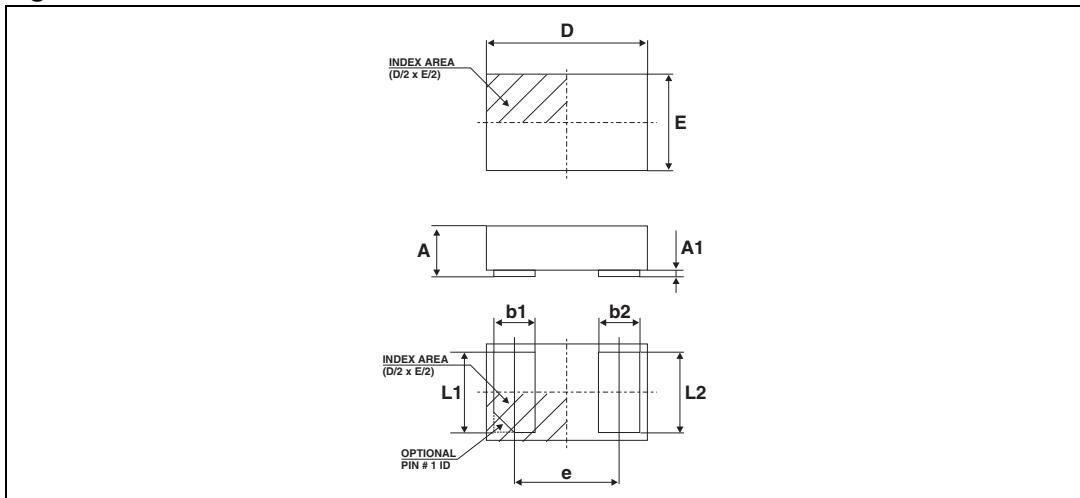
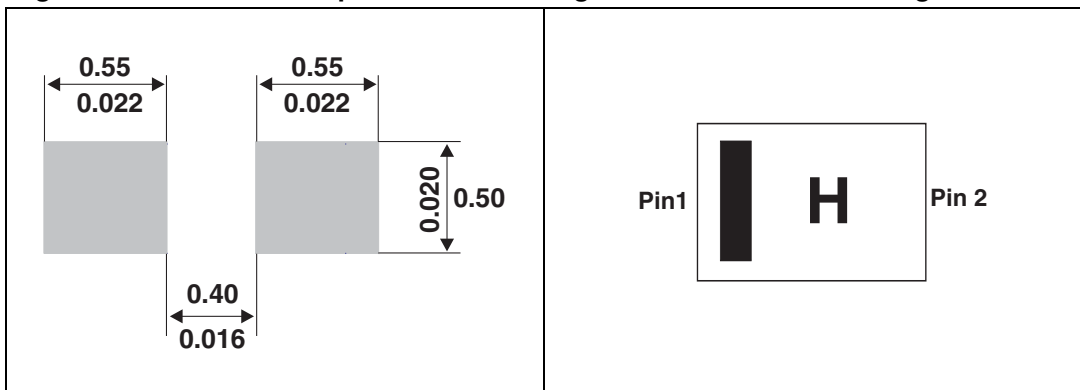


Table 4. SOD882T dimension values

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.30		0.40	0.012		0.016
A1	0.00		0.05	0.000		0.002
b1	0.20	0.25	0.30	0.008	0.010	0.012
b2	0.20	0.25	0.30	0.008	0.010	0.012
D		1.00			0.039	
E		0.60			0.024	
e		0.65			0.026	
L1	0.45	0.50	0.55	0.018	0.020	0.022
L2	0.45	0.50	0.55	0.018	0.020	0.022

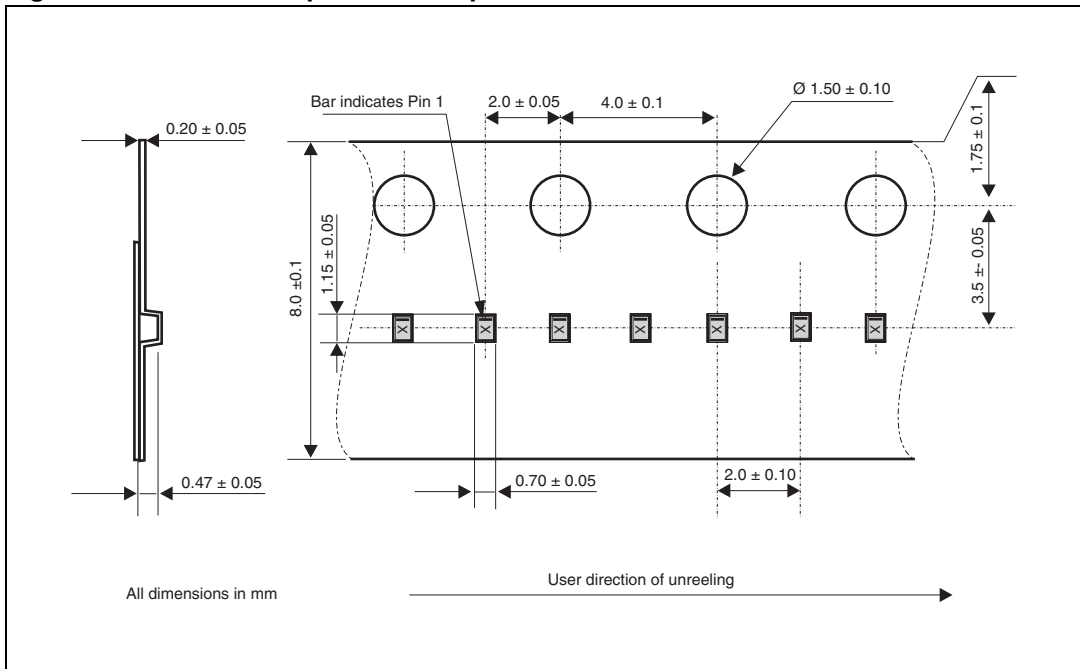
Figure 21. SOD882T footprint

Figure 22. SOD882T marking



Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 23. SOD882T tape and reel specifications

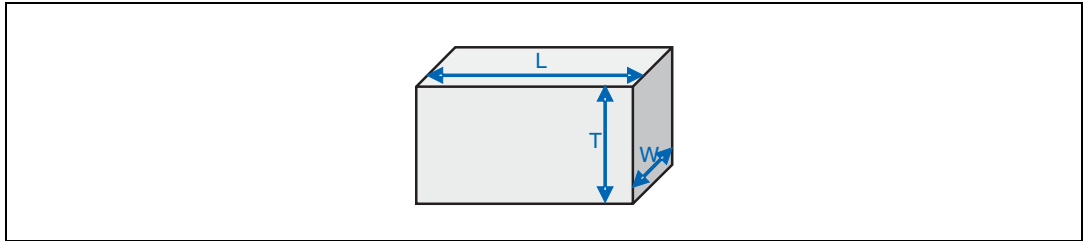


4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
 - a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

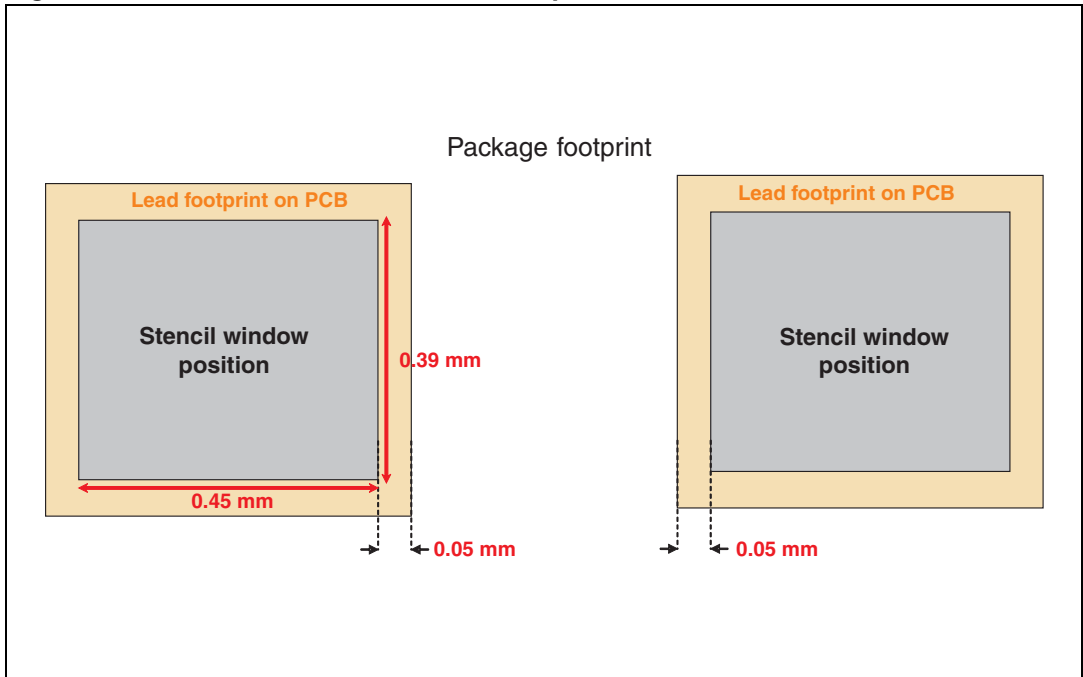
Figure 24. Stencil opening dimensions



- b) General design rule
 - Stencil thickness (T) = 75 ~ 125 μm
 - Aspect Ratio = $\frac{W}{T} \geq 1.5$
 - Aspect Area = $\frac{L \times W}{2T(L + W)} \geq 0.66$

2. Reference design
 - a) Stencil opening thickness: 100 μm
 - b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
 - c) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 25. Recommended stencil window position



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 μm .

4.3 Placement

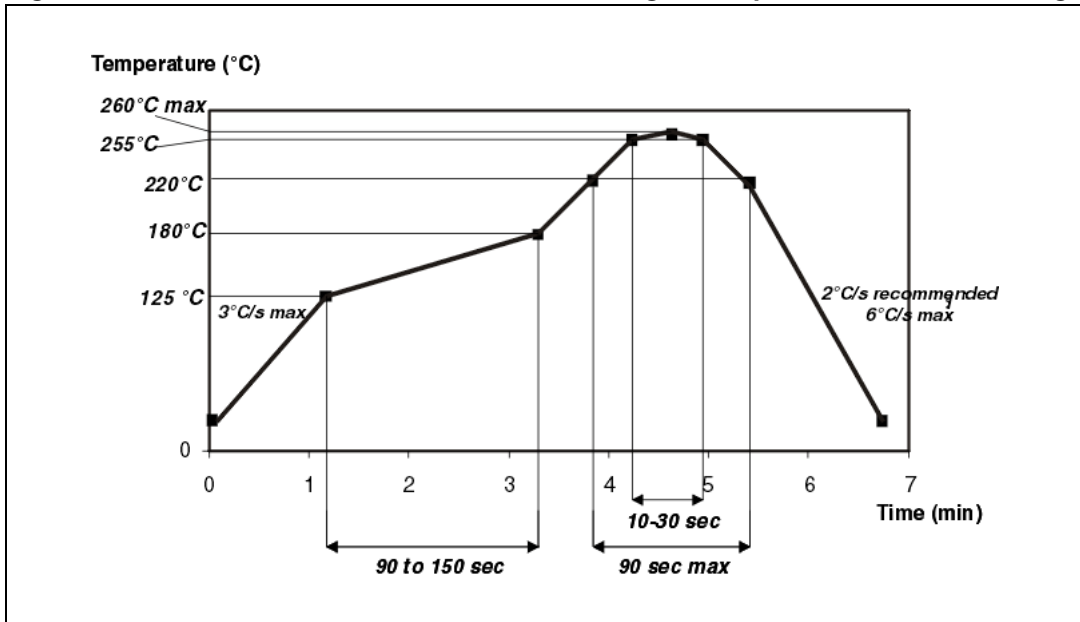
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 26. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 5. Ordering information

Order code	Marking ⁽¹⁾	Package	Weight	Base qty	Delivery mode
ESDALC5-1BM2	G	SOD882	0.92 mg	12000	Tape and reel
ESDALC5-1BT2	H	SOD882T	0.76 mg	12000	Tape and reel

1. The marking can be rotated by 90° to differentiate assembly location

6 Revision history

Table 6. Document revision history

Date	Revision	Changes
02-Feb-2010	1	Initial release.

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