

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF40193B

MSI

4-bit up/down binary counter

Product specification
File under Integrated Circuits, IC04

January 1995

4-bit up/down binary counter

HEF40193B MSI

DESCRIPTION

The HEF40193B is a 4-bit synchronous up/down binary counter. The counter has a count-up clock input (CP_U), a count-down clock input (CP_D), an asynchronous parallel load input (\overline{PL}), four parallel data inputs (P₀ to P₃), an asynchronous master reset input (MR), four counter outputs (O₀ to O₃), an active LOW terminal count-up (carry) output (\overline{TC}_U) and an active LOW terminal count-down (borrow) output (\overline{TC}_D).

The counter outputs change state on the LOW to HIGH transition of either clock input. However, for correct counting, both clock inputs cannot be LOW simultaneously. The outputs \overline{TC}_U and \overline{TC}_D are normally HIGH. When the circuit has reached the maximum count state of '15', the next HIGH to LOW transition of CP_U will cause \overline{TC}_U to go LOW. \overline{TC}_U will stay LOW until CP_U goes HIGH again. Likewise, output \overline{TC}_D will go LOW when the circuit is in the zero state and CP_D goes LOW. When \overline{PL} is LOW, the information on P₀ to P₃ is asynchronously loaded into the counter. A HIGH on MR resets the counter independent of all other input conditions. The counter stages are of a static toggle type flip-flop.

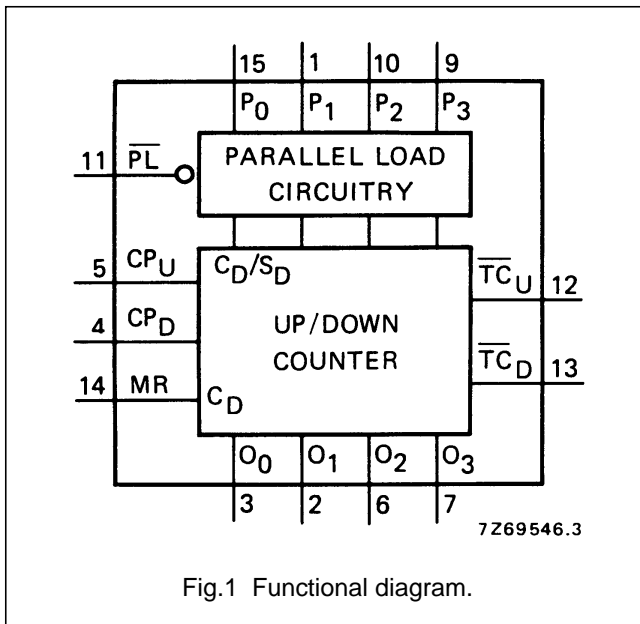


Fig.1 Functional diagram.

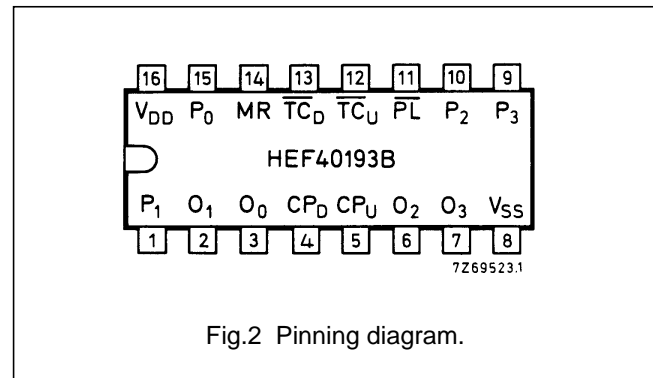


Fig.2 Pinning diagram.

PINNING

- \overline{PL} parallel load input (active LOW)
- P₀ to P₃ parallel data inputs
- CP_U count-up clock pulse input (LOW to HIGH, edge-triggered)
- CP_D count-down clock pulse input (LOW to HIGH, edge-triggered)
- MR master reset input (asynchronous)
- \overline{TC}_U buffered terminal count-up (carry) output (active LOW)
- \overline{TC}_D buffered terminal count-down (borrow) output (active LOW)
- O₀ to O₃ buffered counter outputs

- HEF40193BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF40193BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF40193BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specification

4-bit up/down binary counter

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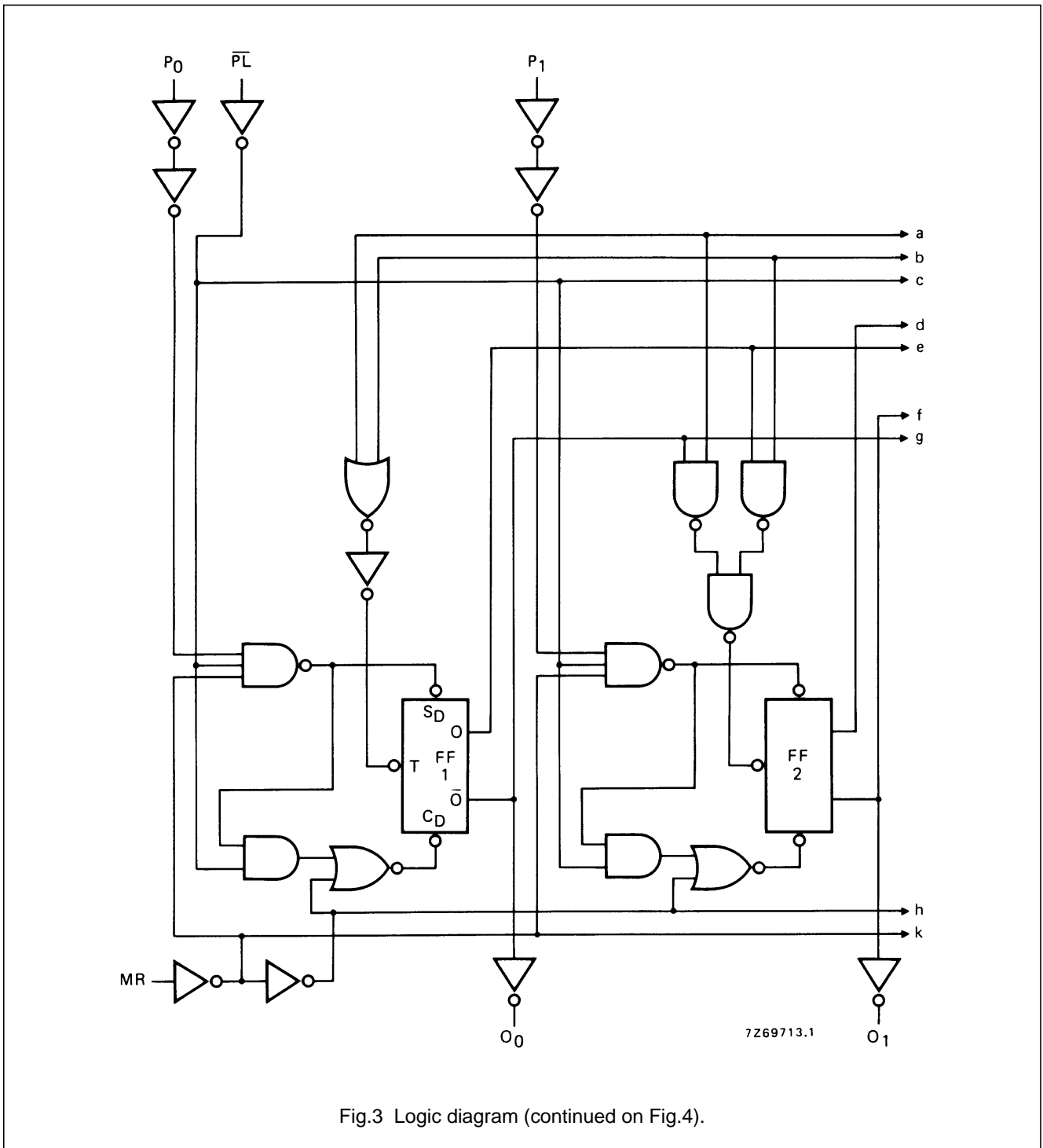
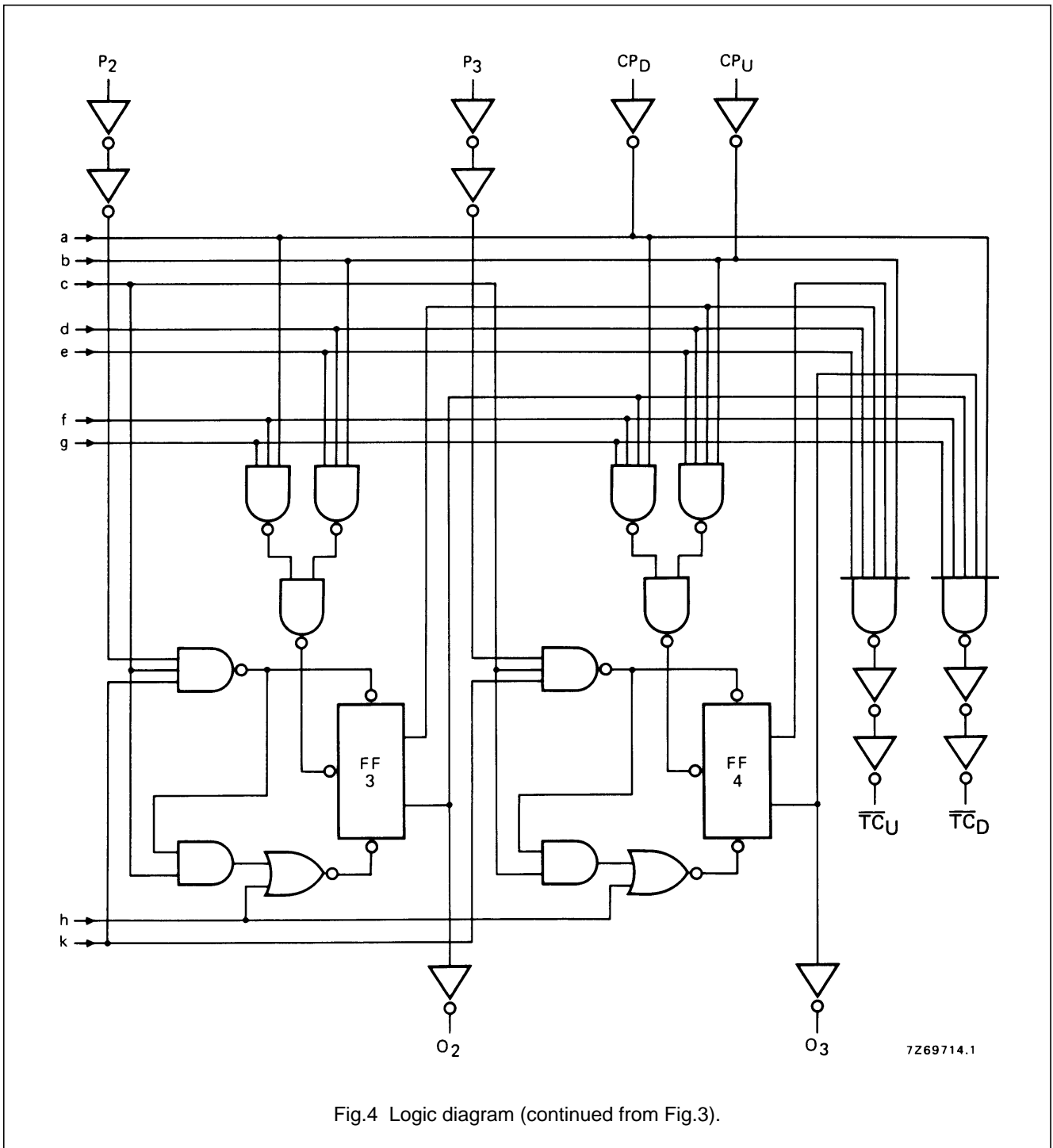


Fig.3 Logic diagram (continued on Fig.4).

4-bit up/down binary counter



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4-bit up/down binary counter


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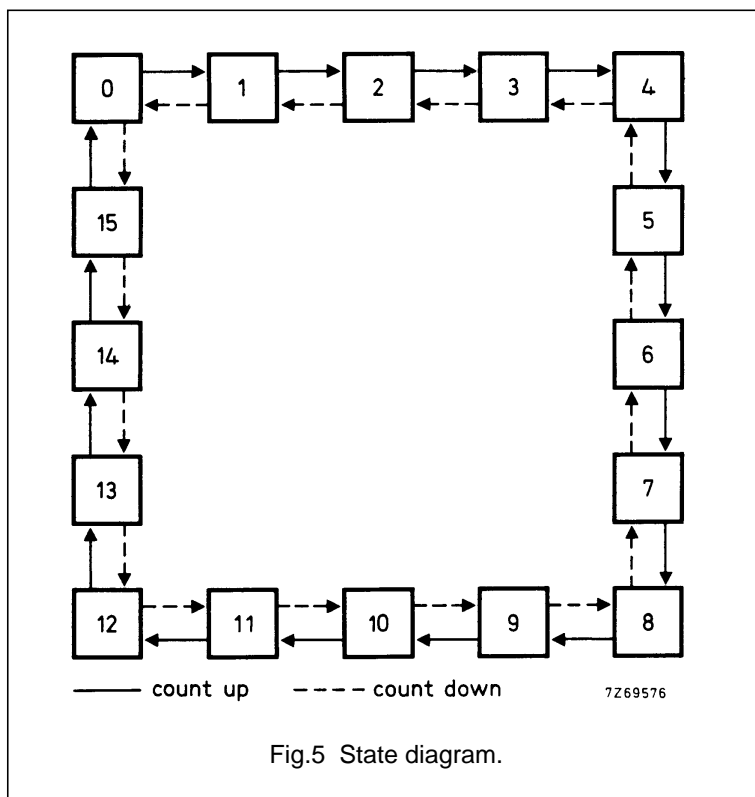
FUNCTION TABLE

MR	\overline{PL}	CP _U	CP _D	MODE
H	X	X	X	reset (asyn.)
L	L	X	X	parallel load
L	H		H	count-up
L	H	H		count-down

Notes

- H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

 = positive-going transition



Logic equations for terminal count:

$$\overline{TC}_U = \overline{O_0 \cdot O_1 \cdot O_2 \cdot O_3 \cdot CP_U}$$

$$\overline{TC}_D = \overline{\overline{O_0} \cdot \overline{O_1} \cdot \overline{O_2} \cdot \overline{O_3} \cdot CP_D}$$

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	600 f _i + Σ(f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
	10	2700 f _i + Σ(f _o C _L) × V _{DD} ²	
	15	7500 f _i + Σ(f _o C _L) × V _{DD} ²	

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AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $CP_U \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	210	415	ns	$183\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		85	165	ns	$74\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		60	120	ns	$52\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	5	t_{PLH}	170	340	ns	$143\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		70	140	ns	$59\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15		50	100	ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
$CP_D \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	210	425	ns	$183\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		85	170	ns	$74\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		60	125	ns	$57\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	5	t_{PLH}	170	340	ns	$143\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		70	140	ns	$59\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15		50	100	ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
$CP_U \rightarrow \overline{TC}_U$ HIGH to LOW	5	t_{PHL}	125	250	ns	$98\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	5	t_{PLH}	95	185	ns	$68\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
$CP_D \rightarrow \overline{TC}_D$ HIGH to LOW	5	t_{PHL}	140	280	ns	$113\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		55	110	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	5	t_{PLH}	100	195	ns	$73\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		40	85	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15		30	65	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
$MR \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	195	390	ns	$168\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		80	160	ns	$69\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		60	120	ns	$52\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$MR \rightarrow \overline{TC}_U$ LOW to HIGH	5	t_{PLH}	145	285	ns	$118\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		60	115	ns	$49\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		45	90	ns	$37\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$MR \rightarrow \overline{TC}_D$ HIGH to LOW	5	t_{PHL}	365	730	ns	$338\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		130	265	ns	$119\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		100	205	ns	$92\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$\overline{PL} \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	185	360	ns	$158\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		75	150	ns	$64\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		55	110	ns	$47\text{ ns} + (0,16\text{ ns/pF}) C_L$	

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	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
LOW to HIGH	5	t _{PLH}	145	290	ns	118 ns + (0,55 ns/pF) C _L
	10		60	120	ns	49 ns + (0,23 ns/pF) C _L
	15		45	90	ns	37 ns + (0,16 ns/pF) C _L

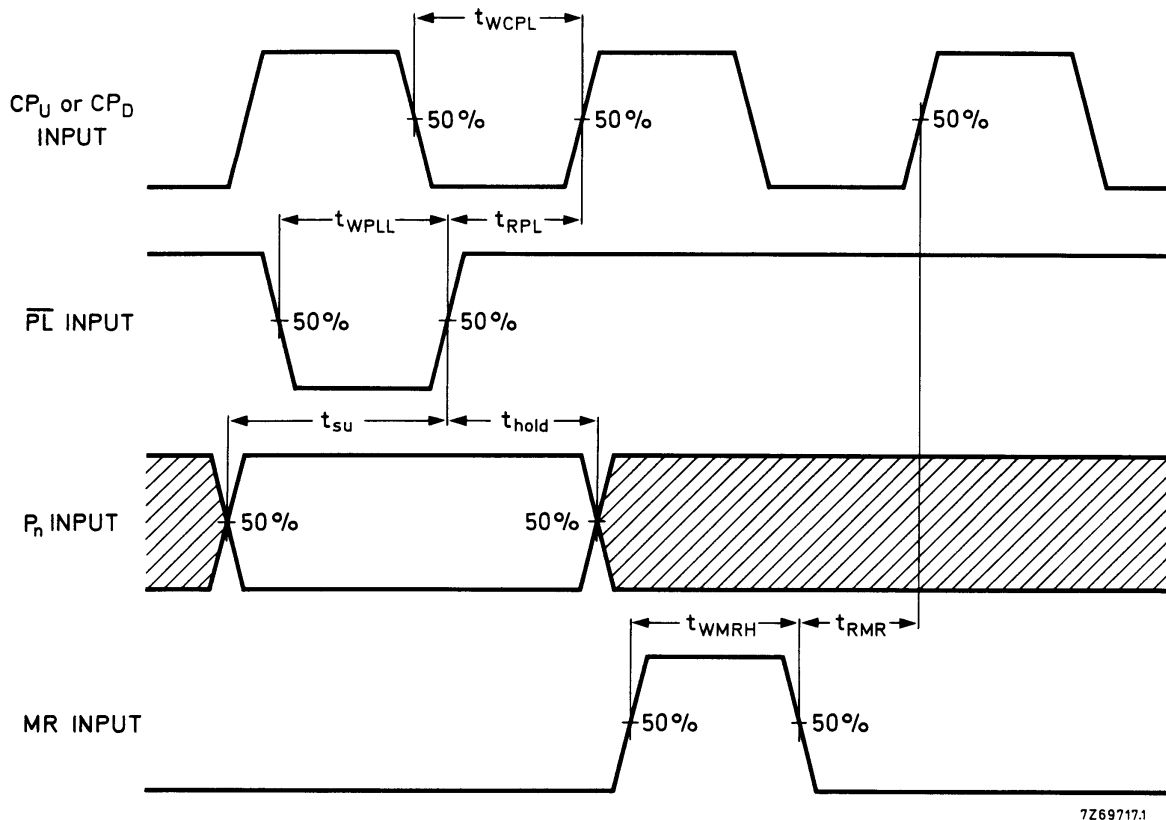
AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Output transition times HIGH to LOW	5	t _{THL}	60	120	ns	10 ns + (1,0 ns/pF) C _L	
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L	
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L	
	LOW to HIGH	5	t _{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C _L
		10		30	60	ns	9 ns + (0,42 ns/pF) C _L
		15		20	40	ns	6 ns + (0,28 ns/pF) C _L
Set-up time P _n → \overline{PL}	5	t _{su}	160	80	ns	see also waveforms Fig.6	
	10		60	30	ns		
	15		50	25	ns		
Hold time P _n → \overline{PL}	5	t _{hold}	10	-70	ns		
	10		5	-25	ns		
	15		5	-20	ns		
Minimum CP _U or CP _D pulse width; LOW	5	t _{WCPL}	150	75	ns		
	10		50	25	ns		
	15		35	20	ns		
Minimum MR pulse width; HIGH	5	t _{WMRH}	180	90	ns		
	10		70	35	ns		
	15		60	30	ns		
Minimum \overline{PL} pulse width; LOW	5	t _{WPLL}	120	60	ns		
	10		45	20	ns		
	15		30	15	ns		
Recovery time for MR	5	t _{RMR}	125	65	ns		
	10		70	35	ns		
	15		50	25	ns		
Recovery time for \overline{PL}	5	t _{RPL}	90	45	ns		
	10		35	15	ns		
	15		25	10	ns		
Maximum clock pulse frequency	5	f _{max}	2,5	5	MHz		
	10		7	14	MHz		
	15		9	18	MHz		

4-bit up/down binary counter

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Fig.6 Waveforms showing recovery times for $\overline{P_L}$ and MR, minimum pulse widths for CP_U, CP_D, $\overline{P_L}$ and MR, and set-up and hold times for P to $\overline{P_L}$. Set-up times and hold times are shown as positive values but may be specified as negative values.

4-bit up/down binary counter

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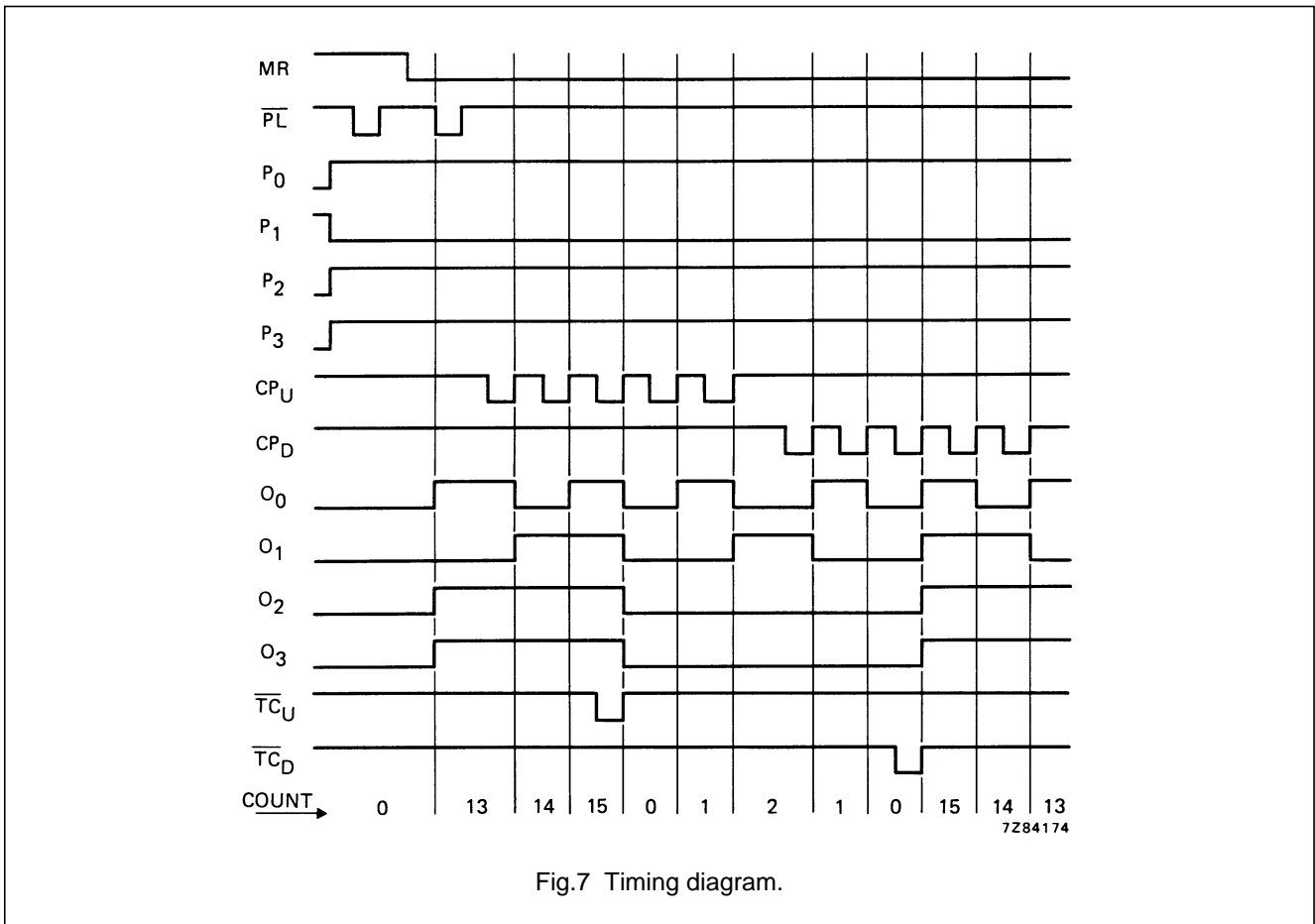


Fig.7 Timing diagram.

APPLICATION INFORMATION

Some examples of applications for the HEF40193B are:

- Up/down difference counting
- Multistage ripple counting
- Multistage synchronous counting

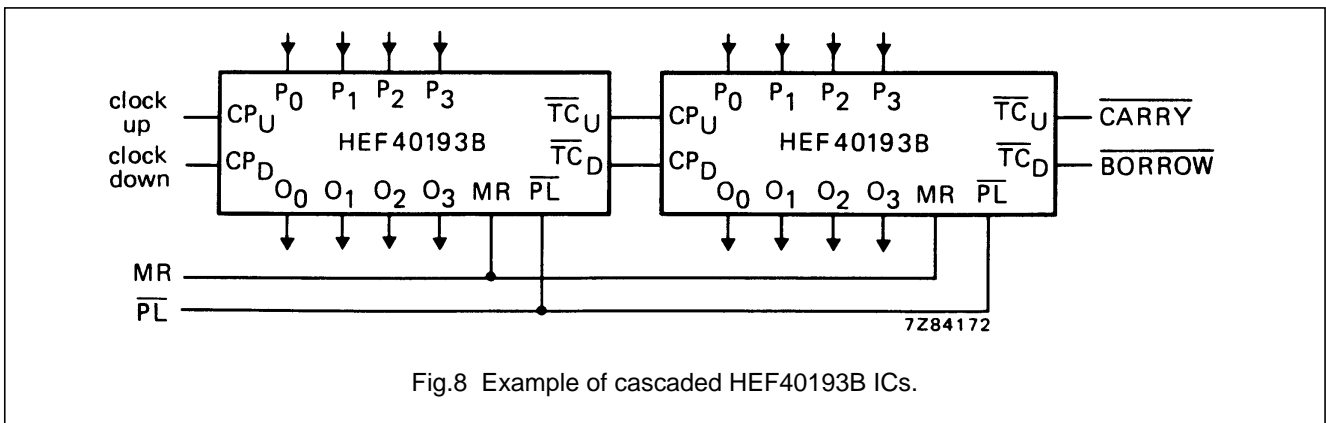


Fig.8 Example of cascaded HEF40193B ICs.

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