

MC10ELT21, MC100ELT21

5 V Differential PECL to TTL Translator

The MC10ELT/100ELT21 is a differential PECL to TTL translator. Because PECL (Positive ECL) levels are used, only +5 V and ground are required. The small outline 8-lead package and the single gate of the ELT21 makes it ideal for those applications where space, performance and low power are at a premium.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- 3.5 ns Typical Propagation Delay
- 24 mA TTL Output
- Flow Through Pinouts
- ESD Protection: Human Body Model; > 2 KV
- Operating Range: V_{CC} = 4.75 V to 5.25 V with GND = 0 V
- Q Output Will Default LOW with Inputs Left Open or < 1.3 V
- Internal Input 50 K Ω Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
- For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 81 devices

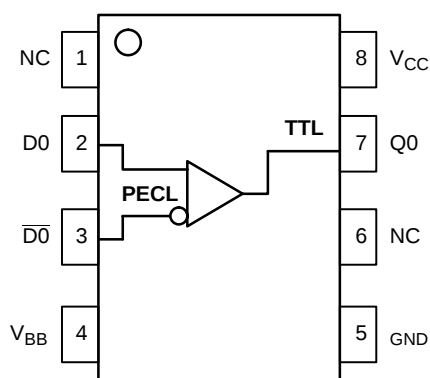


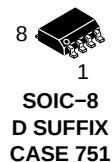
Figure 1. 8-Lead Pinout and Logic Diagram
(Top View)



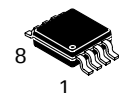
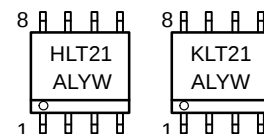
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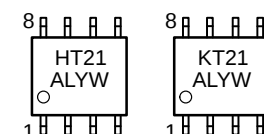
MARKING DIAGRAMS*



SOIC-8
D SUFFIX
CASE 751



TSSOP-8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional marking information, refer to Application Note AND8002/D.

PIN DESCRIPTION

PIN	FUNCTION
Q0	TTL Output
D0, $\overline{D0}$	PECL Differential Inputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
GND	Ground
NC	No Connect

ORDERING INFORMATION

Device	Package	Shipping [†]
MC10ELT21D	SOIC-8	98 Units/Rail
MC10ELT21DR2	SOIC-8	2500 Tape & Reel
MC100ELT21D	SOIC-8	98 Units/Rail
MC100ELT21DR2	SOIC-8	2500 Tape & Reel
MC10ELT21DT	TSSOP-8	98 Units/Rail
MC10ELT21DTR2	TSSOP-8	2500 Tape & Reel
MC100ELT21DT	TSSOP-8	98 Units/Rail
MC100ELT21DTR2	TSSOP-8	2500 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Power Supply	GND = 0 V		7	V
V _{IN}	PECL Input Voltage	GND = 0 V	V _I ≤ V _{CC}	0 to 6	V
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
T _A	Operating Temperature Range			–40 to +85	°C
T _{stg}	Storage Temperature Range			–65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC–8 SOIC–8	190 130	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC–8	41 to 44	°C/W
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP–8 TSSOP–8	185 140	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP–8	41 to 44 ± 5%	°C/W
T _{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected. Functional operation should be restricted to the Recommended Operating Conditions.

10ELT SERIES PECL INPUT DC CHARACTERISTICS V_{CC}= 5.0 V; GND= 0.0 V (Note 1)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{IH}	Input HIGH Voltage (Single-Ended)	3770		4110	3870		4190	3930		4265	mV
V _{IL}	Input LOW Voltage (Single-Ended)	3050		3500	3050		3520	3050		3555	mV
V _{BB}	Output Voltage Reference	3.57		3.7	3.65		3.75	3.69		3.81	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 2)	2.2		5.0	2.2		5.0	2.2		5.0	V
I _{IH}	Input HIGH Current			255			175			175	μA
I _{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.25 V.
- V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC}.

100ELT SERIES PECL INPUT DC CHARACTERISTICS V_{CC}= 5.0 V; GND= 0.0 V (Note 3)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{IH}	Input HIGH Voltage (Single-Ended)	3835		4120	3835		4120	3835		4120	mV
V _{IL}	Input LOW Voltage (Single-Ended)	3190		3525	3190		3525	3190		3525	mV
V _{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.745	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 4)	2.2		5.0	2.2		5.0	2.2		5.0	V
I _{IH}	Input HIGH Current			255			175			175	μA
I _{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.25 V.
- V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC}.

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TTL OUTPUT DC CHARACTERISTICS $V_{CC} = 4.75 \text{ V to } 5.25 \text{ V}$; $T_A = -40^\circ\text{C to } 85^\circ\text{C}$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.0 \text{ mA}$	2.4		(Note 5)	V
V_{OL}	Output LOW Voltage	$I_{OL} = 24 \text{ mA}$			0.5	V
I_{CCH}	Power Supply Current			20	29	mA
I_{CCL}	Power Supply Current			22	32	mA
I_{OS}	Output Short Circuit Current		-150		-60	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Maximum level is $V_{CC} - 0.7$ by design.

AC CHARACTERISTICS $V_{CC} = 4.75 \text{ V to } 5.25 \text{ V}$; $GND = 0.0 \text{ V}$ (Note 6)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency					100					MHz
t_{JITTER}	Random Clock Jitter (RMS)					35					ps
t_{PLH}	Propagation Delay @ 1.5 V	2.0		5.5	2.0		5.5	2.0		5.5	ns
t_{PHL}	Propagation Delay @ 1.5 V	2.0		5.5	2.0		5.5	2.0		5.5	ns
V_{PP}	Input Swing (Note 7)	200		1000	200		1000	200		1000	mV
t_r/t_f	Output Rise/Fall Time (10–90%)					750					ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. $R_L = 500 \Omega$ to GND and $C_L = 20 \text{ pF}$ to GND. Refer to Figure 2.

7. $V_{PP}(\text{min})$ is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈ 40 .

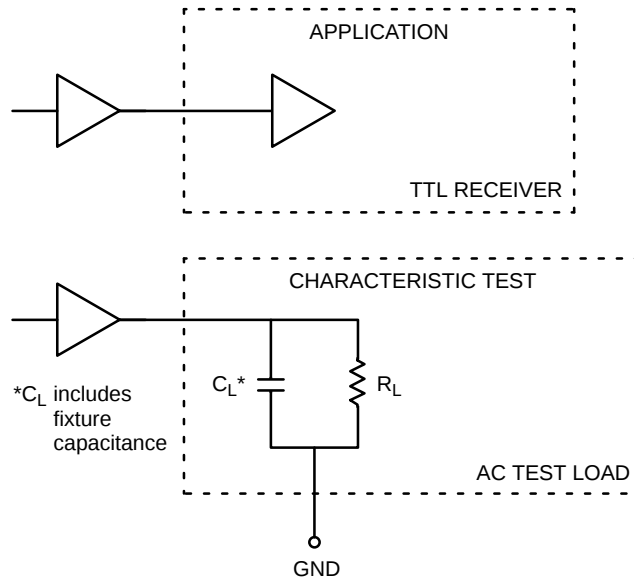


Figure 2. TTL Output Loading Used for Device Evaluation

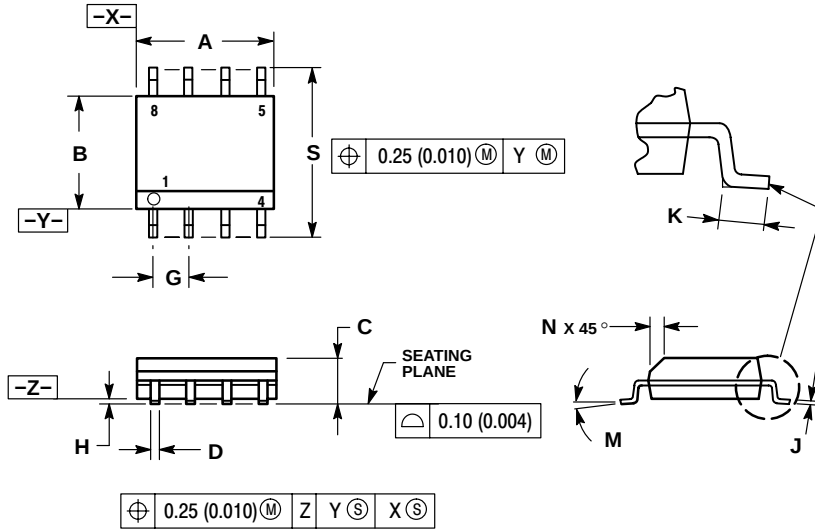
Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1560** – Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

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PACKAGE DIMENSIONS

SOIC-8 D SUFFIX PLASTIC SOIC PACKAGE CASE 751-07 ISSUE AB

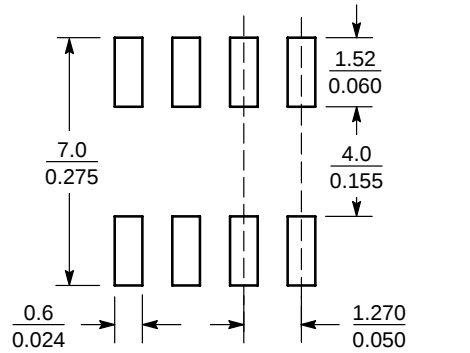


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT



SO-8

SCALE 6:1 (mm/inches)

