

# MC100LVEL32

## 3.3V ECL ÷2 Divider

The MC100LVEL32 is an integrated ÷2 divider. The LVEL32 is functionally identical to the EL32, but operates from a 3.3 V supply.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flop will attain a random state; the reset allows for the synchronization of multiple LVEL32's in a system.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

- 510 ps Propagation Delay
- 2.6 GHz Typical Maximum Frequency
- ESD Protection: Human Body Model; >4 kV, Machine Model; >200 V
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:  
 $V_{CC} = 3.0$  V to 3.8 V with  $V_{EE} = 0$  V
- NECL Mode Operating Range:  
 $V_{CC} = 0$  V with  $V_{EE} = -3.0$  V to  $-3.8$  V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1  
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 111 devices
- Pb-Free Packages are Available



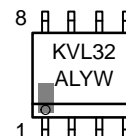
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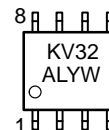
### MARKING DIAGRAMS\*



SOIC-8  
D SUFFIX  
CASE 751



TSSOP-8  
DT SUFFIX  
CASE 948R



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# MC100LEVEL32

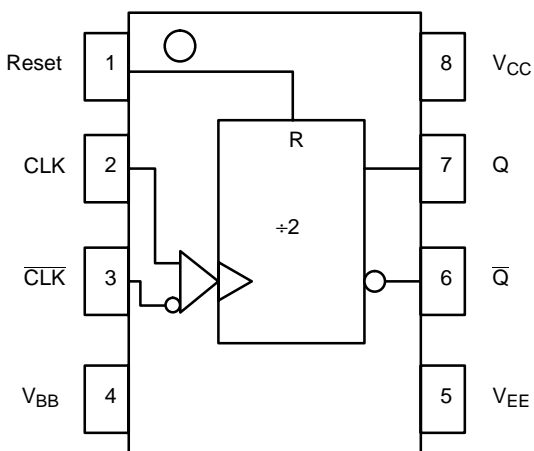


Figure 1. Logic Diagram and Pinout Assessment

Table 1. PIN DESCRIPTION

Pin	Function
CLK*, $\overline{\text{CLK}}^{**}$	ECL Differential Clock Inputs
Q, $\overline{\text{Q}}$	ECL Differential Data +2 Outputs
Reset	ECL Asynch Reset
$V_{\text{BB}}$	Reference Voltage Output
$V_{\text{CC}}$	Positive Supply
$V_{\text{EE}}$	Negative Supply

\*Pin will default low when left open, per internal 75 K pull-down to  $V_{\text{EE}}$ .

\*\* Pin will default to  $V_{\text{CC}}/2$  when left open per internal 75 K $\Omega$  pull-down to  $V_{\text{EE}}$  and 75 K $\Omega$  pull-up to  $V_{\text{CC}}$ .

Table 2. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{\text{CC}}$	PECL Mode Power Supply	$V_{\text{EE}} = 0 \text{ V}$		8 to 0	V
$V_{\text{EE}}$	NECL Mode Power Supply	$V_{\text{CC}} = 0 \text{ V}$		-8 to 0	V
$V_{\text{I}}$	PECL Mode Input Voltage	$V_{\text{EE}} = 0 \text{ V}$	$V_{\text{I}} \leq V_{\text{CC}}$	6 to 0	V
$V_{\text{I}}$	NECL Mode Input Voltage	$V_{\text{CC}} = 0 \text{ V}$	$V_{\text{I}} \geq V_{\text{EE}}$	-6 to 0	V
$V_{\text{I}}$	PECL Mode Input Voltage	$V_{\text{EE}} = 0 \text{ V}$	$V_{\text{I}} \leq V_{\text{CC}}$	6 to 0	V
$V_{\text{I}}$	NECL Mode Input Voltage	$V_{\text{CC}} = 0 \text{ V}$	$V_{\text{I}} \geq V_{\text{EE}}$	-6 to 0	V
$I_{\text{out}}$	Output Current	Continuous		50	mA
		Surge		100	mA
$I_{\text{BB}}$	$V_{\text{BB}}$ Sink/Source			$\pm 0.5$	mA
$T_{\text{A}}$	Operating Temperature Range			-40 to +85	$^{\circ}\text{C}$
$T_{\text{stg}}$	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
$\theta_{\text{JA}}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm	SOIC-8	190	$^{\circ}\text{C}/\text{W}$
		500 lfpm	SOIC-8	130	$^{\circ}\text{C}/\text{W}$
$\theta_{\text{JC}}$	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8	41 to 44 $\pm 5\%$	$^{\circ}\text{C}/\text{W}$
$\theta_{\text{JA}}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm	TSSOP-8	185	$^{\circ}\text{C}/\text{W}$
		500 lfpm	TSSOP-8	140	$^{\circ}\text{C}/\text{W}$
$\theta_{\text{JC}}$	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44 $\pm 5\%$	$^{\circ}\text{C}/\text{W}$
$T_{\text{sol}}$	Wave Solder	<2 to 3 sec @ 248 $^{\circ}\text{C}$		265	$^{\circ}\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

# MC100LEVEL32

**Table 3. LVPECL DC CHARACTERISTICS**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  (Note 1)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		29	35		29	35		31	36	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
$V_{OL}$	Output LOW Voltage (Note 2)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	1490		1825	mV
$V_{BB}$	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 6) $V_{PP} < 500\text{ mV}$ $V_{PP} \geq 500\text{ mV}$	1.2		3.1	1.1		3.1	1.1		3.1	V
		1.4		3.1	1.3		3.1	1.3		3.1	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current				0.5			0.5			$\mu\text{A}$
		$\frac{CLK}{CLK}$	-600			-600			-600		$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
2. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and  $1\text{ V}$ .

**Table 4. LVNECL DC CHARACTERISTICS**  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 4)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		29	35		29	35		31	36	mA
$V_{OH}$	Output HIGH Voltage (Note 5)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
$V_{OL}$	Output LOW Voltage (Note 5)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
$V_{BB}$	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 6) $V_{PP} < 500\text{ mV}$ $V_{PP} \geq 500\text{ mV}$	-2.1		-0.2	-2.1		-0.2	-2.1		-0.2	V
		-1.9		-0.2	-1.9		-0.2	-1.9		-0.2	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current				0.5			0.5			$\mu\text{A}$
		$\frac{CLK}{CLK}$	-600			-600			-600		$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
5. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
6.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and  $1\text{ V}$ .

# MC100LVEL32

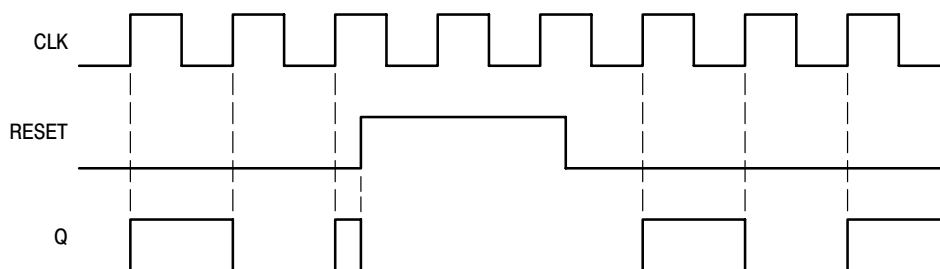
**Table 5. AC CHARACTERISTICS**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 7)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\max}$	Maximum Toggle Frequency	2.2	2.5		2.4	2.6		2.6	2.8		GHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CLK to Q (Differential) CLK to Q (Single-Ended) Reset to Q	350 300 440	500 500 555	530 580 640	370 320 450	510 510 540	550 600 650	410 360 480	540 540 580	590 640 680	ps
$t_{\text{RR}}$	Reset Recovery	175	50		175	50		175	50		ps
$t_{\text{PW}}$	Minimum Pulse Width Reset	500	300		500	300		500	300		ps
$t_{\text{JITTER}}$	Random Clock Jitter (RMS)		2.0			2.0			2.0		ps
$V_{\text{PP}}$	Input Swing (Differential Swing) (Note 8)	150		1000	150		1000	150		1000	mV
$t_r$ $t_f$	Output Rise/Fall Times Q (20% – 80%)	120	225	320	120	225	320	120	225	320	ps

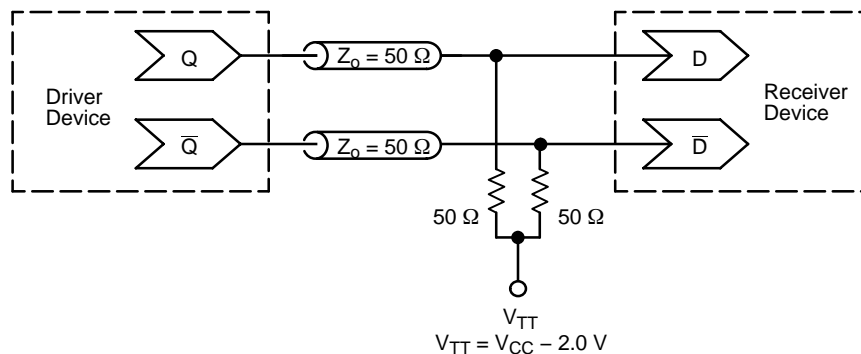
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7.  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .

8.  $V_{\text{PP}}(\text{min})$  is input swing measured single-ended on each input in differential configuration.



**Figure 1. Timing Diagram**



**Figure 2. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

# MC100LVEL32

## ORDERING INFORMATION

Device	Package	Package†
MC100LVEL32D	SO-8	98 Units / Rail
MC100LVEL32DR2	SO-8	2500 / Tape & Reel
MC100LVEL32DR2G	SO-8 (Pb-Free)	2500 / Tape & Reel
MC100LVEL32DT	TSSOP-8	98 Units / Rail
MC100LVEL32DTG	TSSOP-8 (Pb-Free)	98 Units / Rail
MC100LVEL32DTR2	TSSOP-8	2500 / Tape & Reel
MC100LVEL32DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

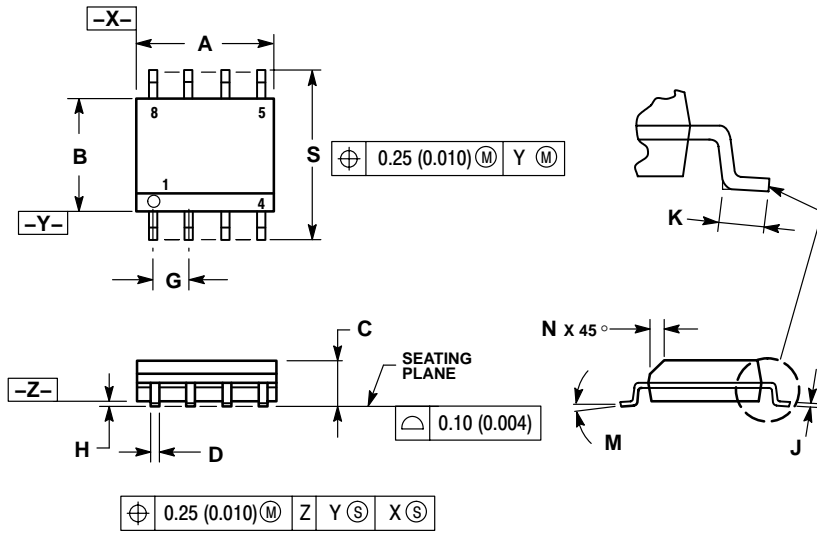
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1642/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC100LEVEL32

## PACKAGE DIMENSIONS

SOIC-8 NB  
D SUFFIX  
CASE 751-07  
ISSUE AC

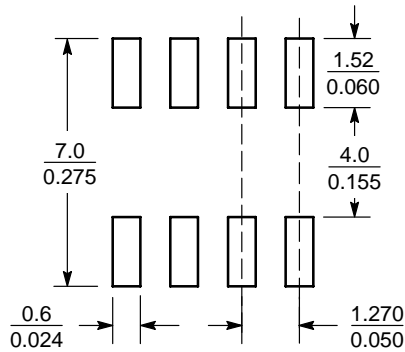


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



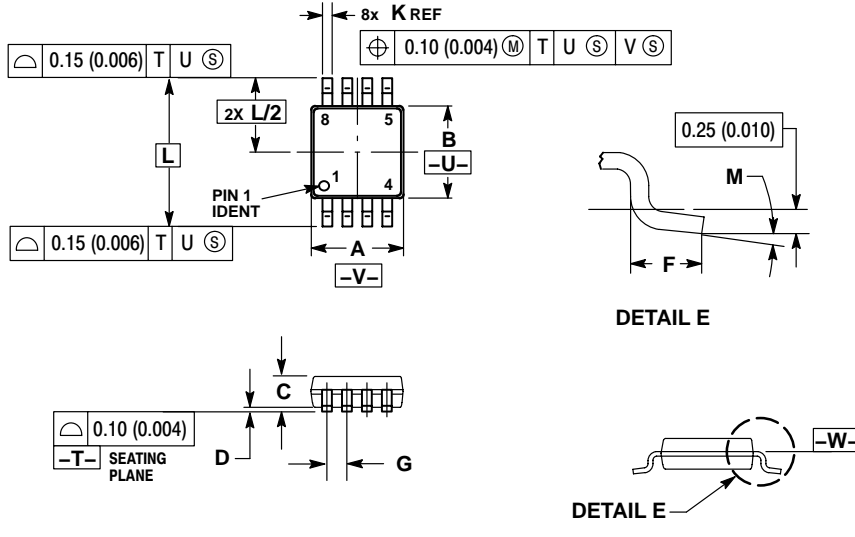
SCALE 6:1 ( $\frac{\text{mm}}{\text{inches}}$ )

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC100LVEL32

## PACKAGE DIMENSIONS

TSSOP-8  
DT SUFFIX  
PLASTIC TSSOP PACKAGE  
CASE 948R-02  
ISSUE A




### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

# MC100LVEL32

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