

74HC595

8-Bit Serial-Input/Serial or Parallel-Output Shift Register with Latched 3-State Outputs

High-Performance Silicon-Gate CMOS

The 74HC595 consists of an 8-bit shift register and an 8-bit D-type latch with three-state parallel outputs. The shift register accepts serial data and provides a serial output. The shift register also provides parallel data to the 8-bit latch. The shift register and latch have independent clock inputs. This device also has an asynchronous reset for the shift register.

The HC595 directly interfaces with the SPI serial data port on CMOS MPUs and MCUs.

Features

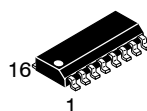
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 328 FETs or 82 Equivalent Gates
- Improvements over HC595
 - Improved Propagation Delays
 - 50% Lower Quiescent Power
 - Improved Input Noise and Latchup Immunity
- These are Pb-Free Devices



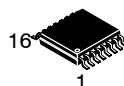
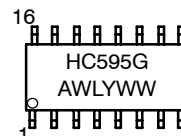
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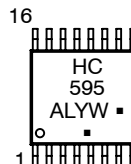
MARKING DIAGRAMS



SOIC-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F

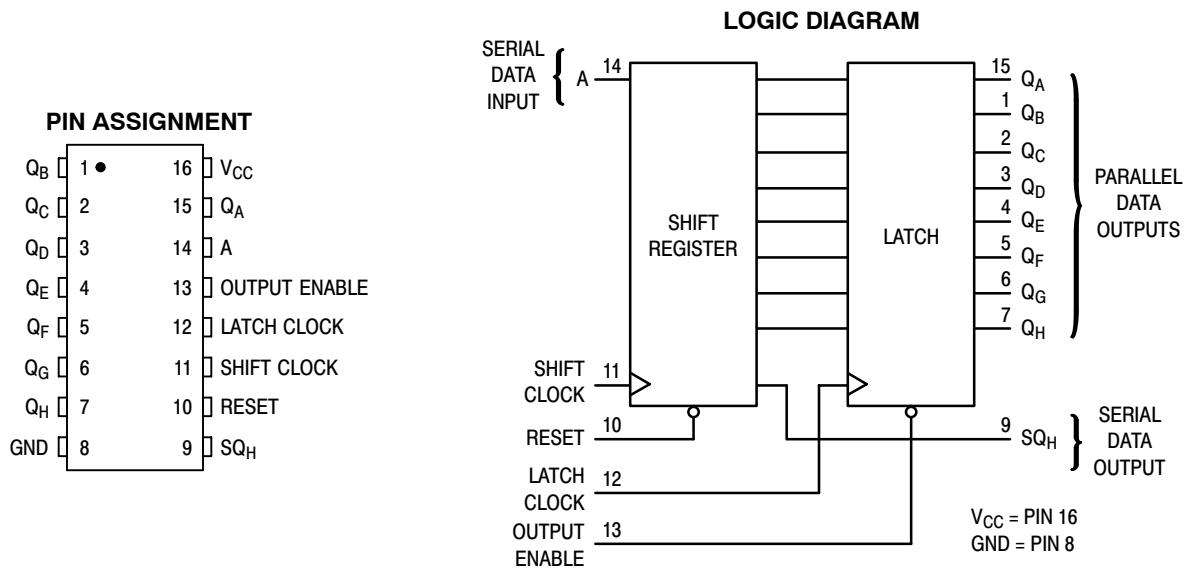


HC595 = Device Code
A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ■ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

74HC595



ORDERING INFORMATION

Device	Package	Shipping [†]
74HC595DR2G	SOIC-16 (Pb-Free)	2500 Tape & Reel
74HC595DTR2G	TSSOP-16*	2500 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or TSSOP Package)	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C

TSSOP Package: – 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C
t _p , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 1000 500 400	ns

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} (V)	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} – 0.1 V I _{out} ≤ 20 µA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} – 0.1 V I _{out} ≤ 20 µA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V _{OH}	Minimum High-Level Output Voltage, Q _A – Q _H	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 µA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA	3.0	2.48	2.34	2.2	
		I _{out} ≤ 6.0 mA	4.5	3.98	3.84	3.7	
		I _{out} ≤ 7.8 mA	6.0	5.48	5.34	5.2	
V _{OL}	Maximum Low-Level Output Voltage, Q _A – Q _H	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 µA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA	3.0	0.26	0.33	0.4	
		I _{out} ≤ 6.0 mA	4.5	0.26	0.33	0.4	
		I _{out} ≤ 7.8 mA	6.0	0.26	0.33	0.4	
V _{OH}	Minimum High-Level Output Voltage, SQ _H	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 µA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA	3.0	2.98	2.34	2.2	
		I _{out} ≤ 4.0 mA	4.5	3.98	3.84	3.7	
		I _{out} ≤ 5.2 mA	6.0	5.48	5.34	5.2	
V _{OL}	Maximum Low-Level Output Voltage, SQ _H	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 µA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 2.4 mA	3.0	0.26	0.33	0.4	
		I _{out} ≤ 4.0 mA	4.5	0.26	0.33	0.4	
		I _{out} ≤ 5.2 mA	6.0	0.26	0.33	0.4	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	µA
I _{OZ}	Maximum Three-State Leakage Current, Q _A – Q _H	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	6.0	±0.25	±2.5	±2.5	µA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 µA	6.0	4.0	40	40	µA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Symbol	Parameter	V _{CC} (V)	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Shift Clock to SQ _H (Figures 1 and 7)	2.0 3.0 4.5 6.0	140 100 28 24	175 125 35 30	210 150 42 36	ns
t _{PHL}	Maximum Propagation Delay, Reset to SQ _H (Figures 2 and 7)	2.0 3.0 4.5 6.0	145 100 29 25	180 125 36 31	220 150 44 38	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Clock to Q _A – Q _H (Figures 3 and 7)	2.0 3.0 4.5 6.0	140 100 28 24	175 125 35 30	210 150 42 36	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q _A – Q _H (Figures 4 and 8)	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q _A – Q _H (Figures 4 and 8)	2.0 3.0 4.5 6.0	135 90 27 23	170 110 34 29	205 130 41 35	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Q _A – Q _H (Figures 3 and 7)	2.0 3.0 4.5 6.0	60 23 12 10	75 27 15 13	90 31 18 15	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, SQ _H (Figures 1 and 7)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C _{in}	Maximum Input Capacitance	–	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State), Q _A – Q _H	–	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V _{CC} = 5.0 V	
		300	
		pF	

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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TIMING REQUIREMENTS (Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	V _{CC} (V)	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{su}	Minimum Setup Time, Serial Data Input A to Shift Clock (Figure 5)	2.0	50	65	75	ns
		3.0	40	50	60	
		4.5	10	13	15	
		6.0	9.0	11	13	
t _{su}	Minimum Setup Time, Shift Clock to Latch Clock (Figure 6)	2.0	75	95	110	ns
		3.0	60	70	80	
		4.5	15	19	22	
		6.0	13	16	19	
t _h	Minimum Hold Time, Shift Clock to Serial Data Input A (Figure 5)	2.0	5.0	5.0	5.0	ns
		3.0	5.0	5.0	5.0	
		4.5	5.0	5.0	5.0	
		6.0	5.0	5.0	5.0	
t _{rec}	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 2)	2.0	50	65	75	ns
		3.0	40	50	60	
		4.5	10	13	15	
		6.0	9.0	11	13	
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0	60	75	90	ns
		3.0	45	60	70	
		4.5	12	15	18	
		6.0	10	13	15	
t _w	Minimum Pulse Width, Shift Clock (Figure 1)	2.0	50	65	75	ns
		3.0	40	50	60	
		4.5	10	13	15	
		6.0	9.0	11	13	
t _w	Minimum Pulse Width, Latch Clock (Figure 6)	2.0	50	65	75	ns
		3.0	40	50	60	
		4.5	10	13	15	
		6.0	9.0	11	13	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

FUNCTION TABLE

Operation	Inputs					Resulting Function			
	Reset	Serial Input A	Shift Clock	Latch Clock	Output Enable	Shift Register Contents	Latch Register Contents	Serial Output SQ _H	Parallel Outputs Q _A – Q _H
Reset shift register	L	X	X	L, H, ↓	L	L	U	L	U
Shift data into shift register	H	D	↑	L, H, ↓	L	D→SR _A ; SR _N →SR _{N+1}	U	SR _G →SR _H	U
Shift register remains unchanged	H	X	L, H, ↓	L, H, ↓	L	U	U	U	U
Transfer shift register contents to latch register	H	X	L, H, ↓	↑	L	U	SR _N →LR _N	U	SR _N
Latch register remains unchanged	X	X	X	L, H, ↓	L	*	U	*	U
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled
Force outputs into high impedance state	X	X	X	X	H	*	**	*	Z

SR = shift register contents
LR = latch register contents

D = data (L, H) logic level
U = remains unchanged

↑ = Low-to-High
↓ = High-to-Low

* = depends on Reset and Shift Clock inputs
** = depends on Latch Clock input

PIN DESCRIPTIONS

INPUTS A (Pin 14)

Serial Data Input. The data on this pin is shifted into the 8-bit serial shift register.

CONTROL INPUTS Shift Clock (Pin 11)

Shift Register Clock Input. A low-to-high transition on this input causes the data at the Serial Input pin to be shifted into the 8-bit shift register.

Reset (Pin 10)

Active-low, Asynchronous, Shift Register Reset Input. A low on this pin resets the shift register portion of this device only. The 8-bit latch is not affected.

Latch Clock (Pin 12)

Storage Latch Clock Input. A low-to-high transition on this input latches the shift register data.

Output Enable (Pin 13)

Active-low Output Enable. A low on this input allows the data from the latches to be presented at the outputs. A high on this input forces the outputs (Q_A–Q_H) into the high-impedance state. The serial output is not affected by this control unit.

OUTPUTS Q_A – Q_H (Pins 15, 1, 2, 3, 4, 5, 6, 7)

Noninverted, 3-state, latch outputs.

SQ_H (Pin 9)

Noninverted, Serial Data Output. This is the output of the eighth stage of the 8-bit shift register. This output does not have three-state capability.

SWITCHING WAVEFORMS

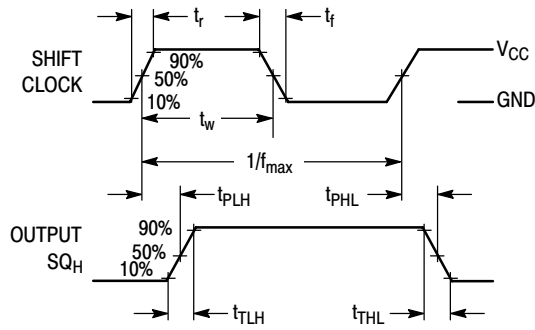


Figure 1.

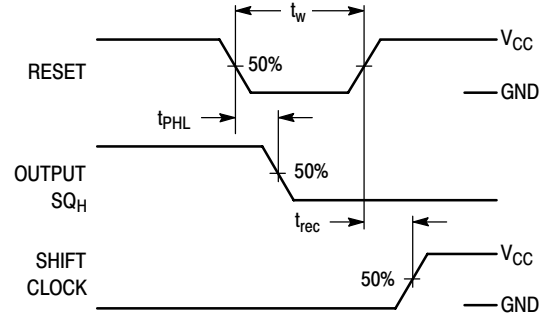


Figure 2.

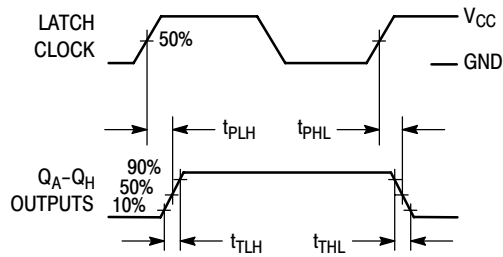


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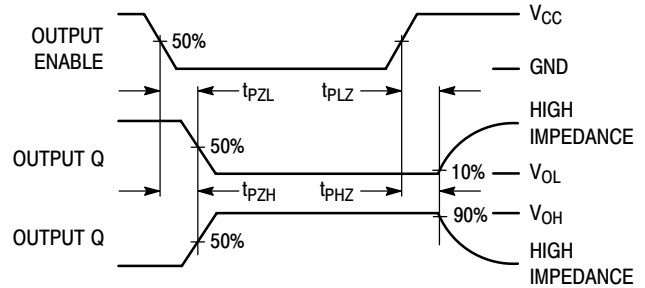


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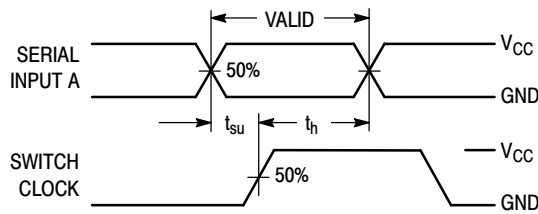


Figure 5.

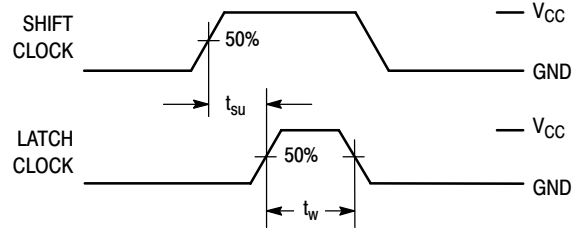
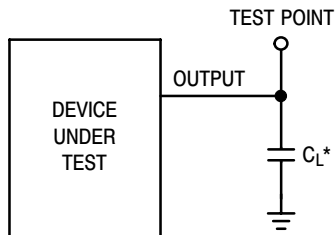


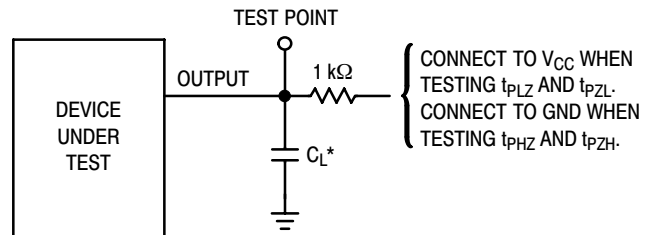
Figure 6.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 7.

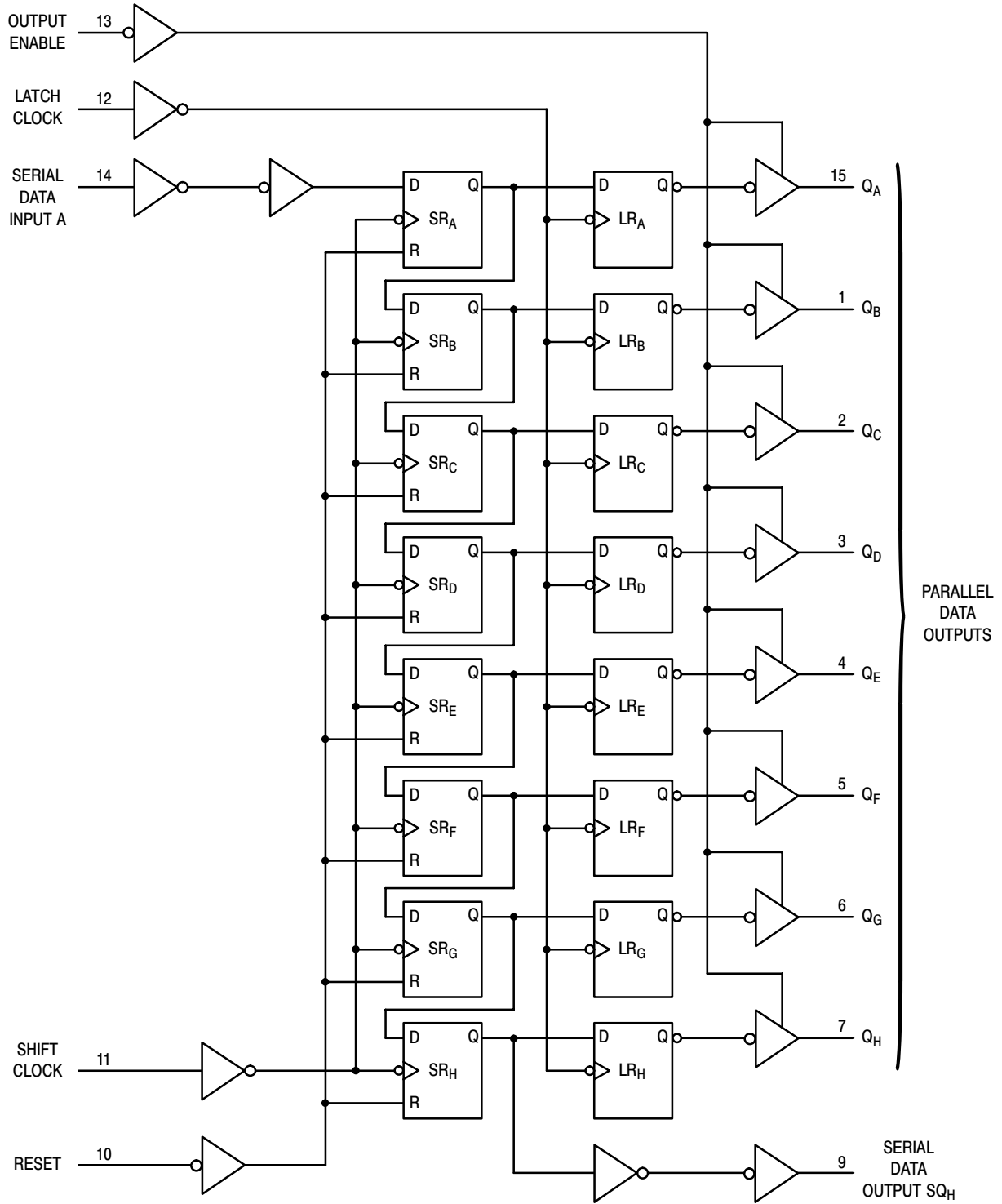


*Includes all probe and jig capacitance

Figure 8.

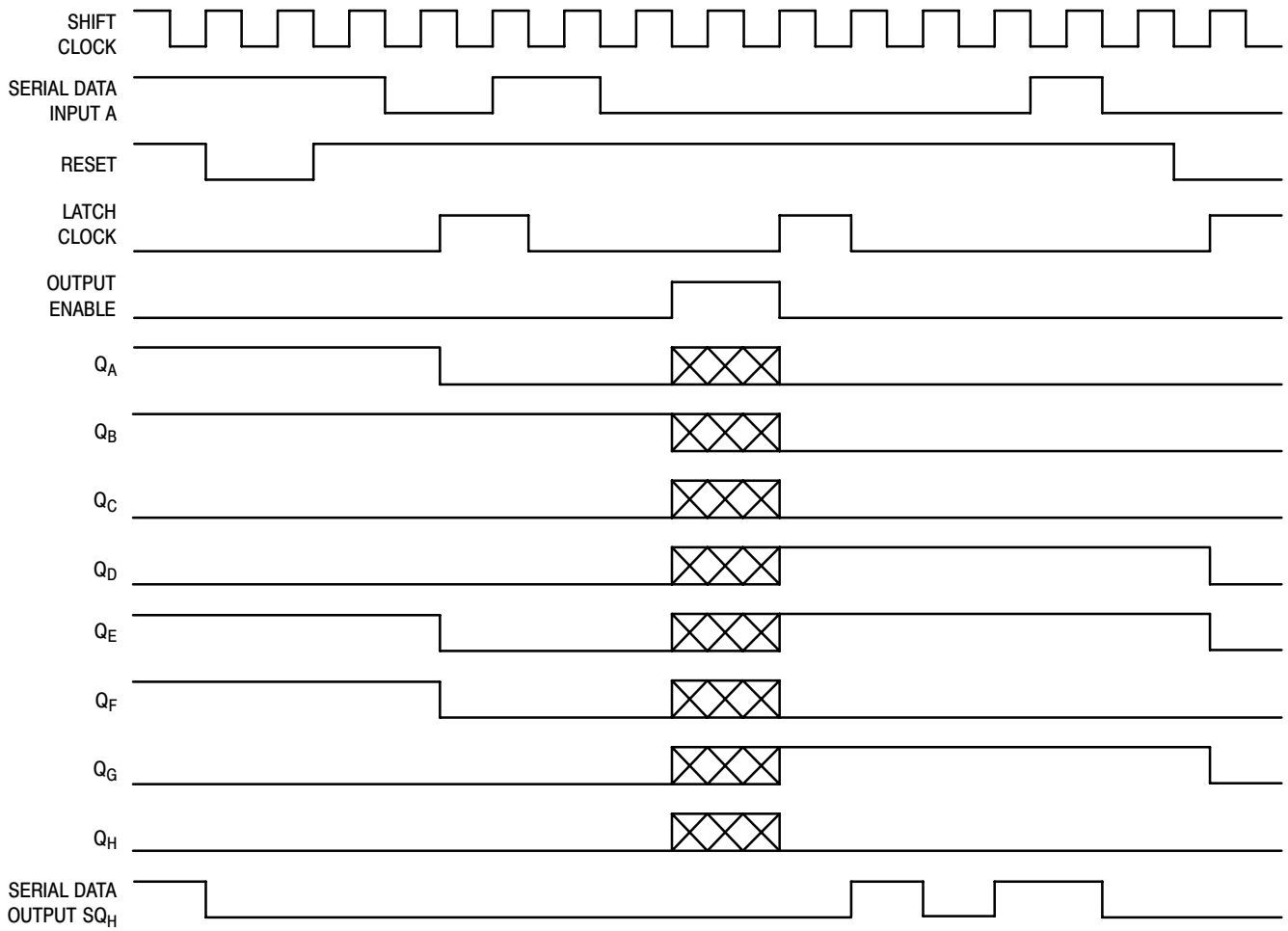
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EXPANDED LOGIC DIAGRAM



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TIMING DIAGRAM

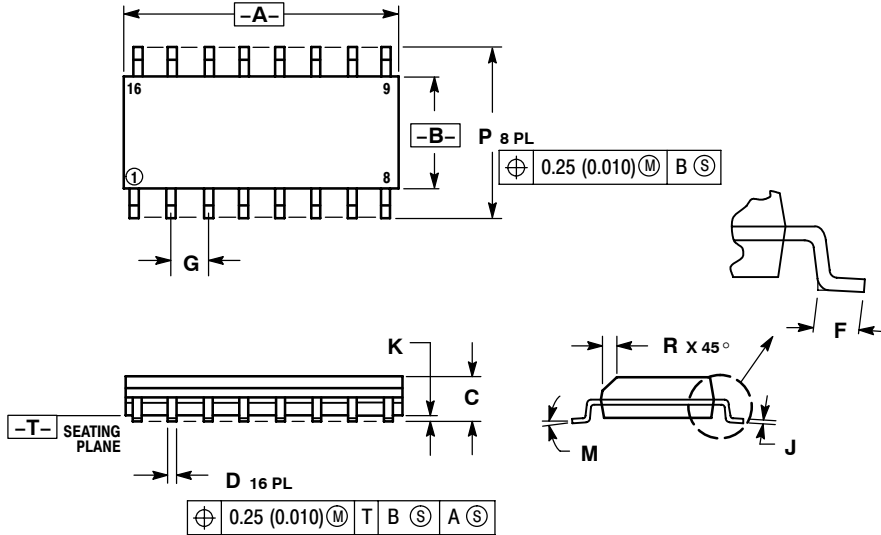


NOTE:  implies that the output is in a high-impedance state.

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PACKAGE DIMENSIONS

SOIC-16
CASE 751B-05
ISSUE K

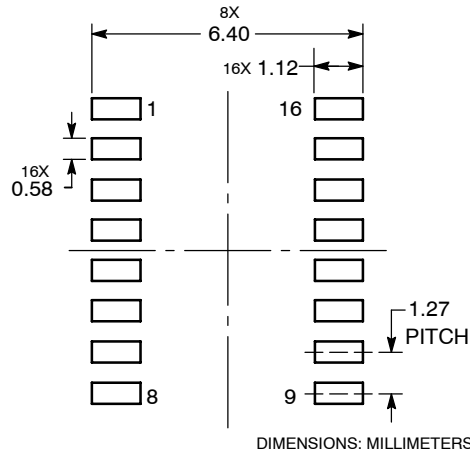


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*



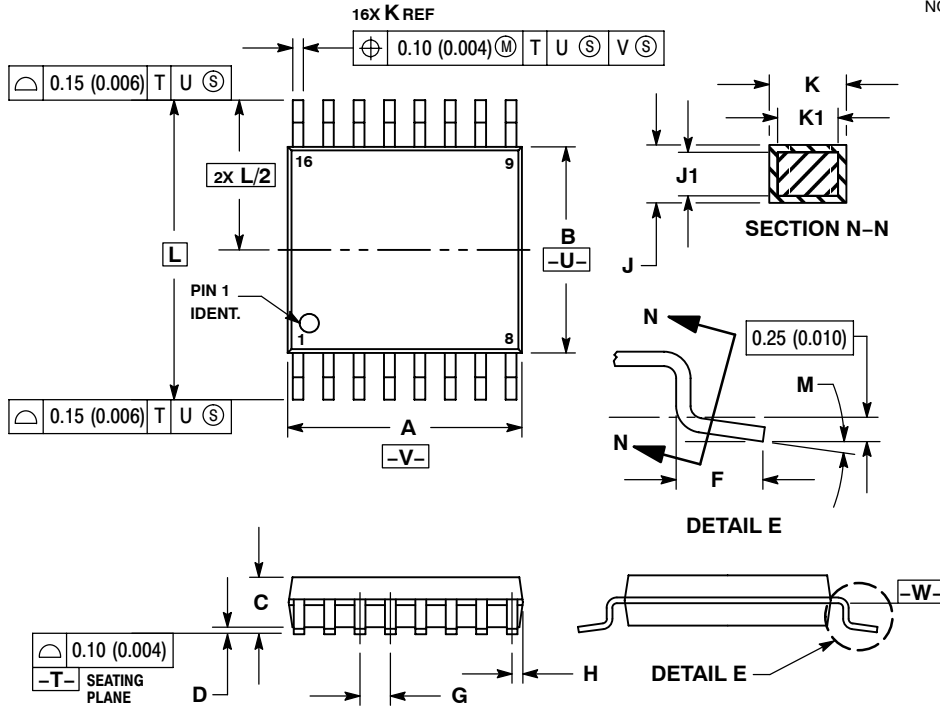
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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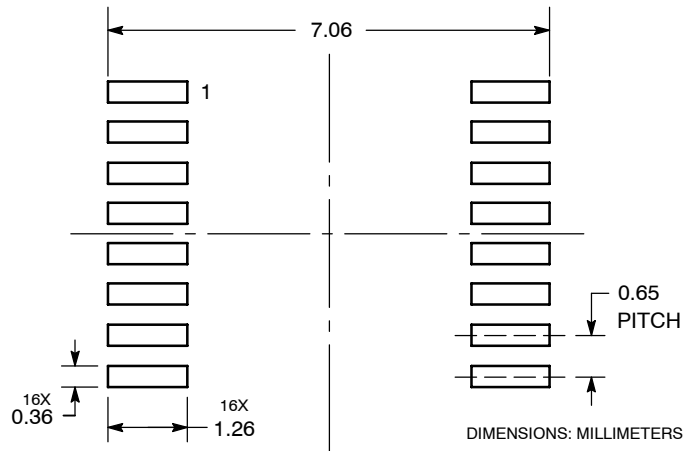
PACKAGE DIMENSIONS

TSSOP-16
CASE 948F-01
ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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