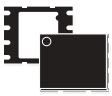
M25PE40

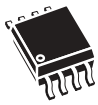
4 Mbit, page-erasable serial Flash memory with byte alterability, 75 MHz SPI bus, standard pinout

Features

- SPI bus compatible serial interface
- 4 Mbit page-erasable Flash memory
- Page size: 256 bytes
  - Page Write in 11 ms (typical)
  - Page Program in 0.8 ms (typical)
  - Page Erase in 10 ms (typical)
- Subsector Erase (4 Kbytes)
- Sector Erase (64 Kbytes)
- Bulk Erase (4 Mbits)
- 2.7 V to 3.6 V single supply voltage
- 75 MHz clock rate (maximum)
- Deep Power-down mode 1 µA (typical)
- Electronic signature
  - JEDEC standard two-byte signature (8013h)
- Software write protection on a 64-Kbyte sector basis
- Hardware write protection of the memory area selected using the BP0, BP1 and BP2 bits
- More than 100 000 Write cycles
- More than 20 year data retention
- Packages
  - ECOPACK® (RoHS compliant)



VFQFPN8 (MP)
6 × 5 mm (MLP8)



SO8W (MW) 208 mils

SO8N (MN) 150 mils

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1 Description

The M25PE40 is a 4 Mbit (512Kbit × 8 bit) serial paged Flash memory accessed by a high speed SPI-compatible bus.

The memory can be written or programmed 1 to 256 bytes at a time, using the Page Write or Page Program instruction. The Page Write instruction consists of an integrated Page Erase cycle followed by a Page Program cycle.

The memory is organized as 8 sectors that are further divided up into 16 subsectors each (128 subsectors in total). Each sector contains 256 pages and each subsector contains 16 pages. Each page is 256 bytes wide. Thus, the whole memory can be viewed as consisting of 2048 pages, or 524,288 bytes.

The memory can be erased a page at a time, using the Page Erase instruction, a subsector at a time, using the Subsector Erase instruction, a sector at a time, using the Sector Erase instruction or as a whole, using the Bulk Erase (BE) instruction.

The memory can be write protected by either hardware or software using a mix of volatile and non-volatile protection features, depending on the application needs. The protection granularity is of 64 Kbytes (sector granularity).

Important note

This datasheet details the functionality of the devices, based on the previous T7X process or based on the current T9HX process (available since July 2007). Delivery of parts operating with a maximum clock rate of 75 MHz starts from week 8 of 2008.

What are the changes?

The M25PE40 in T9HX process offers the following additional features:

- the whole memory array is partitioned into 4-Kbyte subsectors
- five new instructions: Write Status Register (WRSR), Write to Lock Register (WRLR), Read Lock Register (RDLR), 4-Kbyte Subsector Erase (SSE) and Bulk Erase (BE)
- Status Register: 4 bits can be written (BP0, BP1, BP2, SRWD)
- $\overline{WP}$ input (pin 3): write protection limits are extended, depending on the value of the BP0, BP1, BP2, SRWD bits. The $\overline{WP}$ write protection remains the same if bits (BP2, BP1, BP0) are set to (0, 0, 1)
- smaller die size allowing assembly into an SO8N package.

Figure 1. Logic diagram - previous T7X process

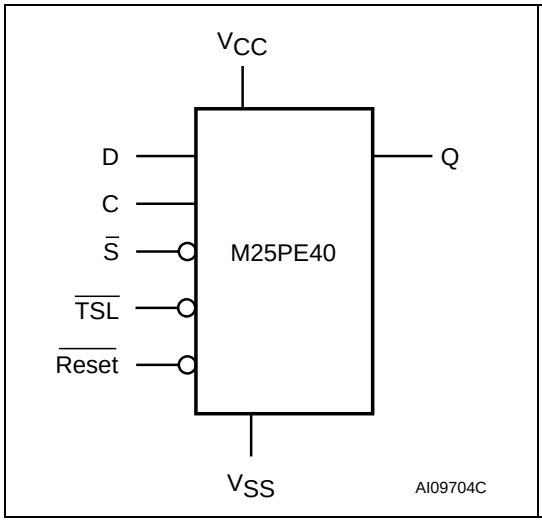


Figure 2. Logic diagram - new T9HX process

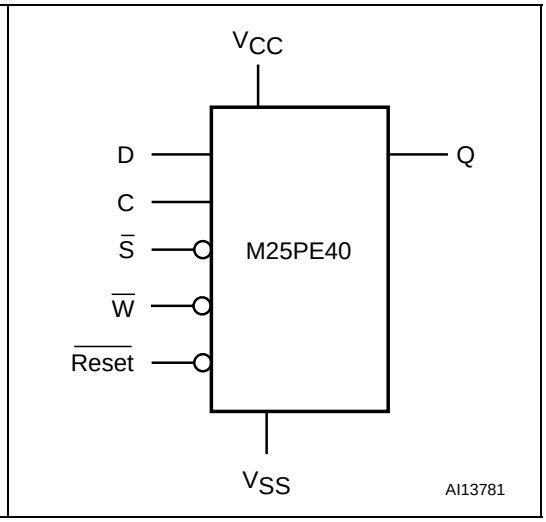
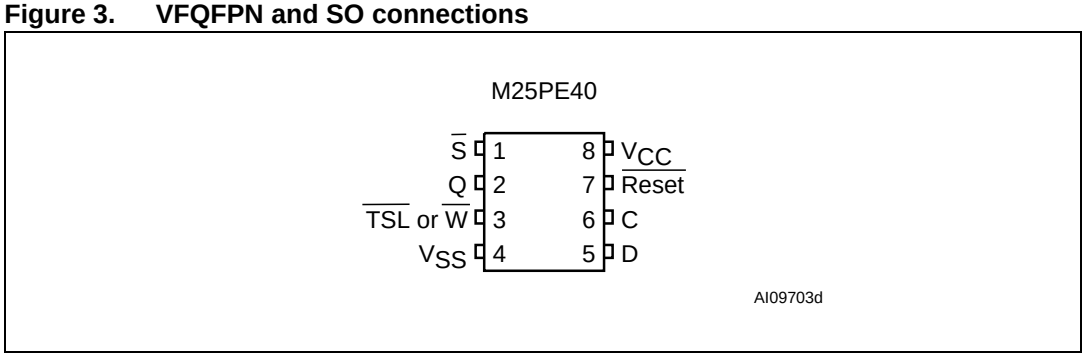


Table 1. Signal names

Signal name	Function	Direction
C	Serial Clock	Input
D	Serial Data input	Input
Q	Serial Data output	Output
S	Chip Select	Input
TSL or $\overline{W}$(1)	Top Sector Lock or Write Protect	Input
$\overline{Reset}$	Reset	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

1. In the previous T7X process the pin is a Top Sector Lock input whereas in the new T9HX process, the pin is a Write Protect input (see *Figure 1* and *Figure 2*).

Figure 3. VFQFPN and SO connections



1. There is an exposed central pad on the underside of the VFQFPN package. This is pulled, internally, to V_{SS}, and must not be allowed to be connected to any other voltage or signal line on the PCB.
2. See *Section 12: Package mechanical* for package dimensions, and how to identify pin-1.

2 Signal description

2.1 Serial Data output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

2.2 Serial Data input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (C).

2.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data output (Q) changes after the falling edge of Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

When this input signal is High, the device is deselected and Serial Data output (Q) is at high impedance. Unless an internal Read, Program, Erase or Write cycle is in progress, the device will be in the Standby Power mode (this is not the Deep Power-down mode). Driving Chip Select ($\overline{S}$) Low selects the device, placing it in the Active Power mode.

After power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

2.5 Reset ($\overline{Reset}$)

The Reset ($\overline{Reset}$) input provides a hardware reset for the memory.

When Reset ($\overline{Reset}$) is driven High, the memory is in the normal operating mode. When Reset ($\overline{Reset}$) is driven Low, the memory will enter the Reset mode. In this mode, the output is high impedance.

Driving Reset ($\overline{Reset}$) Low while an internal operation is in progress will affect this operation (write, program or erase cycle) and data may be lost.

2.6 Write Protect ($\overline{W}$) or Top Sector Lock ($\overline{TSL}$)

- **The Write Protect function is available in the T9HX process only** (see *Important note on page 6*).

  The Write Protect ($\overline{W}$) input is used to freeze the size of the area of memory that is protected against write, program and erase instructions (as specified by the values in the BP2, BP1 and BP0 bits of the Status Register. See *Section 6.4: Read Status Register (RDSR)* for a description of these bits.

- **The Top Sector Lock function is available in the T7X process only (see *Important note on page 6*).**

  The input signal sets the device in the Hardware Protected mode, when Top Sector Lock ($\overline{TSL}$) is connected to V_{SS}, causing the top 256 pages (upper addresses) of the memory to become read-only (protected from write, program and erase operations).

  When Top Sector Lock ($\overline{TSL}$) is connected to V_{CC}, the top 256 pages of memory behave like the other pages of memory.

2.7 V_{CC} supply voltage

V_{CC} is the supply voltage.

2.8 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

3 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

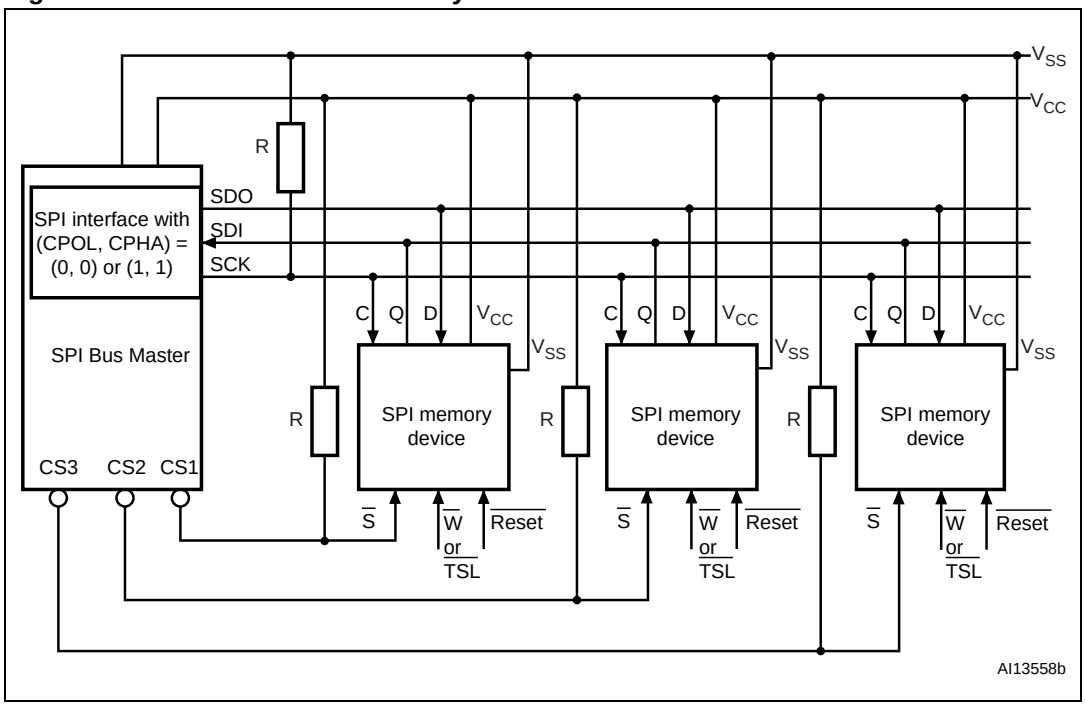
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 5*, is the clock polarity when the bus master is in Standby mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 4. Bus master and memory devices on the SPI bus

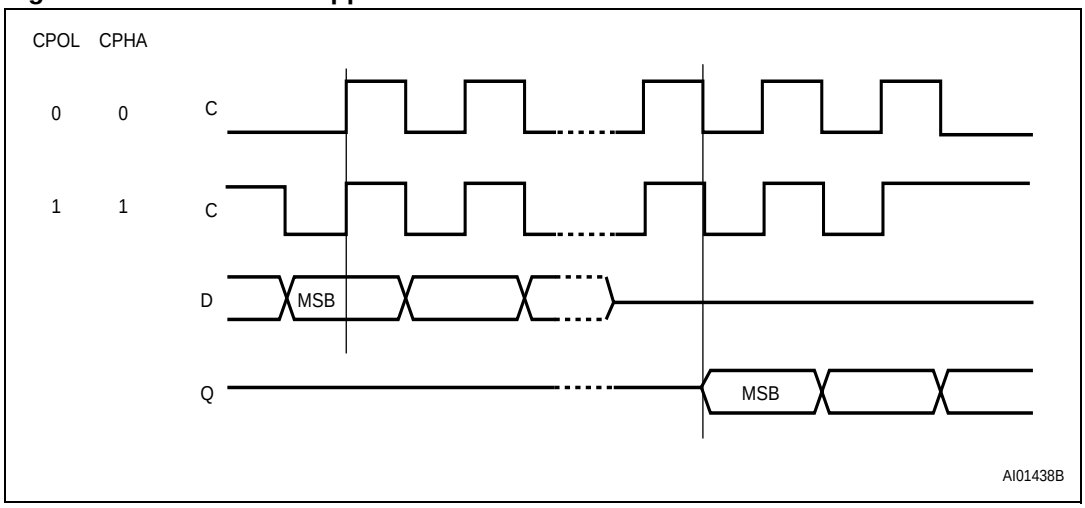


1. The Write Protect or Top Sector Lock ($\overline{W}$ or $\overline{TSL}$) signal should be driven, High or Low as appropriate.

Figure 4 shows an example of three devices connected to an MCU, on an SPI bus. Only one device is selected at a time, so only one device drives the Serial Data output (Q) line at a time, the other devices are high impedance. Resistors R (represented in *Figure 4*) ensure that the M25PE40 is not selected if the Bus Master leaves the $\overline{S}$ line in the high impedance state. As the Bus Master may enter a state where all inputs/outputs are in high impedance at the same time (for example, when the Bus Master is reset), the clock line (C) must be connected to an external pull-down resistor so that, when all inputs/outputs become high impedance, the $\overline{S}$ line is pulled High while the C line is pulled Low (thus ensuring that $\overline{S}$ and C do not become High at the same time, and so, that the t_{SHCH} requirement is met). The typical value of R is 100 kΩ, assuming that the time constant $R*C_p$ (C_p = parasitic capacitance of the bus line) is shorter than the time during which the Bus Master leaves the SPI bus in high impedance.

Example: C_p = 50 pF, that is R*C_p = 5 µs <=> the application must ensure that the Bus Master never leaves the SPI bus in the high impedance state for a time period shorter than 5 µs.

Figure 5. SPI modes supported



4 Operating features

4.1 Sharing the overhead of modifying data

To write or program one (or more) data bytes, two instructions are required: Write Enable (WREN), which is one byte, and a Page Write (PW) or Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal cycle (of duration t_{PW} or t_{PP}).

To share this overhead, the Page Write (PW) or Page Program (PP) instruction allows up to 256 bytes to be programmed (changing bits from 1 to 0) or written (changing bits to 0 or 1) at a time, provided that they lie in consecutive addresses on the same page of memory.

4.2 An easy way to modify data

The Page Write (PW) instruction provides a convenient way of modifying data (up to 256 contiguous bytes at a time), and simply requires the start address, and the new data in the instruction sequence.

The Page Write (PW) instruction is entered by driving Chip Select ($\overline{S}$) Low, and then transmitting the instruction byte, three address bytes (A23-A0) and at least one data byte, and then driving Chip Select ($\overline{S}$) High. While Chip Select ($\overline{S}$) is being held Low, the data bytes are written to the data buffer, starting at the address given in the third address byte (A7-A0). When Chip Select ($\overline{S}$) is driven High, the Write cycle starts. The remaining, unchanged, bytes of the data buffer are automatically loaded with the values of the corresponding bytes of the addressed memory page. The addressed memory page then automatically put into an erase cycle. Finally, the addressed memory page is programmed with the contents of the data buffer.

All of this buffer management is handled internally, and is transparent to the user. The user is given the facility of being able to alter the contents of the memory on a byte-by-byte basis.

For optimized timings, it is recommended to use the Page Write (PW) instruction to write all consecutive targeted bytes in a single sequence versus using several Page Write (PW) sequences with each containing only a few bytes (see *Section 6.9: Page Write (PW)*, *Table 21: AC characteristics (50 MHz operation, T9HX (0.11µm) process)*, and *Table 22: AC characteristics (75 MHz operation, T9HX (0.11µm) process)*).

4.3 A fast way to modify data

The Page Program (PP) instruction provides a fast way of modifying data (up to 256 contiguous bytes at a time), provided that it only involves resetting bits to 0 that had previously been set to '1'.

This might be:

- when the designer is programming the device for the first time
- when the designer knows that the page has already been erased by an earlier Page Erase (PE) or Sector Erase (SE) instruction. This is useful, for example, when storing a fast stream of data, having first performed the erase cycle when time was available
- when the designer knows that the only changes involve resetting bits to '0' that are still set to '1'. When this method is possible, it has the additional advantage of minimizing the number of unnecessary erase operations, and the extra stress incurred by each page.

For optimized timings, it is recommended to use the Page Program (PP) instruction to program all consecutive targeted bytes in a single sequence versus using several Page Program (PP) sequences with each containing only a few bytes (see *Section 6.10: Page Program (PP)*, *Table 21: AC characteristics (50 MHz operation, T9HX (0.11µm) process)*, and *Table 22: AC characteristics (75 MHz operation, T9HX (0.11µm) process)*).

4.4 Polling during a Write, Program or Erase cycle

A further improvement in the write, program or erase time can be achieved by not waiting for the worst case delay (t_{PW}, t_{PP}, t_{PE}, or t_{SE}). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous cycle is complete.

4.5 Reset

An internal Power-on Reset circuit helps protect against inadvertent data writes. Addition protection is provided by driving Reset ($\overline{\text{Reset}}$) Low during the power-on process, and only driving it High when V_{CC} has reached the correct voltage level, V_{CC}(min).

4.6 Active Power, Standby Power and Deep Power-down modes

When Chip Select ($\overline{S}$) is Low, the device is selected, and in the Active Power mode.

When Chip Select ($\overline{S}$) is High, the device is deselected, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write). The device then goes in to the Standby Power mode. The device consumption drops to I_{CC1}.

The Deep Power-down mode is entered when the specific instruction (the Deep Power-down (DP) instruction) is executed. The device consumption drops further to I_{CC2}. The device remains in this mode until the Release from Deep Power-down instruction is executed.

All other instructions are ignored while the device is in the Deep Power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program or Erase instructions.

4.7 Status Register

The Status Register contains a number of status and control bits that can be read or set (as appropriate) by using specific instructions. See *Section 6.4: Read Status Register (RDSR)* for a detailed description of the Status Register bits.

4.8 Protection modes

The environments where non-volatile memory devices are used can be very noisy. No SPI device can operate correctly in the presence of excessive noise. To help combat this, the features the following data protection mechanisms:

4.8.1 Protocol-related protections

- Power On Reset and an internal timer (t_{PUW}) can provide protection against inadvertent changes while the power supply is outside the operating specification.
- Program, Erase and Write instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Reset ($\overline{\text{Reset}}$) driven Low
  - Write Disable (WRDI) instruction completion
  - Page Write (PW) instruction completion
  - Page Program (PP) instruction completion
  - Write to Lock Register (WRLR) instruction completion
  - Page Erase (PE) instruction completion
  - Subsector Erase (SSE) instruction completion
  - Sector Erase (SE) instruction completion
  - Bulk Erase (BE) instruction completion
- The Reset ($\overline{\text{Reset}}$) signal can be driven Low to freeze and reset the internal logic. For the specific cases of Program and Write cycles, the designer should refer to *Section 6.5: Write Status Register (WRSR)*, *Section 6.9: Page Write (PW)*, *Section 6.10: Page Program (PP)*, *Section 6.12: Page Erase (PE)*, *Section 6.14: Sector Erase (SE)*, *Section 6.13: Subsector Erase (SSE)*, and to *Table 12: Device status after a Reset Low pulse*.
- In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection from inadvertent Write, Program and Erase instructions while the device is not in active use.

4.8.2 Specific hardware and software protections

The M25PE40 features a Hardware Protected mode, HPM, and two Software Protected modes, SPM1 and SPM2 that can be combined to protect the memory array as required. They are described below:

HPM

- **HPM in T7X process (see *Important note on page 6*):**

  The Hardware Protected mode (HPM) is entered when Top Sector Lock ($\overline{TSL}$) is driven Low, causing the top 256 pages of memory to become read-only. When Top Sector Lock ($\overline{TSL}$) is driven High, the top 256 pages of memory behave like the other pages of memory and the protection depends on the Block Protect bits (see SPM2 below).

- **HPM in T9HX process (see *Important note on page 6*):**

  The Hardware Protected mode (HPM) is used to write-protect the non-volatile bits of the Status Register (that is, the Block Protect bits, BP2, BP1 and BP0, and the Status Register Write Disable bit, SRWD).
  HPM is entered by driving the Write Protect ($\overline{W}$) signal Low with the SRWD bit set to High. This additional protection allows the Status Register to be hardware-protected (see also *Section 6.4.4: SRWD bit*).

SPM1 and SPM2

- **The first Software Protected mode (SPM1)** is managed by specific Lock Registers assigned to each 64-Kbyte sector.

  The Lock Registers can be read and written using the Read Lock Register (RDLR) and Write to Lock Register (WRLR) instructions.

  In each Lock Register two bits control the protection of each sector: the Write Lock bit and the Lock Down bit.

  – Write Lock bit:

    The Write Lock bit determines whether the contents of the sector can be modified (using the Write, Program or Erase instructions). When the Write Lock bit is set to ‘1’, the sector is write protected – any operations that attempt to change the data in the sector will fail. When the Write Lock bit is reset to ‘0’, the sector is not write protected by the Lock Register, and may be modified.

  – Lock Down bit:

    The Lock Down bit provides a mechanism for protecting software data from simple hacking and malicious attack. When the Lock Down bit is set to ‘1’, further modification to the Write Lock and Lock Down bits cannot be performed. A reset, or power-up, is required before changes to these bits can be made. When the Lock Down bit is reset to ‘0’, the Write Lock and Lock Down bits can be changed.

  The Write Lock bit and the Lock Down bit are volatile and their value is reset to ‘0’ after a power-down or a reset.

Table 2. Software protection truth table (Sectors 0 to 7, 64-Kbyte granularity)

Sector Lock Register		Protection status
Lock Down bit	Write Lock bit	
0	0	Sector unprotected from Program/Erase/Write operations, protection status reversible
0	1	Sector protected from Program/Erase/Write operations, protection status reversible
1	0	Sector unprotected from Program/Erase/Write operations, sector protection status cannot be changed except by a reset or power-up.
1	1	Sector protected from Program/Erase/Write operations, sector protection status cannot be changed except by a reset or power-up.

- **The second Software Protected mode (SPM2)** uses the Block Protect bits (BP2, BP1, BP0, see *Section 6.4.3*)) to allow part of the memory to be configured as read-only.

Table 3. Protected area sizes

Status Register content			Memory content	
BP2 bit	BP1 bit	BP0 bit	Protected area	Unprotected area
0	0	0	none	All sectors(1) (eight sectors: 0 to 7)
0	0	1	Upper eighth (sector 7)	Lower seven-eighths (seven sectors: 0 to 6)
0	1	0	Upper quarter (two sectors: 6 and 7)	Lower three-quarters (six sectors: 0 to 5)
0	1	1	Upper half (four sectors: 4 to 7)	Lower half (four sectors: 0 to 3)
1	0	0	All sectors (eight sectors: 0 to 7)	none
1	0	1	All sectors (eight sectors: 0 to 7)	none
1	1	0	All sectors (eight sectors: 0 to 7)	none
1	1	1	All sectors (eight sectors: 0 to 7)	none

1. The device is ready to accept a Bulk Erase instruction if, and only if, all Block Protect bits (BP2, BP1, BP0) are 0.

5 Memory organization

The memory is organized as:

- 2048 pages (256 bytes each)
- 524,288 bytes (8 bits each)
- 128 subsectors (32 Kbits, 4096 bytes each)
- 8 sectors (512 Kbits, 65536 bytes each)

Each page can be individually:

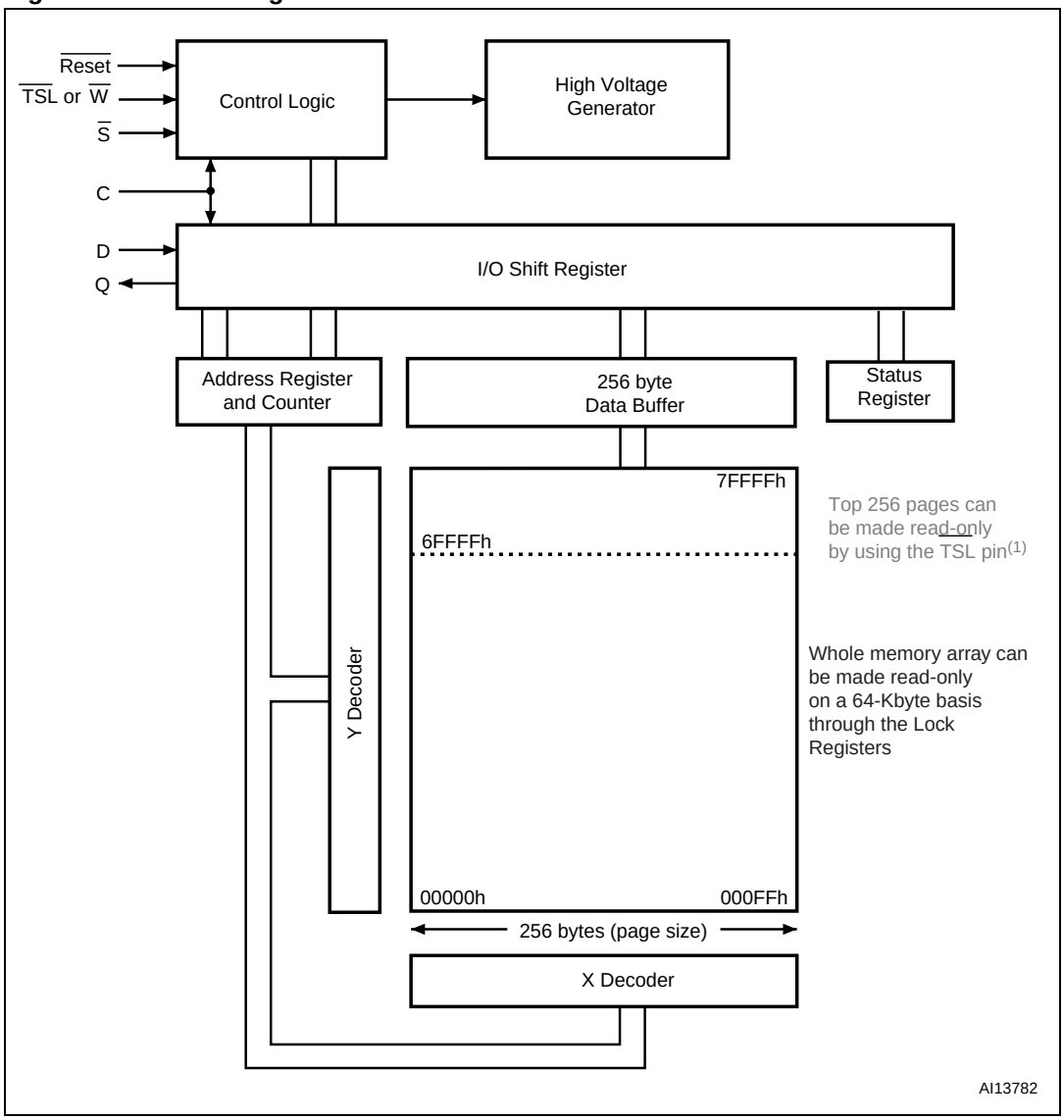
- programmed (bits are programmed from 1 to 0)
- erased (bits are erased from 0 to 1)
- written (bits are changed to either 0 or 1)

The device is page or sector erasable (bits are erased from 0 to 1).

Table 4. Memory organization

Sector	Subsector	Address range	
7	127	7F000h	7FFFFh
	⋮	⋮	⋮
	112	70000h	70FFFh
6	111	6F000h	6FFFFh
	⋮	⋮	⋮
	96	60000h	60FFFh
5	95	5F000h	5FFFFh
	⋮	⋮	⋮
	80	50000h	50FFFh
4	79	4F000h	4FFFFh
	⋮	⋮	⋮
	64	40000h	40FFFh
3	63	3F000h	3FFFFh
	⋮	⋮	⋮
	48	30000h	30FFFh
2	47	2F000h	2FFFFh
	⋮	⋮	⋮
	32	20000h	20FFFh
1	31	1F000h	1FFFFh
	⋮	⋮	⋮
	16	10000h	10FFFh
0	15	0F000h	0FFFFh
	⋮	⋮	⋮
	4	04000h	04FFFh
	3	03000h	03FFFh
	2	02000h	02FFFh
	1	01000h	01FFFh
	0	00000h	00FFFh

Figure 6. Block diagram



1. These features (in gray) are only available in the T7X process.

6 Instructions

All instructions, addresses and data are shifted in and out of the device, most significant bit first.

Serial Data input (D) is sampled on the first rising edge of Serial Clock (C) after Chip Select ($\overline{S}$) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data input (D), each bit being latched on the rising edges of Serial Clock (C).

The instruction set is listed in*Table 5*.

Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none.

In the case of a Read Data Bytes (READ), Read Data Bytes at Higher Speed (FAST_READ), Read Status Register (RDSR) or Read to Lock Register (RDLR) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select ($\overline{S}$) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a Page Write (PW), Page Program (PP), Page Erase (PE), Subsector Erase (SSE), Sector Erase (SE), Bulk Erase (BE), Write Enable (WREN), Write Disable (WRDI), Write Status Register (WRSR), Write to Lock Register (WRLR), Deep Power-down (DP) or Release from Deep Power-down (RDP) instruction, Chip Select ($\overline{S}$) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select ($\overline{S}$) must driven High when the number of clock pulses after Chip Select ($\overline{S}$) being driven Low is an exact multiple of eight.

All attempts to access the memory array during a Write cycle, Program cycle or Erase cycle are ignored, and the internal Write cycle, Program cycle or Erase cycle continues unaffected.

Table 5. Instruction set

Instruction	Description	One-byte instruction code		Addr bytes	Dummy bytes	Data bytes
WREN	Write Enable	0000 0110	06h	0	0	0
WRDI	Write Disable	0000 0100	04h	0	0	0
RDID	Read Identification	1001 1111	9Fh	0	0	1 to 3
RDSR(1)	Read Status Register	0000 0101	05h	0	0	1 to ∞
WRLR(1)	Write to Lock Register	1110 0101	E5h	3	0	1
WRSR(1)	Write Status Register	0000 0001	01h	0	0	1
RDLR	Read Lock Register	1110 1000	E8h	3	0	1
READ	Read Data Bytes	0000 0011	03h	3	0	1 to ∞
FAST_READ	Read Data Bytes at Higher Speed	0000 1011	0Bh	3	1	1 to ∞
PW	Page Write	0000 1010	0Ah	3	0	1 to 256
PP	Page Program	0000 0010	02h	3	0	1 to 256
PE	Page Erase	1101 1011	DBh	3	0	0
SSE(1)	Subsector Erase	0010 0000	20h	3	0	0
SE	Sector Erase	1101 1000	D8h	3	0	0
BE(1)	Bulk Erase	1100 0111	C7h	0	0	0
DP	Deep Power-down	1011 1001	B9h	0	0	0
RDP	Release from Deep Power-down	1010 1011	ABh	0	0	0

1. Instruction available only in the T9HX process (see *Important note on page 6*).

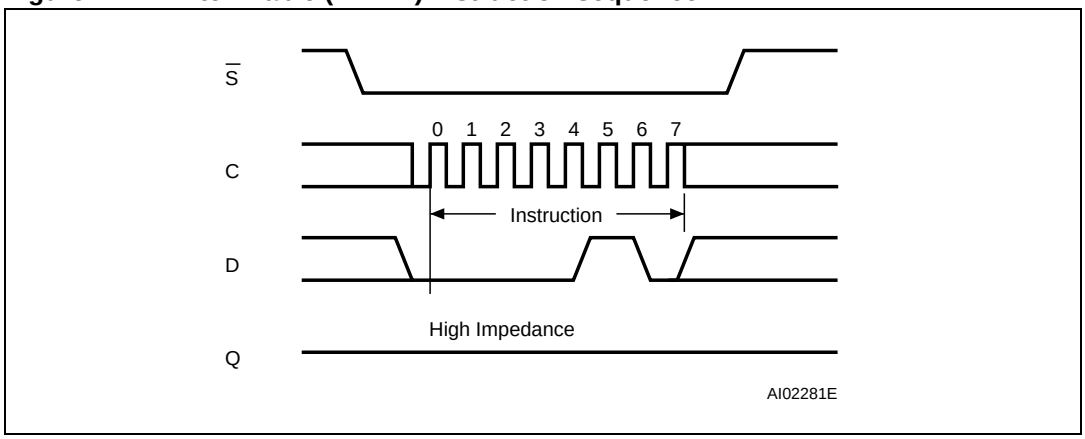
6.1 Write Enable (WREN)

The Write Enable (WREN) instruction (*Figure 7*) sets the Write Enable Latch (WEL) bit.

The Write Enable Latch (WEL) bit must be set prior to every Page Write (PW), Page Program (PP), Page Erase (PE), and Sector Erase (SE) instruction.

The Write Enable (WREN) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip Select ($\overline{S}$) High.

Figure 7. Write Enable (WREN) instruction sequence



6.2 Write Disable (WRDI)

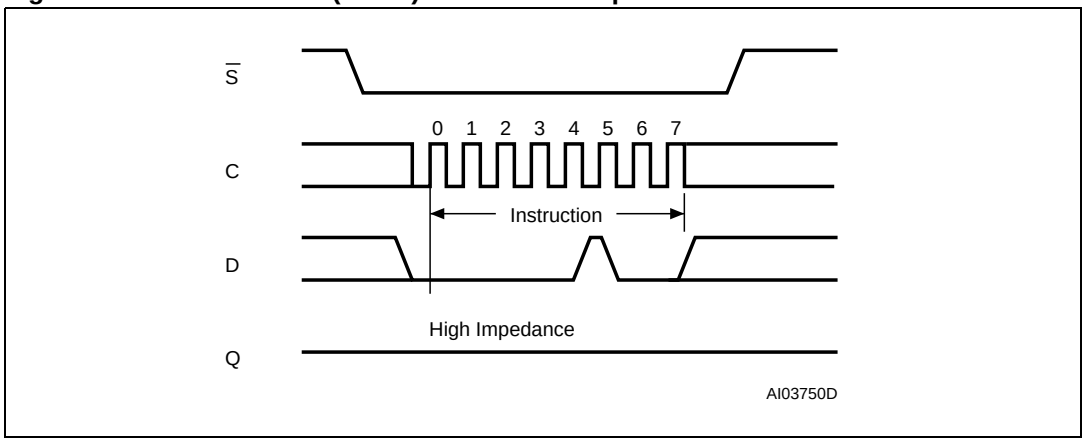
The Write Disable (WRDI) instruction (*Figure 8*) resets the Write Enable Latch (WEL) bit.

The Write Disable (WRDI) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip Select ($\overline{S}$) High.

The Write Enable Latch (WEL) bit is reset under the following conditions:

- Power-up
- Write Disable (WRDI) instruction completion
- Page Write (PW) instruction completion
- Page Program (PP) instruction completion
- Write Status Register (WRSR) instruction completion
- Write to Lock Register (WRLR) instruction completion
- Page Erase (PE) instruction completion
- Subsector Erase (SSE) instruction completion
- Sector Erase (SE) instruction completion
- Bulk Erase (BE) instruction completion

Figure 8. Write Disable (WRDI) instruction sequence



6.3 Read Identification (RDID)

The Read Identification (RDID) instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The manufacturer identification is assigned by JEDEC, and has the value 20h for Numonyx. The device identification is assigned by the device manufacturer, and indicates the memory type in the first byte (80h), and the memory capacity of the device in the second byte (13h).

Any Read Identification (RDID) instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

The device is first selected by driving Chip Select ($\overline{S}$) Low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data output (Q), each bit being shifted out during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 9*.

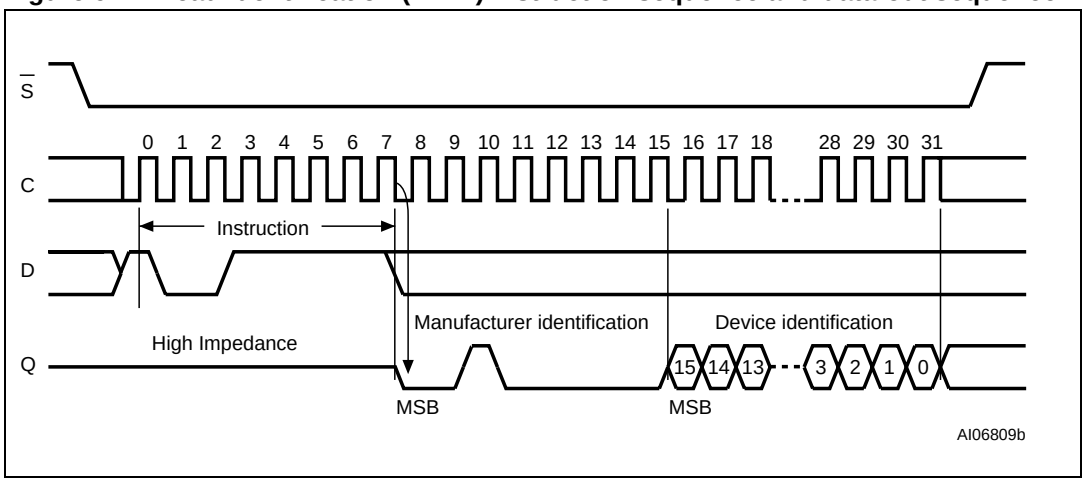
The Read Identification (RDID) instruction is terminated by driving Chip Select ($\overline{S}$) High at any time during data output.

When Chip Select ($\overline{S}$) is driven High, the device is put in the Standby Power mode. Once in the Standby Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Table 6. Read Identification (RDID) Data-out sequence

Manufacturer identification	Device identification	
	Memory type	Memory capacity
20h	80h	13h

Figure 9. Read Identification (RDID) instruction sequence and data-out sequence



6.4 Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in *Figure 10*.

The status bits of the Status Register are as follows:

6.4.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write, Program or Erase cycle. When set to ‘1’, such a cycle is in progress, when reset to ‘0’ no such cycle is in progress.

6.4.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to ‘1’ the internal Write Enable Latch is set, when set to ‘0’ the internal Write Enable Latch is reset and no Write, Program or Erase instruction is accepted.

6.4.3 BP2, BP1, BP0 bits

The Block Protect bits (BP2, BP1, BP0) are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or more of the Block Protect (BP2, BP1, BP0) bits is set to ‘1’, the relevant memory area (as defined in *Table 3*) becomes protected against Page Program (PP), Page Erase (PE), Sector Erase (SE) and Subsector Erase (SSE) instructions. The Block Protect (BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Bulk Erase (BE) instruction is executed if, and only if:

- all Block Protect (BP2, BP1, BP0) bits are 0
- the Lock Register protection bits are not all set (‘1’).

6.4.4 SRWD bit

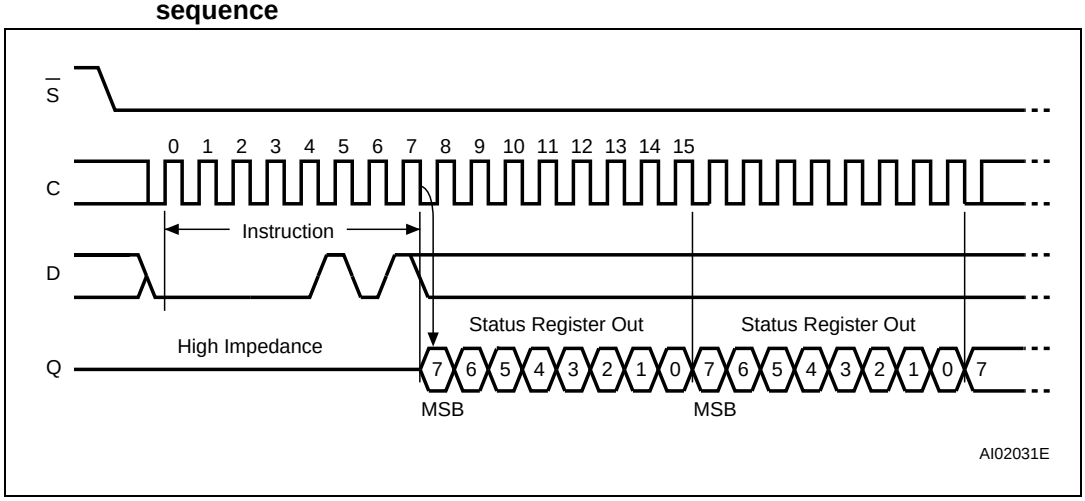
The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. When the Status Register Write Disable (SRWD) bit is set to ‘1’, and Write Protect ($\overline{W}$) is driven Low, the non-volatile bits of the Status Register (SRWD, BP2, BP1, BP0) become read-only bits. In such a state, as the Write Status Register (WRSR) instruction is no longer accepted for execution, the definition of the size of the Write Protected area **cannot** be further modified.

Table 7. Status Register format(1)(2)(3)

b7							b0
SRWD	0	0	BP2	BP1	BP0	WEL	WIP

1. WEL (Write Enable Latch) and WIP ((Write In Program) are volatile read-only bits (WEL is set and reset by specific instructions; WIP is automatically set and reset by the internal logic of the device).
2. SRWD = Status Register Write Protect bit; BP0, BP1, BP2 = Block Protect bits.
3. The BP bits and the SRWD bit exist only in the T9HX process.

Figure 10. Read Status Register (RDSR) instruction sequence and data-out sequence



6.5 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register.

Note: The Status Register BPi and SRWD bits are available in the M25PE40 in the T9HX process only. See Important note on page 6 for more details.

Before the Write Status Register (WRSR) instruction can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code and the data byte on Serial Data input (D).

The instruction sequence is shown in *Figure 11*.

The Write Status Register (WRSR) instruction has no effect on b6, b5, b1 and b0 of the Status Register. b6 and b5 are always read as 0.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in *Table 3*. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Write Disable (SRWD) bit in accordance with the Write Protect ($\overline{W}$) signal (see *Section 6.4.4*).

If a Write Status Register (WRSR) instruction is interrupted by a $\overline{Reset}$ Low pulse, the internal cycle of the Write Status Register operation (whose duration is t_W) is first completed (provided that the supply voltage V_{CC} remains within the operating range). After that the device enters the Reset mode (see also *Table 12: Device status after a Reset Low pulse* and *Table 24: Timings after a Reset Low pulse*).

Figure 11. Write Status Register (WRSR) instruction sequence

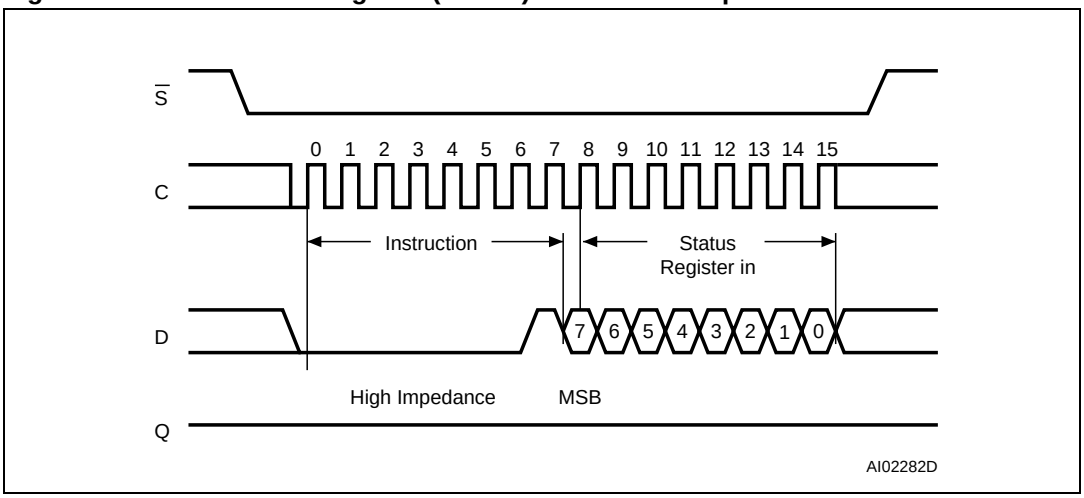


Table 8. Protection modes (T9HX process only, see *Important note on page 6*)

$\overline{W}$ signal	SRWD bit	Mode	Write protection of the Status Register	Memory content	
				Protected area(1)	Unprotected area(1)
1	0	Second software protected (SPM2)	Status Register is writable (if the WREN instruction has set the WEL bit) The values in the SRWD, BP2, BP1 and BP0 bits can be changed	Protected against Page Program, Sector Erase and Bulk Erase	Ready to accept Page Program and Sector Erase instructions
0	0				
1	1				
0	1	Hardware protected (HPM)	Status Register is hardware write protected The values in the SRWD, BP2, BP1 and BP0 bits cannot be changed	Protected against Page Program, Sector Erase and Bulk Erase	Ready to accept Page Program and Sector Erase instructions

1. As defined by the values in the Block Protect (BP2, BP1, BP0) bits of the Status Register, as shown in *Table 3*.

The protection features of the device are summarized in *Table 8*.

When the Status Register Write Disable (SRWD) bit of the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction, regardless of the whether Write Protect ($\overline{W}$) is driven High or Low.

When the Status Register Write Disable (SRWD) bit of the Status Register is set to '1', two cases need to be considered, depending on the state of Write Protect ($\overline{W}$):

- If Write Protect ($\overline{W}$) is driven High, it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction.
- If Write Protect ($\overline{W}$) is driven Low, it is *not* possible to write to the Status Register *even* if the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction (attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area that are software protected (SPM2) by the Block Protect (BP2, BP1, BP0) bits of the Status Register, are also hardware protected against data modification.

Regardless of the order of the two events, the Hardware Protected Mode (HPM) can be entered:

- by setting the Status Register Write Disable (SRWD) bit after driving Write Protect ($\overline{W}$) Low
- or by driving Write Protect ($\overline{W}$) Low after setting the Status Register Write Disable (SRWD) bit.

The only way to exit the Hardware Protected mode (HPM) once entered is to pull Write Protect ($\overline{W}$) High.

If Write Protect ($\overline{W}$) is permanently tied High, the Hardware Protected mode (HPM) can never be activated, and only the Software Protected mode (SPM2), using the Block Protect (BP2, BP1, BP0) bits of the Status Register, can be used.

6.6 Read Data Bytes (READ)

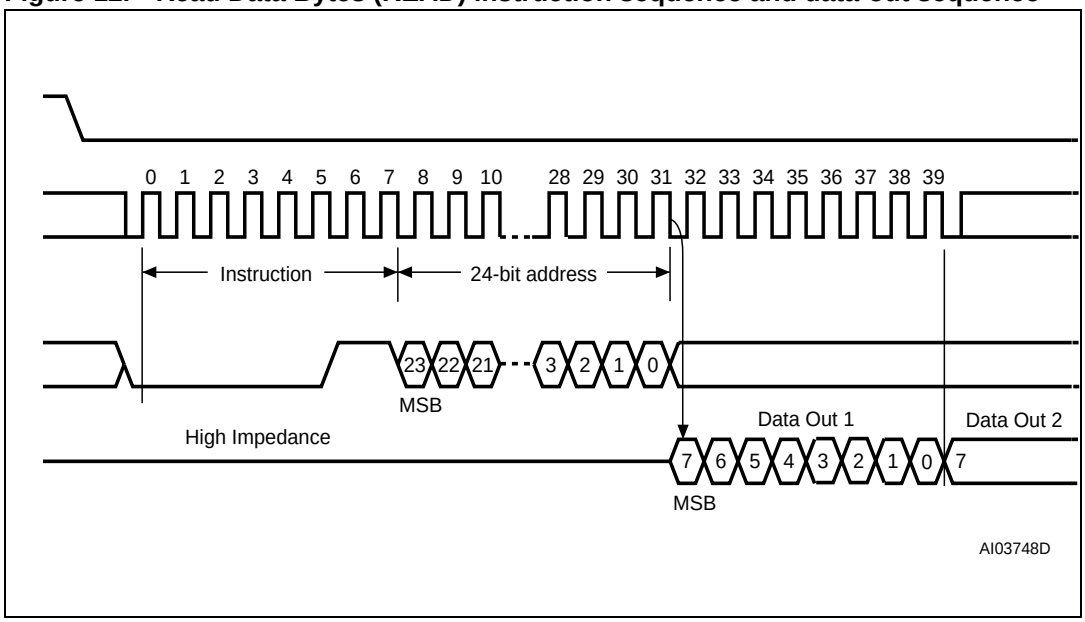
The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data output (Q), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 12*.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 12. Read Data Bytes (READ) instruction sequence and data-out sequence



1. Address bits A23 to A19 are Don't care.

6.7 Read Data Bytes at Higher Speed (FAST_READ)

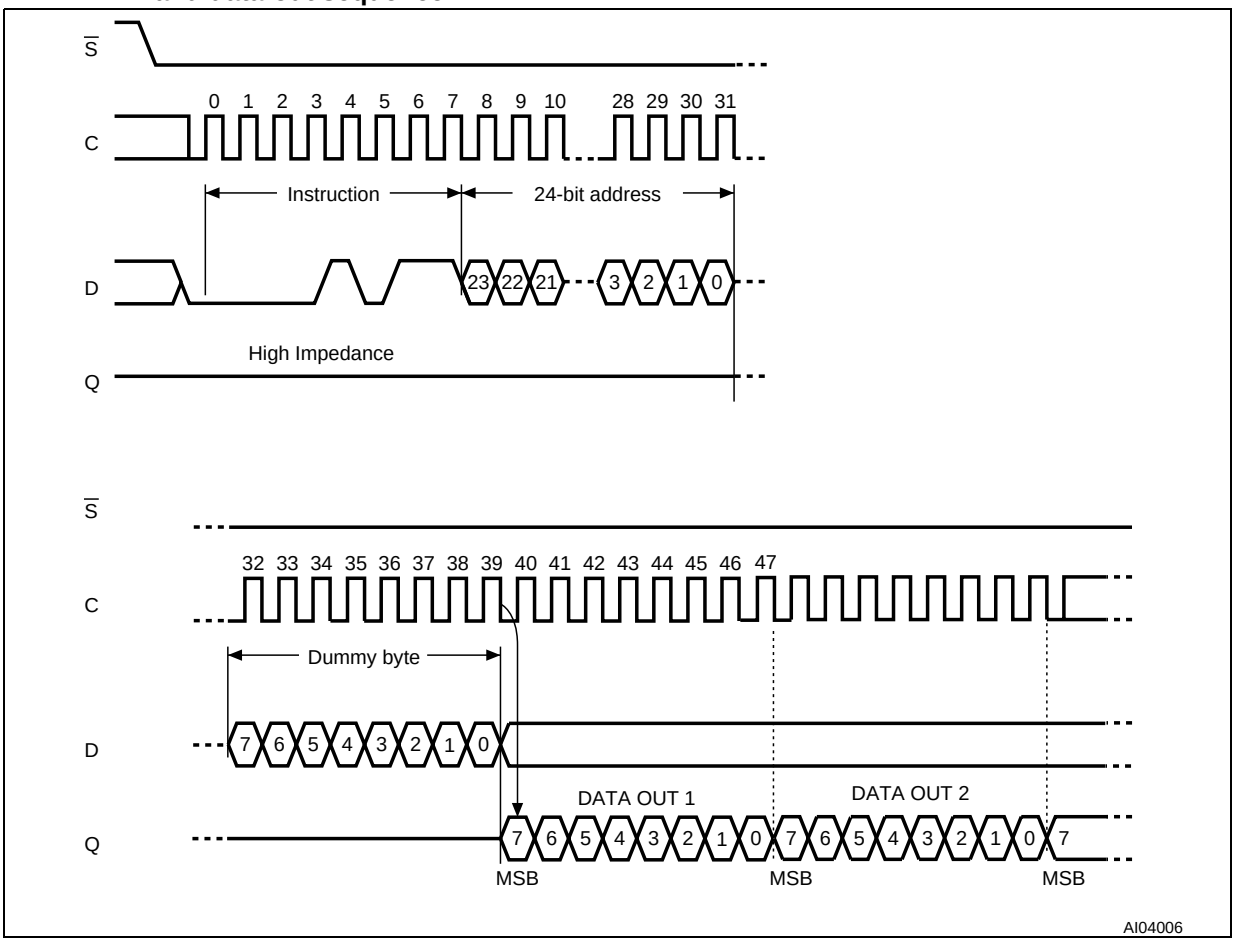
The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the Read Data Bytes at Higher Speed (FAST_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data output (Q), each bit being shifted out, at a maximum frequency f_C, during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 13*.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes at Higher Speed (FAST_READ) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any Read Data Bytes at Higher Speed (FAST_READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 13. Read Data Bytes at Higher Speed (FAST_READ) instruction sequence and data-out sequence



1. Address bits A23 to A19 are Don't care.

6.8 Read Lock Register (RDLR)

*Note: The Read Lock Register (RDLR) instruction is decoded only in the M25PE40 in the T9HX process (see **Important note on page 6**).*

The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the Read Lock Register (RDLR) instruction is followed by a 3-byte address (A23-A0) pointing to any location inside the concerned sector (or subsector). Each address bit is latched-in during the rising edge of Serial Clock (C). Then the value of the Lock Register is shifted out on Serial Data output (Q), each bit being shifted out, at a maximum frequency f_C, during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 14*.

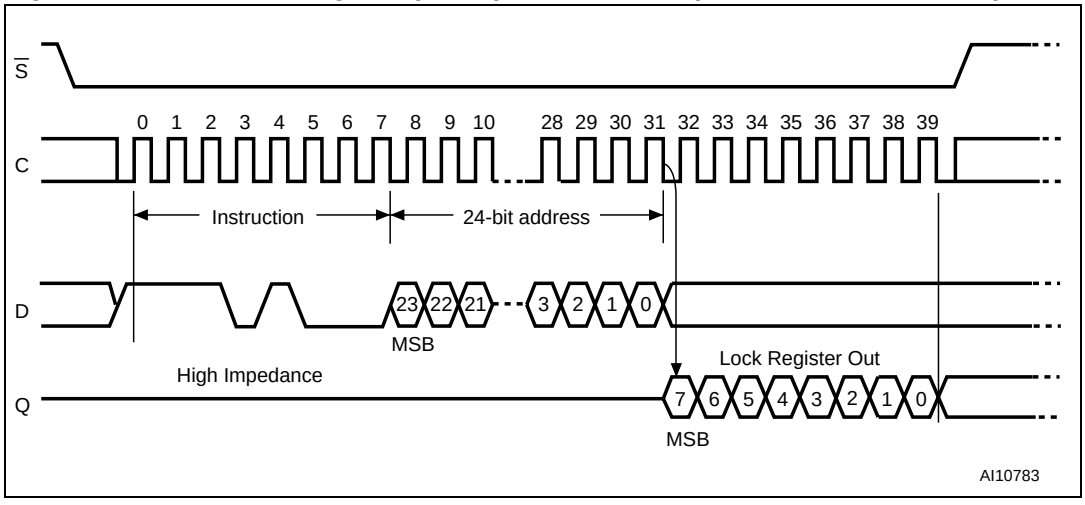
The Read Lock Register (RDLR) instruction is terminated by driving Chip Select ($\overline{S}$) High at any time during data output.

Any Read Lock Register (RDLR) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Table 9. Lock Registers

Bit	Bit name	Value	Function
b7-b4	Reserved		
b1	Sector Lock Down	‘1’	The Write Lock and Lock Down bits cannot be changed. Once a ‘1’ is written to the Lock Down bit it cannot be cleared to ‘0’, except by a reset or power-up.
		‘0’	The Write Lock and Lock Down bits can be changed by writing new values to them (default value).
b0	Sector Write Lock	‘1’	Write, Program and Erase operations in this sector will not be executed. The memory contents will not be changed.
		‘0’	Write, Program and Erase operations in this sector are executed and will modify the sector contents (default value).

Figure 14. Read Lock Register (RDLR) instruction sequence and data-out sequence



6.9 Page Write (PW)

The Page Write (PW) instruction allows bytes to be written in the memory. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Write (PW) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data input (D). The rest of the page remains unchanged if no power failure occurs during this write cycle.

The Page Write (PW) instruction performs a page erase cycle even if only one byte is updated.

If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data exceeding the addressed page boundary roll over, and are written from the start address of the same page (the one whose 8 least significant address bits (A7-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 15*.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be written correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly written at the requested addresses without having any effects on the other bytes of the same page.

For optimized timings, it is recommended to use the Page Write (PW) instruction to write all consecutive targeted bytes in a single sequence versus using several Page Write (PW) sequences with each containing only a few bytes (see *Table 21: AC characteristics (50 MHz operation, T9HX (0.11µm) process)* and *Table 22: AC characteristics (75 MHz operation, T9HX (0.11µm) process)*).

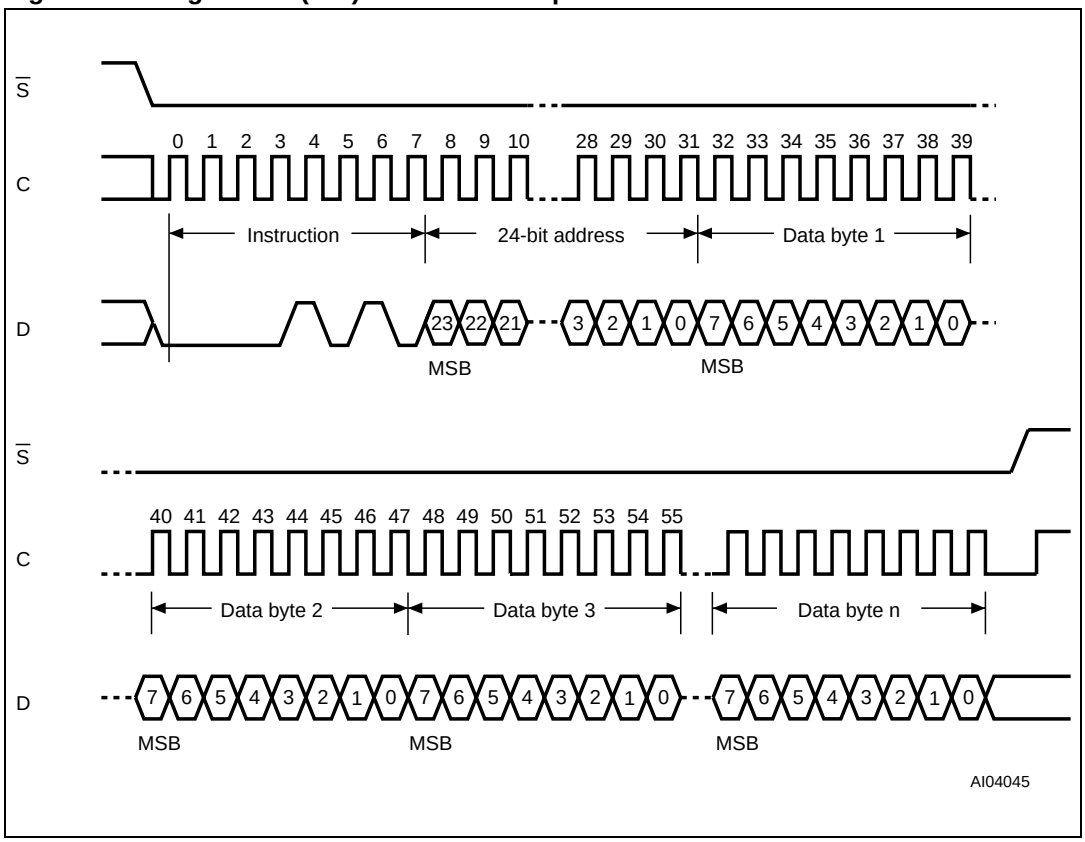
Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Write (PW) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Page Write cycle (whose duration is t_{PW}) is initiated. While the Page Write cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Write cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the Write Enable Latch (WEL) bit is reset.

A Page Write (PW) instruction applied to a page that is hardware protected is not executed.

Any Page Write (PW) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 15. Page Write (PW) instruction sequence



1. Address bits A23 to A19 are Don't care.
2. $1 \leq n \leq 256$.

6.10 Page Program (PP)

The Page Program (PP) instruction allows bytes to be programmed in the memory (changing bits from 1 to 0, only). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Program (PP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data input (D). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data exceeding the addressed page boundary roll over, and are programmed from the start address of the same page (the one whose 8 least significant address bits (A7-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 16*.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

For optimized timings, it is recommended to use the Page Program (PP) instruction to program all consecutive targeted bytes in a single sequence versus using several Page Program (PP) sequences with each containing only a few bytes (see *Table 20: AC characteristics (33 MHz operation)*).

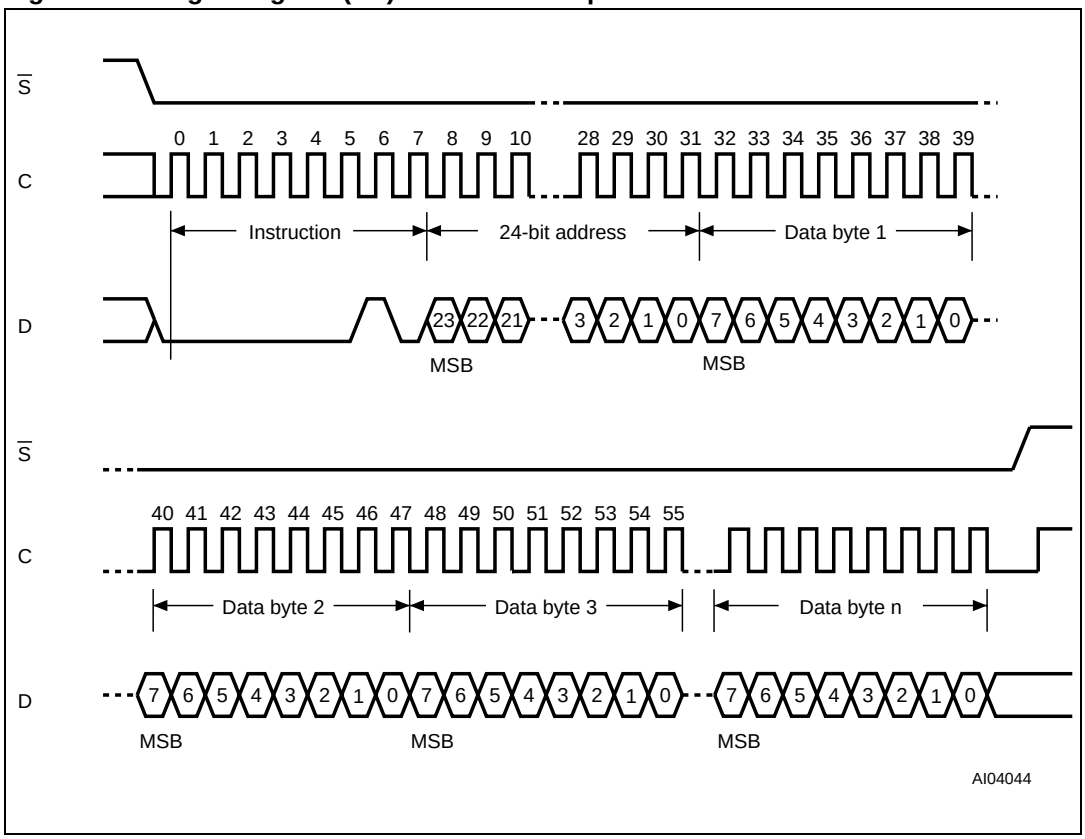
Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page that is hardware protected is not executed.

Any Page Program (PP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 16. Page Program (PP) instruction sequence



1. Address bits A23 to A19 are Don't care.
2. $1 \leq n \leq 256$.

6.11 Write to Lock Register (WRLR)

*Note: The Write to Lock Register (WRLR) instruction is decoded only in the M25PE40 in the T9HX process (see **Important note on page 6**).*

The Write to Lock Register (WRLR) instruction allows bits to be changed in the Lock Registers. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Write to Lock Register (WRLR) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes (pointing to any address in the targeted sector and one data byte on Serial Data input (D). The instruction sequence is shown in *Figure 17*. Chip Select ($\overline{S}$) must be driven High after the eighth bit of the data byte has been latched in, otherwise the Write to Lock Register (WRLR) instruction is not executed.

Lock Register bits are volatile, and therefore do not require time to be written. When the Write to Lock Register (WRLR) instruction has been successfully executed, the Write Enable Latch (WEL) bit is reset after a delay time less than t_{SHSL} minimum value.

Any Write to Lock Register (WRLR) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 17. Write to Lock Register (WRLR) instruction sequence

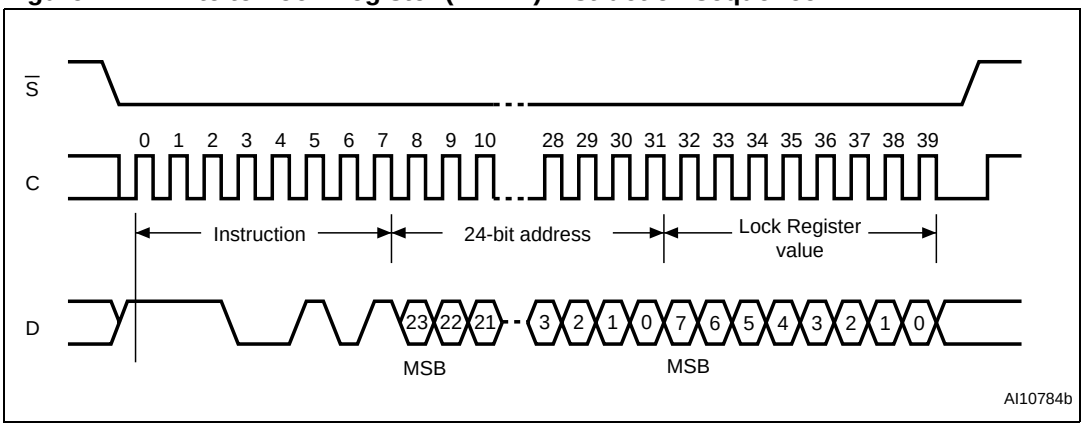


Table 10. Lock Register in(1)

Sector	Bit	Value
All sectors	b7-b2	'0'
	b1	Sector Lock Down bit value
	b0	Sector Write Lock bit value

1. The table rows in gray are true for products processed in the T7X process only (see *Important note on page 6*).

6.12 Page Erase (PE)

The Page Erase (PE) instruction sets to ‘1’ (FFh) all bits inside the chosen page. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Erase (PE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, and three address bytes on Serial Data input (D). Any address inside the page is a valid address for the Page Erase (PE) instruction. Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

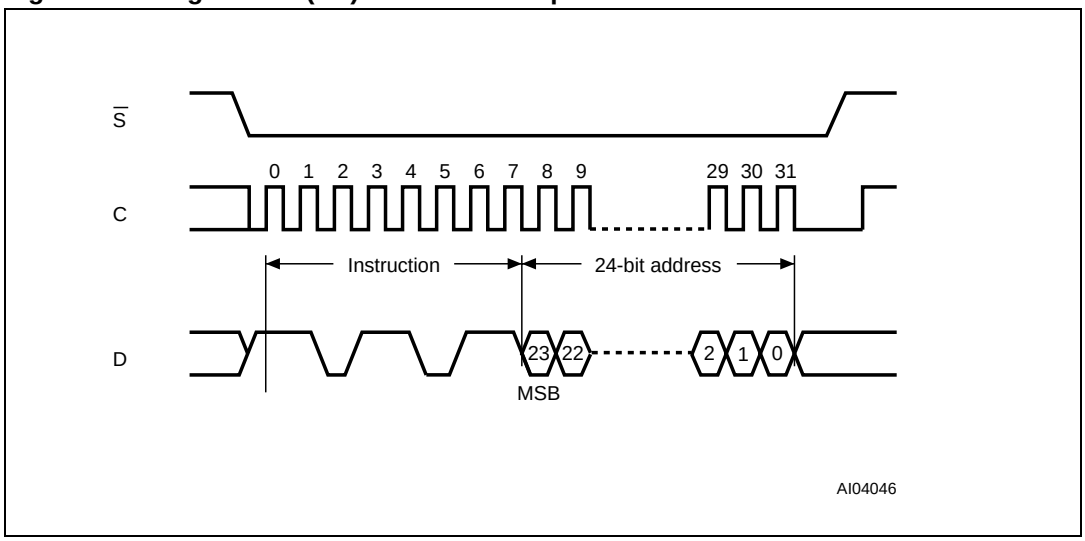
The instruction sequence is shown in *Figure 18*.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Page Erase (PE) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Page Erase cycle (whose duration is t_{PE}) is initiated. While the Page Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the Write Enable Latch (WEL) bit is reset.

A Page Erase (PE) instruction applied to a page that is hardware protected is not executed.

Any Page Erase (PE) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 18. Page Erase (PE) instruction sequence



1. Address bits A23 to A19 are Don’t care.

6.13 Subsector Erase (SSE)

*Note: The Subsector Erase (SSE) instruction is decoded only in the M25PE40 in the T9HX process (see **Important note on page 6**).*

The Subsector Erase (SSE) instruction sets to '1' (FFh) all bits inside the chosen subsector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Subsector Erase (SE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, and three address bytes on Serial Data input (D). Any address inside the Subsector (see *Table 4*) is a valid address for the Subsector Erase (SE) instruction. Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 20*.

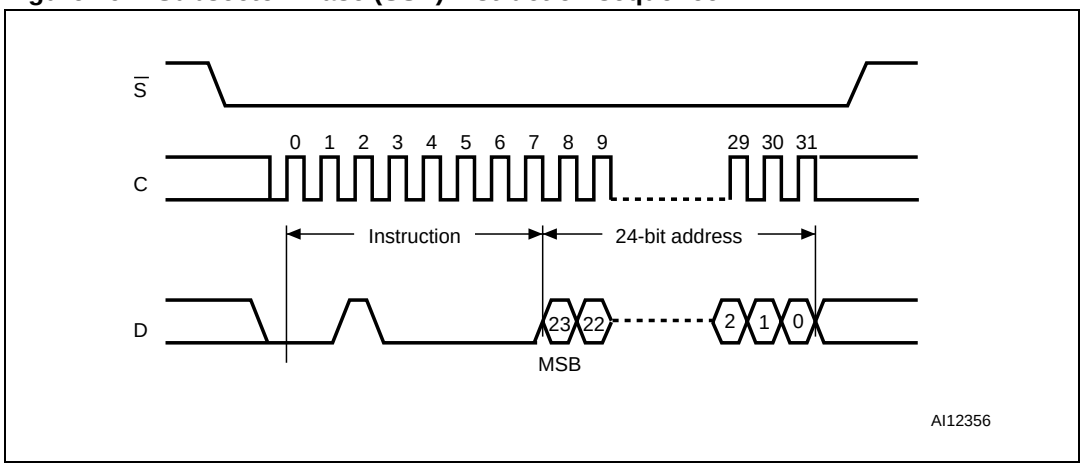
Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Subsector Erase (SE) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Subsector Erase cycle (whose duration is t_{SSE}) is initiated. While the Subsector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Subsector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the Write Enable Latch (WEL) bit is reset.

A Subsector Erase (SSE) instruction applied to a subsector that contains a page that is hardware or software protected is not executed.

Any Subsector Erase (SSE) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

If Reset ($\overline{Reset}$) is driven Low while a Subsector Erase (SSE) cycle is in progress, the Subsector Erase cycle is interrupted and data may not be erased correctly (see *Table 12: Device status after a Reset Low pulse*). On $\overline{Reset}$ going Low, the device enters the Reset mode and a time of t_{RHSL} is then required before the device can be re-selected by driving Chip Select ($\overline{S}$) Low. For the value of t_{RHSL} see *Table 24: Timings after a Reset Low pulse* in *Section 11: DC and AC parameters*.

Figure 19. Subsector Erase (SSE) instruction sequence



1. Address bits A23 to A19 are Don't care.

6.14 Sector Erase (SE)

The Sector Erase (SE) instruction sets to ‘1’ (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Sector Erase (SE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, and three address bytes on Serial Data Input (D). Any address inside the Sector (see *Table 4*) is a valid address for the Sector Erase (SE) instruction. Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

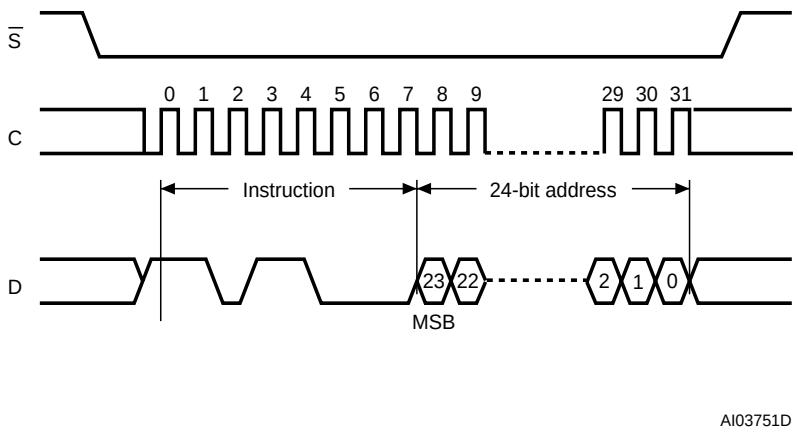
The instruction sequence is shown in *Figure 20*.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is complete, the Write Enable Latch (WEL) bit is reset.

A Sector Erase (SE) instruction applied to a sector that contains a page that is hardware protected is not executed.

Any Sector Erase (SE) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 20. Sector Erase (SE) instruction sequence



1. Address bits A23 to A19 are Don’t care.

6.15 Bulk Erase (BE)

Note: The Bulk Erase (BE) instruction is decoded only in the M25PE40 in the T9HX process (see Important note on page 6).

The Bulk Erase (BE) instruction sets all bits to '1' (FFh). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Bulk Erase (BE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data input (D). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

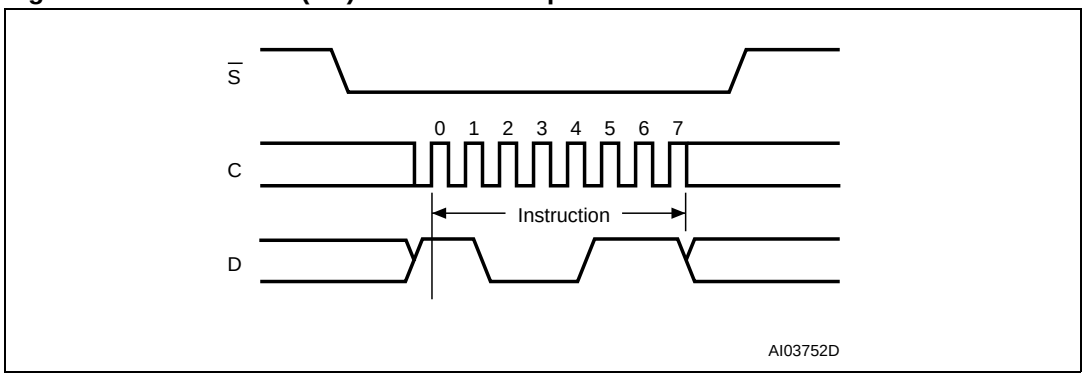
The instruction sequence is shown in *Figure 21*.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Bulk Erase instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Bulk Erase cycle (whose duration is t_{BE}) is initiated. While the Bulk Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Bulk Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

Any Bulk Erase (BE) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress. A Bulk Erase (BE) instruction is ignored if at least one sector or subsector is write-protected (hardware or software protection).

If Reset ($\overline{Reset}$) is driven Low while a Bulk Erase (BE) cycle is in progress, the Bulk Erase cycle is interrupted and data may not be erased correctly (see *Table 12: Device status after a Reset Low pulse*). On $\overline{Reset}$ going Low, the device enters the Reset mode and a time of t_{RHSL} is then required before the device can be re-selected by driving Chip Select ($\overline{S}$) Low. For the value of t_{RHSL} see *Table 24: Timings after a Reset Low pulse* in *Section 11: DC and AC parameters*.

Figure 21. Bulk Erase (BE) instruction sequence



6.16 Deep Power-down (DP)

Executing the Deep Power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the Deep Power-down mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase instructions.

Driving Chip Select ($\overline{S}$) High deselects the device, and puts the device in the Standby Power mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-down mode. The Deep Power-down mode can only be entered by executing the Deep Power-down (DP) instruction, subsequently reducing the standby current (from I_{CC1} to I_{CC2}, as specified in *Table 17*).

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down (RDP) instruction. This releases the device from this mode.

The Deep Power-down mode automatically stops at power-down, and the device always powers-up in the Standby Power mode.

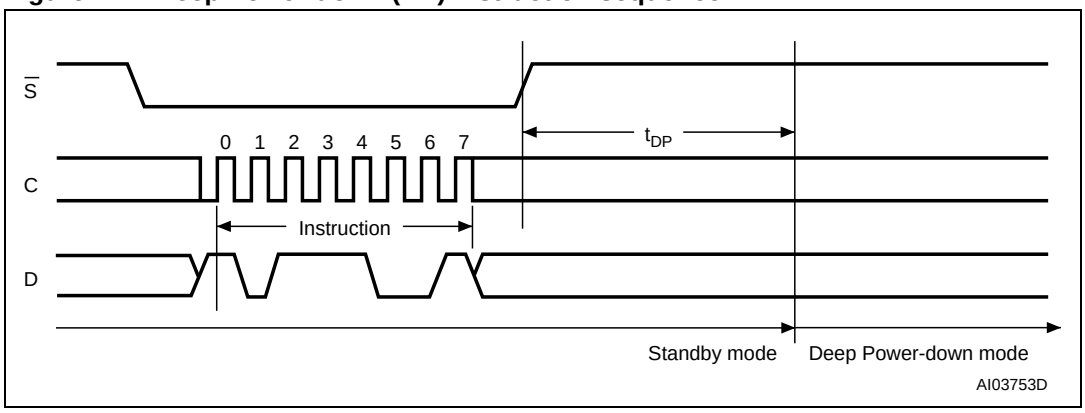
The Deep Power-down (DP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data input (D). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 22*.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Deep Power-down (DP) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-down mode is entered.

Any Deep Power-down (DP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 22. Deep Power-down (DP) instruction sequence



6.17 Release from Deep Power-down (RDP)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down (RDP) instruction. Executing this instruction takes the device out of the Deep Power-down mode.

The Release from Deep Power-down (RDP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data input (D). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

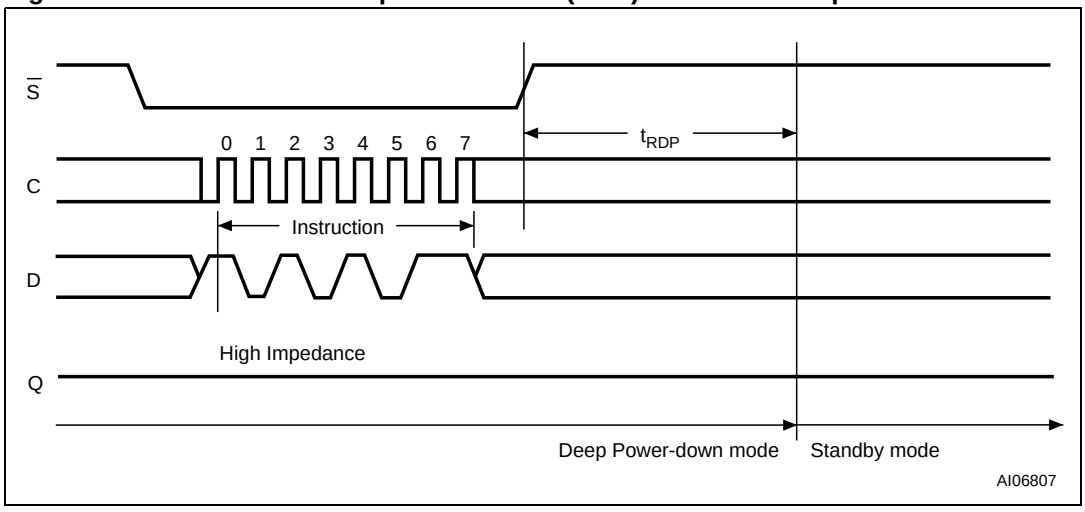
The instruction sequence is shown in *Figure 23*.

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select ($\overline{S}$) High. Sending additional clock cycles on Serial Clock (C), while Chip Select ($\overline{S}$) is driven Low, cause the instruction to be rejected, and not executed.

After Chip Select ($\overline{S}$) has been driven High, followed by a delay, t_{RDP}, the device is put in the Standby Power mode. Chip Select ($\overline{S}$) must remain High at least until this period is over. The device waits to be selected, so that it can receive, decode and execute instructions.

Any Release from Deep Power-down (RDP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 23. Release from Deep Power-down (RDP) instruction sequence



7 Power-up and power-down

At power-up and power-down, the device must not be selected (that is Chip Select ($\overline{S}$) must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value:

- V_{CC}(min) at power-up, and then for a further delay of t_{VSL}
- V_{SS} at power-down.

A safe configuration is provided in *Section 3: SPI modes*.

To avoid data corruption and inadvertent write operations during power-up, a Power On Reset (POR) circuit is included. The logic inside the device is held reset while V_{CC} is less than the Power On Reset (POR) threshold voltage, V_{WI} – all operations are disabled, and the device does not respond to any instruction.

Moreover, the device ignores all Write Enable (WREN), Page Write (PW), Page Program (PP), Page Erase (PE) and Sector Erase (SE) instructions until a time delay of t_{PUW} has elapsed after the moment that V_{CC} rises above the V_{WI} threshold. However, the correct operation of the device is not guaranteed if, by this time, V_{CC} is still below V_{CC}(min). No Write, Program or Erase instructions should be sent until the later of:

- t_{PUW} after V_{CC} passed the V_{WI} threshold
- t_{VSL} after V_{CC} passed the V_{CC}(min) level.

These values are specified in *Table 11*.

If the delay, t_{VSL}, has elapsed, after V_{CC} has risen above V_{CC}(min), the device can be selected for READ instructions even if the t_{PUW} delay is not yet fully elapsed.

As an extra protection, the Reset ($\overline{Reset}$) signal could be driven Low for the whole duration of the power-up and power-down phases.

At power-up, the device is in the following state:

- The device is in the Standby Power mode (not the Deep Power-down mode)
- The Write Enable Latch (WEL) bit is reset
- The Write In Progress (WIP) bit is reset
- The Lock Registers are reset (Write Lock bit, Lock Down bit) = (0, 0).

Normal precautions must be taken for supply rail decoupling, to stabilize the V_{CC} supply. Each device in a system should have the V_{CC} rail decoupled by a suitable capacitor close to the package pins. (Generally, this capacitor is of the order of 100 nF).

At power-down, when V_{CC} drops from the operating voltage, to below the Power On Reset (POR) threshold voltage, V_{WI}, all operations are disabled and the device does not respond to any instruction. (The designer needs to be aware that if a Power-down occurs while a Write, Program or Erase cycle is in progress, some data corruption can result.)

Figure 24. Power-up timing

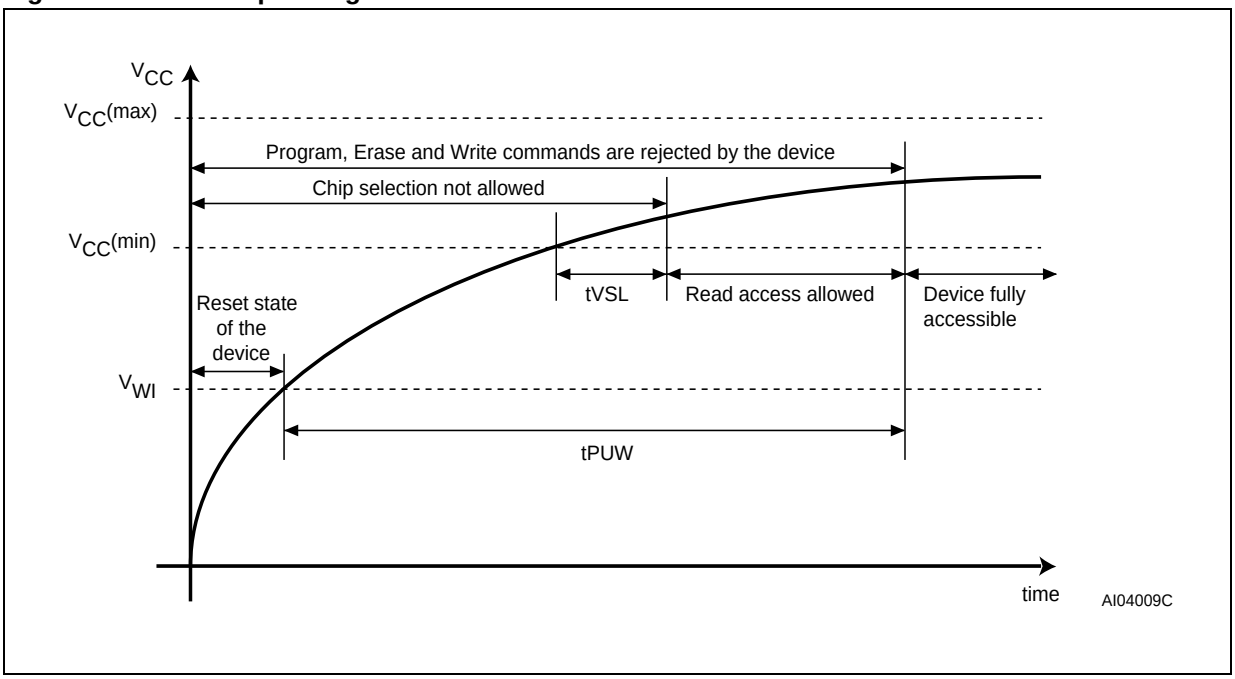


Table 11. Power-up timing and V_{WI} threshold

Symbol	Parameter	Min.	Max.	Unit
t_{VSL} (1)	V_{CC}(min) to $\overline{S}$ low	30		µs
t_{PUW} (1)	Time delay before the first Write, Program or Erase instruction	1	10	ms
V_{WI} (1)	Write Inhibit voltage	1.5	2.5	V

1. These parameters are characterized only, over the temperature range –40 °C to +85 °C.

8 Reset

Driving Reset ($\overline{\text{Reset}}$) Low while an internal operation is in progress will affect this operation (write, program or erase cycle) and data may be lost.

All the Lock bits are reset to ‘0’ after a $\overline{\text{Reset}}$ Low pulse.

Table 12 shows the status of the device after a $\overline{\text{Reset}}$ Low pulse.

Table 12. Device status after a $\overline{\text{Reset}}$ Low pulse

Conditions: Reset pulse occurred	Lock bits status	Internal logic status	Addressed data
While decoding an instruction(1): WREN, WRDI, RDID, RDSR, READ, RDLR, Fast_Read, WRLR, PW, PP, PE, SE, BE, SSE, DP, RDP	Reset to ‘0’	Same as POR	Not significant
Under completion of an Erase or Program cycle of a PW, PP, PE, SSE, SE, BE operation	Reset to ‘0’	Equivalent to POR	Addressed data could be modified
Under completion of a WRSR operation	Reset to ‘0’	Equivalent to POR (after t_W)	Write is correctly completed
Device deselected ($\overline{\text{S}}$ High) and in Standby mode	Reset to ‘0’	Same as POR	Not significant

1. $\overline{\text{S}}$ remains Low while $\overline{\text{Reset}}$ is Low.

9 Initial delivery state

The device is delivered with the memory array erased: all bits are set to ‘1’ (each byte contains FFh). All usable Status Register bits are 0.

10 Maximum rating

Stressing the device above the rating listed in *Table 13: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the Numonyx SURE Program and other relevant quality documents.

Table 13. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	See note (1)		°C
V_{IO}	Input and output voltage (with respect to ground)	–0.6	V_{CC} + 0.6	V
V_{CC}	Supply voltage	–0.6	4.0	V
V_{ESD}	Electrostatic discharge voltage (human body model)(2)	–2000	2000	V

1. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the Numonyx ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. JEDEC Std JESD22-A114A (C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω).

11 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 14. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.7	3.6	V
T_A	Ambient operating temperature	–40	85	°C

Table 15. Measurement conditions(1)

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	30		pF
	Input rise and fall times		5	ns
	Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and output timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V

1. Output Hi-Z is defined as the point where data out is no longer driven.

Figure 25. AC measurement I/O waveform

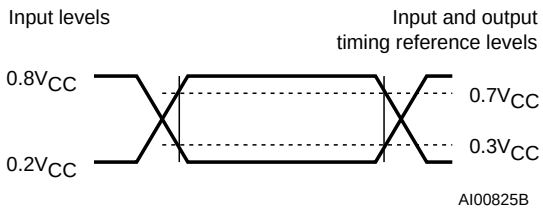


Table 16. Capacitance(1)

Symbol	Parameter	Test condition	Min.	Max.	Unit
C_{OUT}	Output capacitance (Q)	V_{OUT} = 0 V		8	pF
C_{IN}	Input capacitance (other pins)	V_{IN} = 0 V		6	pF

1. Sampled only, not 100% tested, at T_A = 25 °C and a frequency of 25 MHz.

Table 17. DC characteristics

Symbol	Parameter	Test condition (in addition to those in *Table 14*)	Min.	Max.	Unit
I_{LI}	Input Leakage current			± 2	µA
I_{LO}	Output Leakage current			± 2	µA
I_{CC1}	Standby current (Standby and Reset modes)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		50	µA
I_{CC2}	Deep Power-down current	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		10	µA
I_{CC3}	Operating current (FAST_READ)	C = 0.1V_{CC}/0.9.V_{CC} at 25 MHz, Q = open		6	mA
		C = 0.1V_{CC}/0.9.V_{CC} at 50 MHz, Q = open		8	mA
I_{CC4}	Operating current (PW)	$\overline{S}$ = V_{CC}		15	mA
I_{CC5}	Operating current (SE)	$\overline{S}$ = V_{CC}		15	mA
V_{IL}	Input Low voltage		– 0.5	0.3V_{CC}	V
V_{IH}	Input High voltage		0.7V_{CC}	V_{CC}+0.4	V
V_{OL}	Output Low voltage	I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output High voltage	I_{OH} = –100 µA	V_{CC}–0.2		V

Table 18. DC characteristics (75 MHz operation, T9HX (0.11 µm) process)(1)

Symbol	Parameter	Test condition (in addition to those in *Table 14*)	Min.	Max.	Unit
I_{LI}	Input Leakage current			± 2	µA
I_{LO}	Output Leakage current			± 2	µA
I_{CC1}	Standby current (Standby and Reset modes)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		50	µA
I_{CC2}	Deep Power-down current	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		10	µA
I_{CC3}	Operating current (FAST_READ)	C = 0.1V_{CC}/0.9.V_{CC} at 33 MHz, Q = open		4	mA
		C = 0.1V_{CC}/0.9.V_{CC} at 75 MHz, Q = open		12	mA
I_{CC4}	Operating current (PW)	$\overline{S}$ = V_{CC}		15	mA
I_{CC5}	Operating current (SE)	$\overline{S}$ = V_{CC}		15	mA
V_{IL}	Input Low voltage		– 0.5	0.3V_{CC}	V
V_{IH}	Input High voltage		0.7V_{CC}	V_{CC}+0.4	V
V_{OL}	Output Low voltage	I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output High voltage	I_{OH} = –100 µA	V_{CC}–0.2		V

1. Delivery of parts operating with a maximum clock rate of 75 MHz starts from week 8 of 2008.

Table 19. AC characteristics (25 MHz operation)

Test conditions specified in *Table 14* and *Table 15*						
Symbol	**Alt.**	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
f_C	f_C	Clock frequency for the following instructions: FAST_READ, PW, PP, PE, SE, DP, RDP, WREN, WRDI, RDSR	D.C.		25	MHz
f_R		Clock frequency for READ instructions	D.C.		20	MHz
t_{CH} (1)	t_{CLH}	Clock High time	18			ns
t_{CL} (1)	t_{CLL}	Clock Low time	18			ns
		Clock Slew rate (peak-to-peak)	0.1			V/ns
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup time (relative to C)	10			ns
t_{CHSL}		$\overline{S}$ Not Active Hold time (relative to C)	10			ns
t_{DVCH}	t_{DSU}	Data In Setup time	5			ns
t_{CHDX}	t_{DH}	Data In Hold time	5			ns
t_{CHSH}		$\overline{S}$ Active Hold time (relative to C)	10			ns
t_{SHCH}		$\overline{S}$ Not Active Setup time (relative to C)	10			ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect time	100			ns
t_{SHQZ} (2)	t_{DIS}	Output Disable time			15	ns
t_{CLQV}	t_V	Clock Low to Output Valid			15	ns
t_{CLQX}	t_{HO}	Output Hold time	0			ns
t_{THSL}		Top Sector Lock Setup time	50			ns
t_{SHTL}		Top Sector Lock Hold time	100			ns
t_{DP} (2)		$\overline{S}$ to Deep Power-down			3	µs
t_{RDP} (2)		$\overline{S}$ High to Standby Power mode			30	µs
t_{PW} (3)		Page Write cycle time (256 bytes)		11	25	ms
		Page Write cycle time (n bytes)		10.2+ n*0.8/256		
t_{PP} (3)		Page Program cycle time (256 bytes)		1.2	5	ms
		Page Program cycle time (n bytes)		0.4+ n*0.8/256		
t_{PE}		Page Erase cycle time		10	20	ms
t_{SE}		Sector Erase cycle time		1	5	s

1. $t_{CH} + t_{CL}$ must be greater than or equal to $1/ f_C$.
2. Value guaranteed by characterization, not 100% tested in production.
3. When using PP and PW instructions to update consecutive bytes, optimized timings are obtained with one sequence including all the bytes versus several sequences of only a few bytes ($1 \le n \le 256$).

Table 20. AC characteristics (33 MHz operation)

33 MHz only available for products marked since week 40 of 2005(1) Test conditions specified in *Table 14* and *Table 15*						
Symbol	**Alt.**	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
f_C	f_C	Clock frequency for the following instructions: FAST_READ, PW, PP, PE, SE, DP, RDP, WREN, WRDI, RDSR	D.C.		33	MHz
f_R		Clock frequency for READ instructions	D.C.		20	MHz
t_{CH} (2)	t_{CLH}	Clock High time	13			ns
t_{CL} (2)	t_{CLL}	Clock Low time	13			ns
		Clock Slew Rate (peak to peak)	0.1			V/ns
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup time (relative to C)	10			ns
t_{CHSL}		$\overline{S}$ Not Active Hold time (relative to C)	10			ns
t_{DVCH}	t_{DSU}	Data In Setup time	3			ns
t_{CHDX}	t_{DH}	Data In Hold time	5			ns
t_{CHSH}		$\overline{S}$ Active Hold time (relative to C)	5			ns
t_{SHCH}		$\overline{S}$ Not Active Setup time (relative to C)	5			ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect time	100			ns
t_{SHQZ} (3)	t_{DIS}	Output Disable time			12	ns
t_{CLQV}	t_V	Clock Low to Output Valid			12	ns
t_{CLQX}	t_{HO}	Output Hold time	0			ns
t_{THSL}		Top Sector Lock Setup time	50			ns
t_{SHTL}		Top Sector Lock Hold time	100			ns
t_{DP} (3)		$\overline{S}$ to Deep Power-down			3	µs
t_{RDP} (3)		$\overline{S}$ High to Standby Power mode			30	µs
t_{PW} (4)		Page Write cycle time (256 bytes)		11	25	ms
		Page Write cycle time (n bytes)		10.2+ n*0.8/256		
t_{PP} (4)		Page Program cycle time (256 bytes)		1.2	5	ms
		Page Program cycle time (n bytes)		0.4+ n*0.8/256		
t_{PE}		Page Erase cycle time		10	20	ms
t_{SE}		Sector Erase cycle time		1	5	s

1. Details of how to find the date of marking are given in application note, AN1995.
2. $t_{CH} + t_{CL}$ must be greater than or equal to $1/ f_C$.
3. Value guaranteed by characterization, not 100% tested in production.
4. When using PP and PW instructions to update consecutive bytes, optimized timings are obtained with one sequence including all the bytes versus several sequences of only a few bytes ($1 \le n \le 256$).

Table 21. AC characteristics (50 MHz operation, T9HX (0.11µm) process(1))(2)

Test conditions specified in *Table 14* and *Table 15*						
Symbol	**Alt.**	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
f_C	f_C	Clock frequency for the following instructions: FAST_READ, RDLR, PW, PP, WRLR, PE, SE, SSE, DP, RDP, WREN, WRDI, RDSR, WRSR	D.C.		50	MHz
f_R		Clock frequency for READ instructions	D.C.		33	MHz
t_{CH}(3)	t_{CLH}	Clock High time	9			ns
t_{CL}(3)	t_{CLL}	Clock Low time	9			ns
		Clock Slew Rate (peak to peak)	0.1			V/ns
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup time (relative to C)	5			ns
t_{CHSL}		$\overline{S}$ Not Active Hold time (relative to C)	5			ns
t_{DVCH}	t_{DSU}	Data In Setup time	2			ns
t_{CHDX}	t_{DH}	Data In Hold time	5			ns
t_{CHSH}		$\overline{S}$ Active Hold time (relative to C)	5			ns
t_{SHCH}		$\overline{S}$ Not Active Setup time (relative to C)	5			ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect time	100			ns
t_{SHQZ}(4)	t_{DIS}	Output Disable time			8	ns
t_{CLQV}	t_V	Clock Low to Output Valid under 30 pF/10 pF			8/6	ns
t_{CLQX}	t_{HO}	Output Hold time	0			ns
t_{WHSL}(5)		Write Protect Setup time	50			ns
t_{SHWL}(5)		Write Protect Hold time	100			ns
t_{DP}(4)		$\overline{S}$ to Deep Power-down			3	µs
t_{RDP}(4)		$\overline{S}$ High to Standby mode			30	µs
t_W		Write Status Register cycle time		3	15	ms
t_{PW}(6)		Page Write cycle time (256 bytes)		11	23	ms
t_{PP}(6)		Page Program cycle time (256 bytes)		0.8	3	ms
		Page Program cycle time (n bytes)		int(n/8) × 0.025(7)		
t_{PE}		Page Erase cycle time		10	20	ms
t_{SE}		Sector Erase cycle time		1.5	5	s
t_{SSE}		Subsector Erase cycle time		80	150	ms
t_{BE}		Bulk Erase cycle time		8	10	s

1. See *Important note on page 6*.
2. Details of how to find the technology process in the marking are given in AN1995, see also *Section 13: Ordering information*.
3. $t_{CH} + t_{CL}$ must be greater than or equal to $1/ f_C$.
4. Value guaranteed by characterization, not 100% tested in production.
5. Only applicable as a constraint for a WRSR instruction when SRWD is set to ‘1’.
6. When using PP and PW instructions to update consecutive bytes, optimized timings are obtained with one sequence including all the bytes versus several sequences of only a few bytes ($1 \le n \le 256$).
7. int(A) corresponds to the upper integer part of A. For instance, int(12/8) = 2, int(32/8) = 4 int(15.3) =16.

Table 22. AC characteristics (75 MHz operation, T9HX (0.11µm) process(1))(2)(3)(4)

Test conditions specified in *Table 14* and *Table 15*						
Symbol	**Alt.**	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
f_C	f_C	Clock frequency for the following instructions: FAST_READ, RDLR, PW, PP, WRLR, PE, SE, SSE, DP, RDP, WREN, WRDI, RDSR, WRSR	D.C.		75	MHz
f_R		Clock frequency for READ instructions	D.C.		33	MHz
t_{CH}(5)	t_{CLH}	Clock High time	6			ns
t_{CL}(5)	t_{CLL}	Clock Low time	6			ns
		Clock Slew Rate (peak to peak)	0.1			V/ns
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup time (relative to C)	5			ns
t_{CHSL}		$\overline{S}$ Not Active Hold time (relative to C)	5			ns
t_{DVCH}	t_{DSU}	Data In Setup time	2			ns
t_{CHDX}	t_{DH}	Data In Hold time	5			ns
t_{CHSH}		$\overline{S}$ Active Hold time (relative to C)	5			ns
t_{SHCH}		$\overline{S}$ Not Active Setup time (relative to C)	5			ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect time	100			ns
t_{SHQZ}(6)	t_{DIS}	Output Disable time			8	ns
t_{CLQV}	t_V	Clock Low to Output Valid			8/6	ns
t_{CLQX}	t_{HO}	Output Hold time	0			ns
t_{WHSL}(7)		Write Protect Setup time	20			ns
t_{SHWL}(7)		Write Protect Hold time	100			ns
t_{DP}(6)		$\overline{S}$ to Deep Power-down			3	µs
t_{RDP}(6)		$\overline{S}$ High to Standby mode			30	µs
t_W		Write Status Register cycle time		3	15	ms
t_{PW}(8)		Page Write cycle time (256 bytes)		11	23	ms
t_{PP}(8)		Page Program cycle time (256 bytes)		0.8	3	ms
		Page Program cycle time (n bytes)		int(n/8) × 0.025(9)		
t_{PE}		Page Erase cycle time		10	20	ms
t_{SE}		Sector Erase cycle time		1.5	5	s
t_{SSE}		Subsector Erase cycle time		80	150	ms
t_{BE}		Bulk Erase cycle time		8	10	s

1. See *Important note on page 6*.
2. Details of how to find the technology process in the marking are given in AN1995, see also *Section 13: Ordering information*.
3. Delivery of parts operating with a maximum clock rate of 75 MHz starts from week 8 of 2008.
4. Preliminary data.
5. $t_{CH} + t_{CL}$ must be greater than or equal to $1/ f_C$.
6. Value guaranteed by characterization, not 100% tested in production.
7. Only applicable as a constraint for a WRSR instruction when SRWD is set to ‘1’.

8. When using PP and PW instructions to update consecutive bytes, optimized timings are obtained with one sequence including all the bytes versus several sequences of only a few bytes ($1 \leq n \leq 256$).
9. int(A) corresponds to the upper integer part of A. For instance, int(12/8) = 2, int(32/8) = 4 int(15.3) =16.

Figure 26. Serial input timing

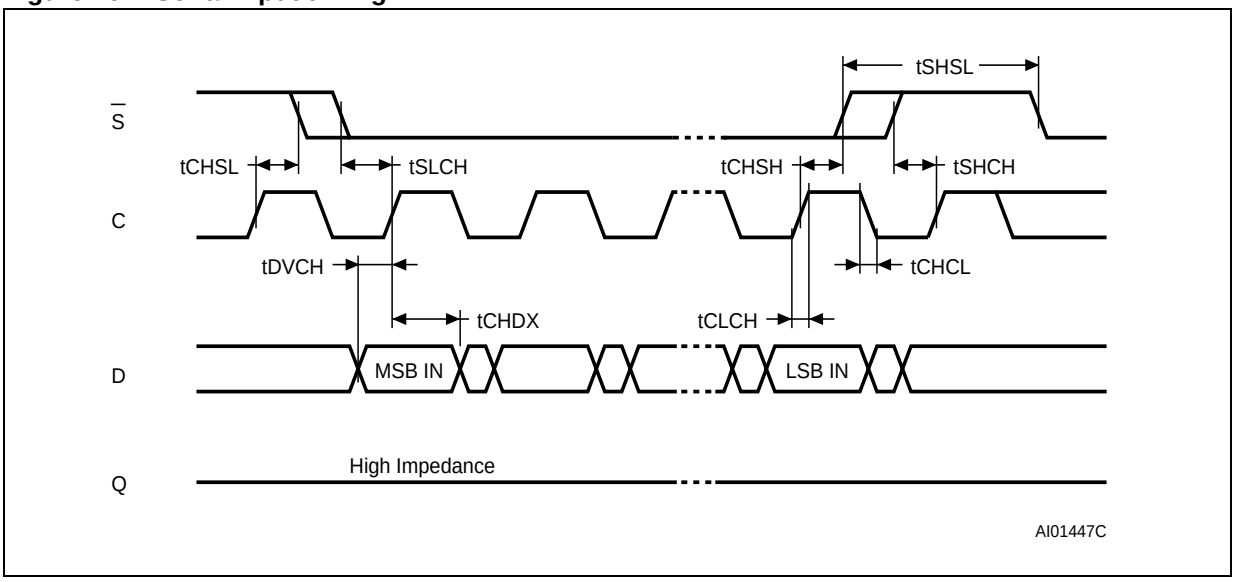
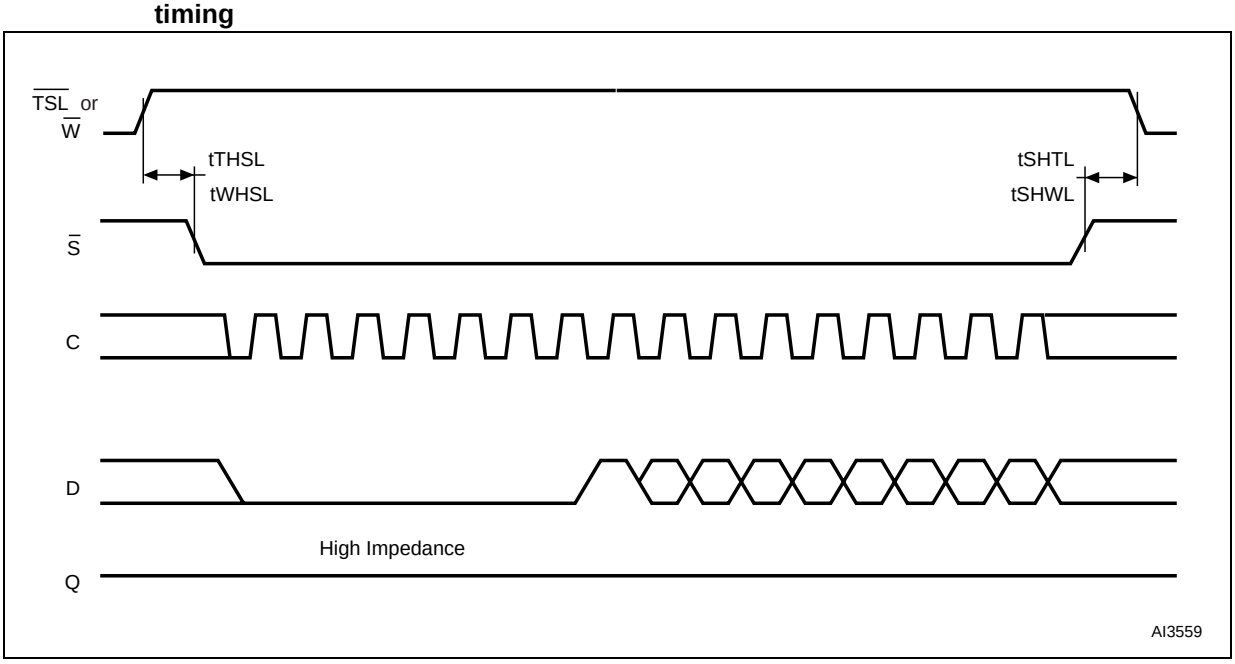


Figure 27. Top Sector Lock (T7X process) or Write Protect (T9HX process) setup and hold timing



1. For the differences between devices produced in the two processes, see *Important note on page 6*.

Figure 28. Output timing

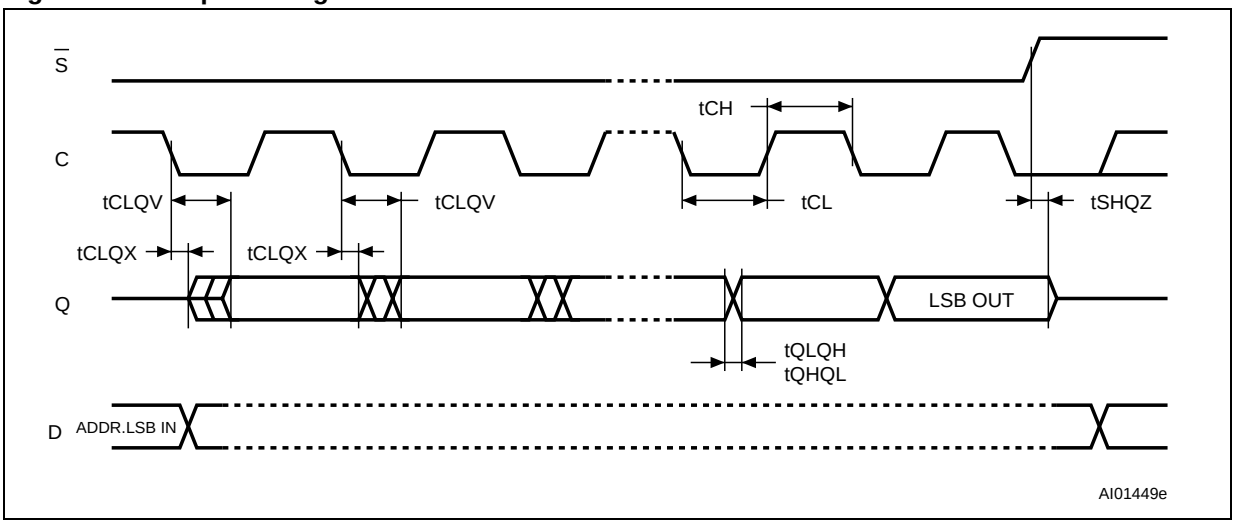


Table 23. Reset conditions

Test conditions specified in *Table 14* and *Table 15*							
Symbol	**Alt.**	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
t_{RLRH}(1)	t_{RST}	Reset pulse width		10			µs
t_{SHRH}		Chip Select High to Reset High	Chip should have been deselected before Reset is de-asserted	10			ns

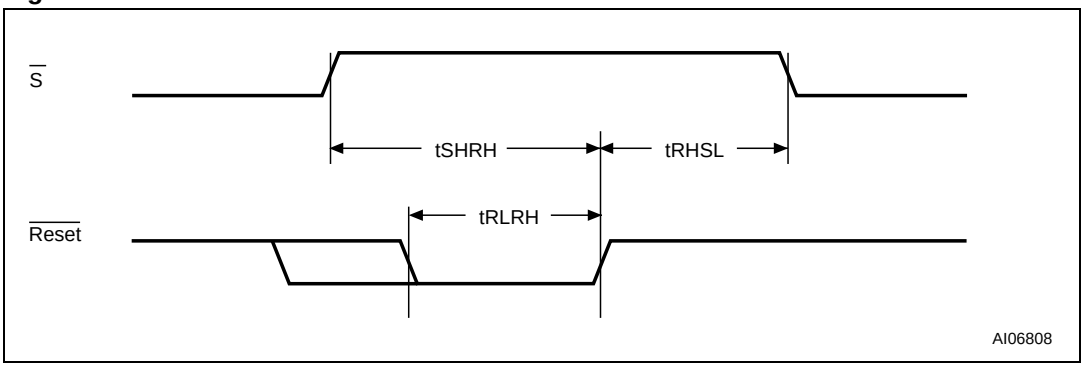
1. Value guaranteed by characterization, not 100% tested in production.

Table 24. Timings after a $\overline{\text{Reset}}$ Low pulse(1)(2)

Test conditions specified in *Table 14* and *Table 15*					
Symbol	**Alt.**	**Parameter**	**Conditions: Reset pulse occurred**	**Max.**	**Unit**
t_{RHSL}	t_{REC}	Reset recovery time	While decoding an instruction(3): WREN, WRDI, RDID, RDSR, READ, RDLR, Fast_Read, WRLR, PW, PP, PE, SE, BE, SSE, DP, RDP	30	µs
			Under completion of an Erase or Program cycle of a PW, PP, PE, SE, BE operation	300	µs
			Under completion of an Erase cycle of an SSE operation	3	ms
			Under completion of a WRSR operation	t_W (see *Table 21*)	ms
			Device deselected ($\overline{S}$ High) and in Standby mode	0	µs

1. All the values are guaranteed by characterization, and not 100% tested in production.
2. See *Table 12* for a description of the device status after a $\overline{\text{Reset}}$ Low pulse.
3. $\overline{S}$ remains Low while $\overline{\text{Reset}}$ is Low.

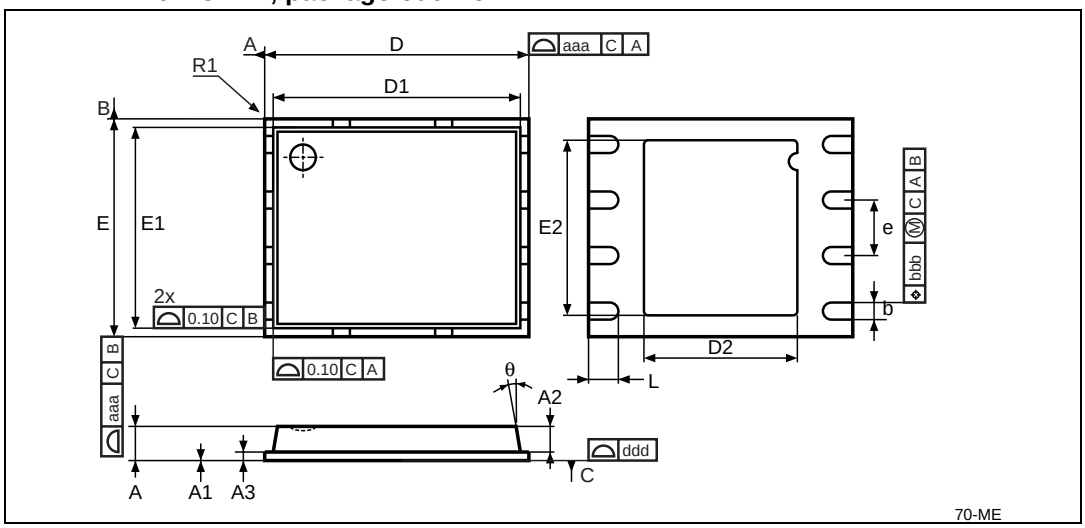
Figure 29. Reset AC waveforms



12 Package mechanical

In order to meet environmental requirements, Numonyx offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 30. VFQFPN8 (MLP8) 8-lead very thin fine pitch quad flat package no lead 6 × 5 mm, package outline



1. Drawing is not to scale.
2. The circle in the top view of the package indicates the position of pin 1.

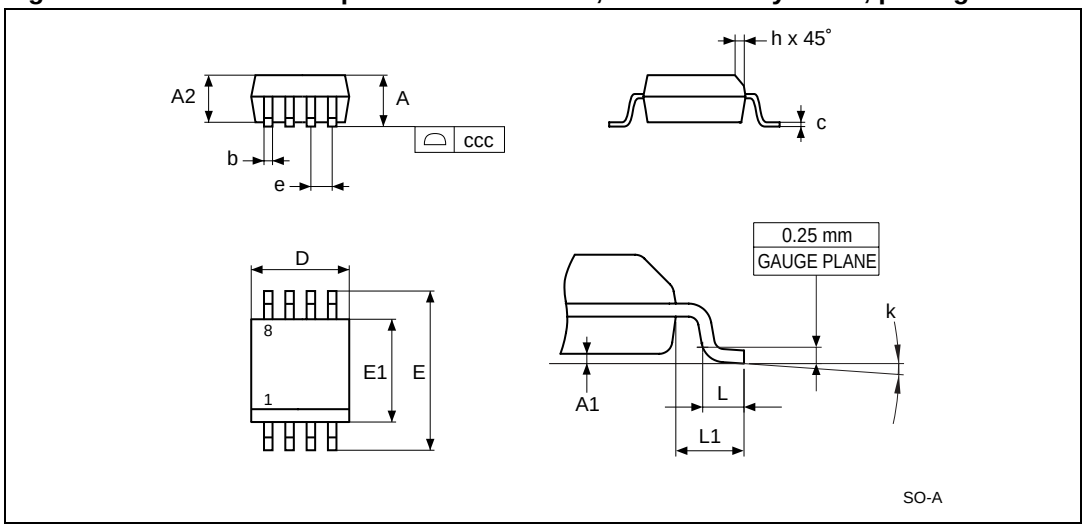
Table 25. VFQFPN8 (MLP8) 8-lead very thin fine pitch quad flat package no lead 6 × 5 mm, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	0.85	0.80	1.00	0.033	0.031	0.039
A1		0.00	0.05		0.000	0.002
A2	0.65			0.026		
A3	0.20			0.008		
b	0.40	0.35	0.48	0.016	0.014	0.019
D	6.00			0.236		
D1	5.75			0.226		
D2	3.40	3.20	3.60	0.134	0.126	0.142
E	5.00			0.197		
E1	4.75			0.187		
E2	4.00	3.80	4.30	0.157	0.150	0.169
e	1.27	–	–	0.050	–	–
R1	0.10	0.00		0.004	0.000	

Table 25. VFQFPN8 (MLP8) 8-lead very thin fine pitch quad flat package no lead 6 × 5 mm, package mechanical data (continued)

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
L	0.60	0.50	0.75	0.024	0.020	0.029
Θ			12°			12°
aaa			0.15			0.006
bbb			0.10			0.004
ddd			0.05			0.002

Figure 31. SO8N – 8 lead plastic small outline, 150 mils body width, package outline

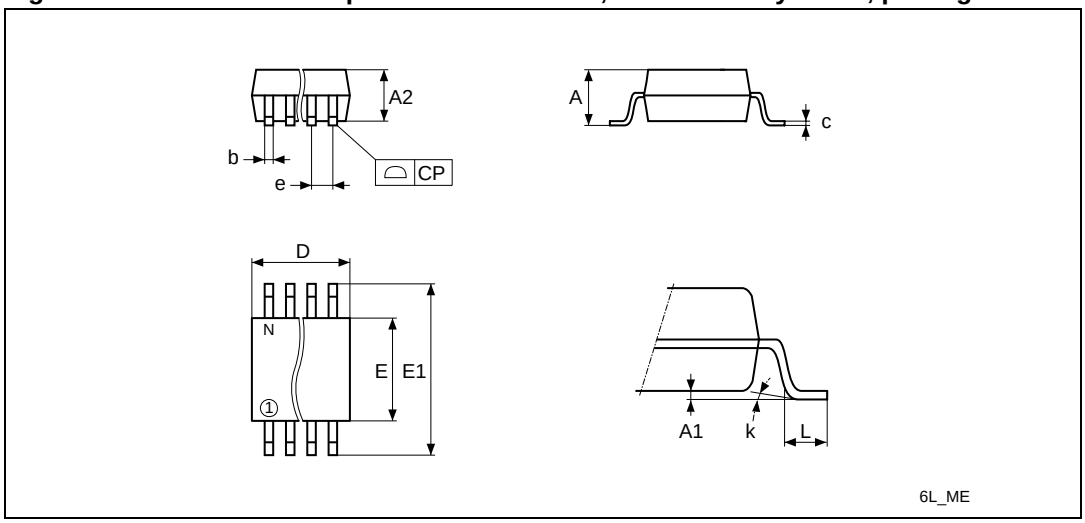


1. Drawing is not to scale.

Table 26. SO8N – 8 lead plastic small outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2		1.25			0.049	
b		0.28	0.48		0.011	0.019
c		0.17	0.23		0.007	0.009
ccc			0.10			0.004
D	4.90	4.80	5.00	0.193	0.189	0.197
E	6.00	5.80	6.20	0.236	0.228	0.244
E1	3.90	3.80	4.00	0.154	0.150	0.157
e	1.27	–	–	0.050	–	–
h		0.25	0.50		0.010	0.020
k		0°	8°		0°	8°
L		0.40	1.27		0.016	0.050
L1	1.04			0.041		

Figure 32. SO8W – 8 lead plastic small outline, 208 mils body width, package outline



1. Drawing is not to scale.

Table 27. SO8W – 8 lead plastic small outline, 208 mils body width, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.50			0.098
A1		0.00	0.25		0.000	0.010
A2		1.51	2.00		0.059	0.079
b	0.40	0.35	0.51	0.016	0.014	0.020
c	0.20	0.10	0.35	0.008	0.004	0.014
CP			0.10			0.004
D			6.05			0.238
E		5.02	6.22		0.198	0.245
E1		7.62	8.89		0.300	0.350
e	1.27	–	–	0.050	–	–
k		0°	10°		0°	10°
L		0.50	0.80		0.020	0.031
N	8			8		

13 Ordering information

Table 28. Ordering information scheme

Example: M25PE40 V MP 6 T G

Device type

M25PE = page-erasable serial Flash memory

Device function

40 = 4 Mbit (512Kbit × 8)

Operating voltage

V = V_{CC} = 2.7 to 3.6 V

Package

MW = SO8W (208 mils width)

MP = VFQFPN8 6 × 5 mm (MLP8)

MN = SO8N (150 mils width)(1)

Device grade

6 = Industrial: device tested with standard test flow over –40 to 85 °C

Option

blank = standard packing

T = tape and reel packing

Plating technology

P or G = ECOPACK® (RoHS compliant)

1. Package only available for products in the T9HX process.

Note: For a list of available options (speed, package, etc.), for further information on any aspect of this device or when ordering parts operating at 75 MHz (0.11 µm, process digit '4'), please contact your nearest Numonyx Sales Office.

14 Revision history

Table 29. Document revision history

Date	Revision	Changes
01-Apr-2004	0.1	Initial release.
09-Nov-2004	1	Write Protect ($\overline{W}$) pin replaced by Top Block Lock ($\overline{TBL}$). *Section 2.5: Reset (Reset)* description modified. JEDEC signature modified. Reset timings t_{RLRH}, t_{RHSL} and t_{SHRH} removed from *Table 20: AC characteristics (33 MHz operation)* and inserted in *Table 21: Reset timings* (t_{RHSL} modified). Document status promoted from target specification to preliminary data.
01-Dec-2004	2	Top Block Lock ($\overline{TBL}$) renamed as Top Sector Lock ($\overline{TSL}$). Small text changes. Deep Power-down mode clarified in *Section 4.6: Active Power, Standby Power and Deep Power-down modes*.
11-Jan-2005	3	Notes removed from *Table 28: Ordering information scheme*. Wording changes. SO16 package removed, SO8 wide package added.
4-Oct-2005	4	Added *Table 20: AC characteristics (33 MHz operation)*. Document status promoted from preliminary data to full datasheet. *Table 19: AC characteristics (25 MHz operation)* updated. *Section 4.2: An easy way to modify data*, *Section 4.3: A fast way to modify data*, *Section 6.9: Page Write (PW)* and *Section 6.10: Page Program (PP)* updated to explain optimal use of Page Write and Page Program instructions. Clock slew rate changed from 0.03 to 0.1 V/ns. Updated *Table 28: Ordering information scheme*. Added ECOPACK® information.
11-Aug 2006	5	Changed document to new template; amended figure in Feature summary; replaced *Figure 4: Bus master and memory devices on the SPI bus*; amended data in *Table 19* and *Table 20*; amended title of *Figure 30: VFQFPN8 (MLP8) 8-lead very thin fine pitch quad flat package no lead 6 × 5 mm, package outline* and added a footnote; amended name of the MP package in *Table 28: Ordering information scheme*.

Table 29. Document revision history (continued)

Date	Revision	Changes
15-Jan-2007	6	50 MHz frequency added. SO8N package added, VFQFPN and SO8W package specifications updated (see *Section 12: Package mechanical*). The sectors are further divided up into subsectors (see *Table 4: Memory organization*). *Important note on page 6* added. *Figure 4: Bus master and memory devices on the SPI bus* updated and explanatory paragraph added. *VCC supply voltage* and *VSS ground* added. *Section 4.8: Protection modes* modified. *Section 8: Reset* added, reset timings table split into *Table 23: Reset conditions* and *Table 24: Timings after a Reset Low pulse*. At power-up the WIP bit is reset (see *Section 7: Power-up and power-down*). V_{IO} max changed in *Table 13: Absolute maximum ratings*. End timing line of t_{SHQZ} moved in *Figure 28: Output timing*. Products processed in T9HX process added to datasheet: – $\overline{WP}$ pin replaces $\overline{TSL}$ (T7X technology), see *Section 2.6: Write Protect (W) or Top Sector Lock (TSL)* – *Write Status Register (WRSR)* and *Subsector Erase (SSE)* instructions added for T9HX process – subsector protection granularity removed in T9HX process, still exists in T7X process – *Table 4: Memory organization* updated to show subsectors – Status Register *BP2, BP1, BP0 bits* and *SRWD bit* added. Small text changes.
23-Jan-2007	7	T7X process name corrected. Write Enable Latch (WEL) bit is reset also on completion of the Subsector Erase, Bulk Erase, Write to Lock Register and Write Status Register instructions (see *Section 6.2: Write Disable (WRDI)*). Address bit A20 is *not* Don't care (*Note 1* modified) in the *Sector Erase (SE) instruction sequence*. SO8N package is only available in products manufactured in the T9HX process.
10-Dec-2007	8	Removed 'low voltage' from the title. *Table 18: DC characteristics (75 MHz operation, T9HX (0.11 µm) process)* and *Table 22: AC characteristics (75 MHz operation, T9HX (0.11µm) process)* added. Added ECOPACK® text in *Section 12: Package mechanical*. Updated the value for the maximum clock frequency (from 50 to 75 MHz) through the document. Minor text changes.
03-Jan-2007	9	Applied Numonyx branding.

Please Read Carefully: