

- Surface Mount
- Dynamic dv/dt Rating
- Logic-Level Gate Drive
- Fast Switching
- Ease of Paralleling
- Advanced Process Technology
- Ultra Low On-Resistance
- Lead-Free

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The SOT-223 package is designed for surface-mount using vapor phase, infra red, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of 1.0W is possible in a typical surface mount application

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^{**}$	5.2	A
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^*$	3.8	
$I_D @ T_A = 70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^*$	3.0	
I_{DM}	Pulsed Drain Current ①	30	
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation (PCB Mount)**	2.1	W
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation (PCB Mount)*	1.0	W
	Linear Derating Factor (PCB Mount)*	8.3	mW/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy②	110	mJ
I_{AR}	Avalanche Current①	3.8	A
E_{AR}	Repetitive Avalanche Energy①	0.10	mJ
dv/dt	Peak Diode Recovery dv/dt ③	7.5	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Amb. (PCB Mount, steady state)*	93	120	°C/W
$R_{\theta JA}$	Junction-to-Amb. (PCB Mount, steady state)**	48	60	

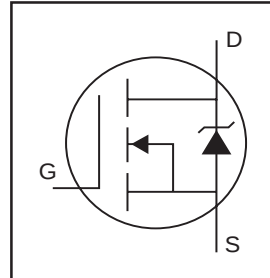
* When mounted on FR-4 board using minimum recommended footprint.

** When mounted on 1 inch square copper board, for comparison with other SMD devices.

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IRLL2705PbF

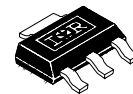
HEXFET® Power MOSFET



$$V_{DSS} = 55V$$

$$R_{DS(on)} = 0.04\Omega$$

$$I_D = 3.8A$$



SOT-223

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.061	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.040	Ω	$V_{GS} = 10V, I_D = 3.8A$ ④
		—	—	0.051		$V_{GS} = 5.0V, I_D = 3.8A$ ④
		—	—	0.065		$V_{GS} = 4.0V, I_D = 1.9A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	5.1	—	—	S	$V_{DS} = 25V, I_D = 1.9A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 55V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 44V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
Q_g	Total Gate Charge	—	32	48	nC	$I_D = 3.8A$
Q_{gs}	Gate-to-Source Charge	—	3.5	5.3		$V_{DS} = 44V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	9.7	14		$V_{GS} = 10V$, See Fig. 6 and 9 ④
$t_{d(on)}$	Turn-On Delay Time	—	6.2	—	ns	$V_{DD} = 28V$
t_r	Rise Time	—	12	—		$I_D = 3.8A$
$t_{d(off)}$	Turn-Off Delay Time	—	35	—		$R_G = 6.2\Omega$
t_f	Fall Time	—	22	—		$R_D = 7.1\Omega$, See Fig. 10 ④
C_{iss}	Input Capacitance	—	870	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	220	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	92	—		$f = 1.0\text{MHz}$, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	0.91	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	30		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 3.8A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	58	88	ns	$T_J = 25^\circ\text{C}, I_F = 3.8A$
Q_{rr}	Reverse Recovery Charge	—	140	210	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

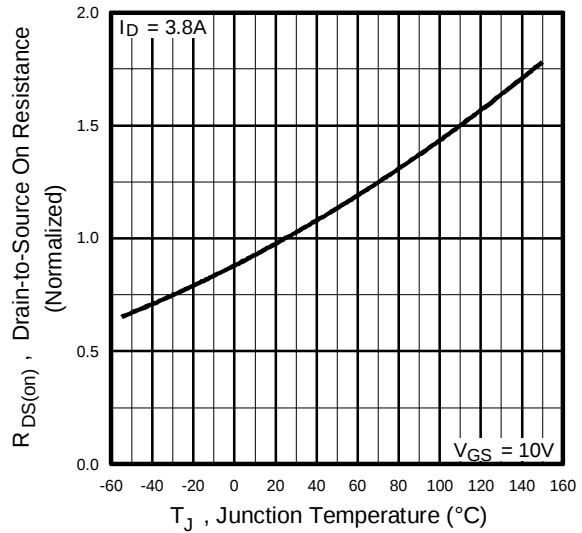
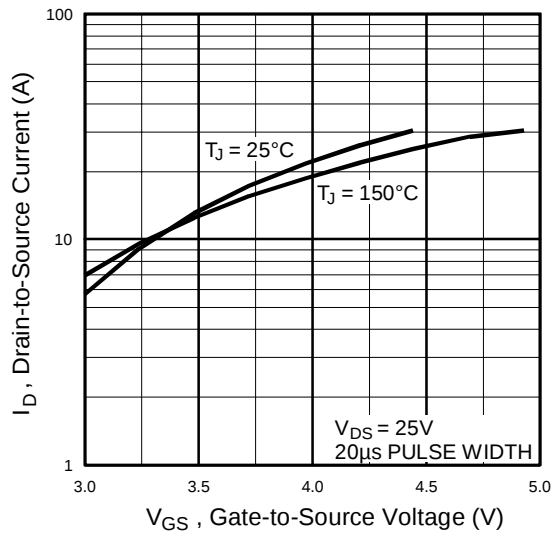
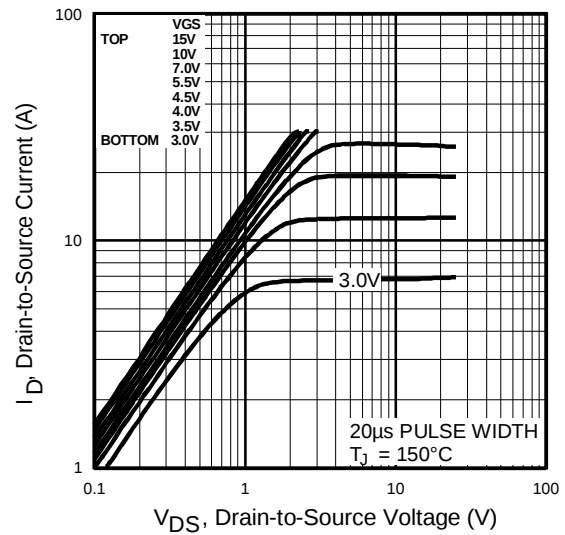
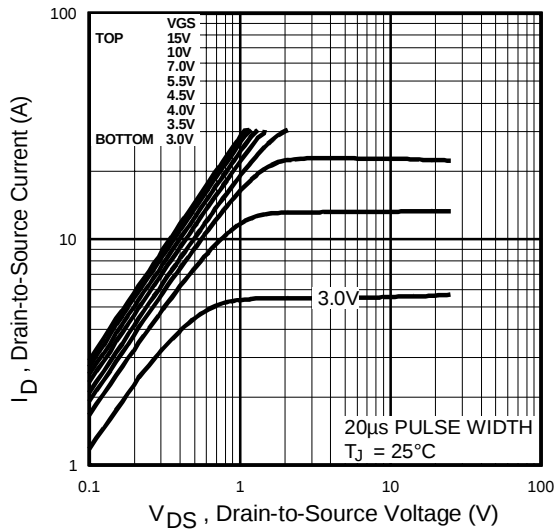
Notes:

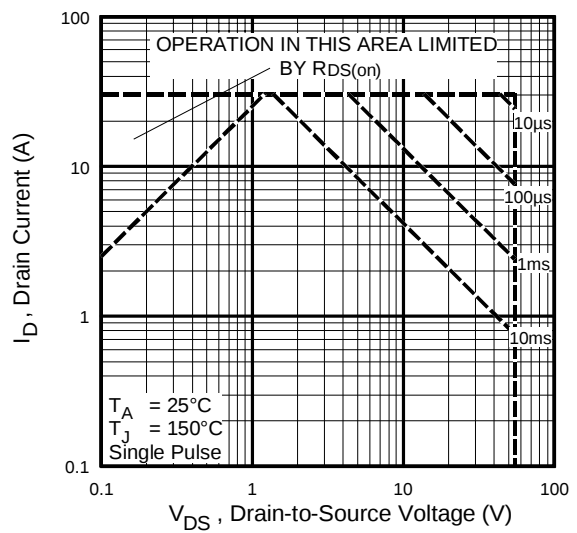
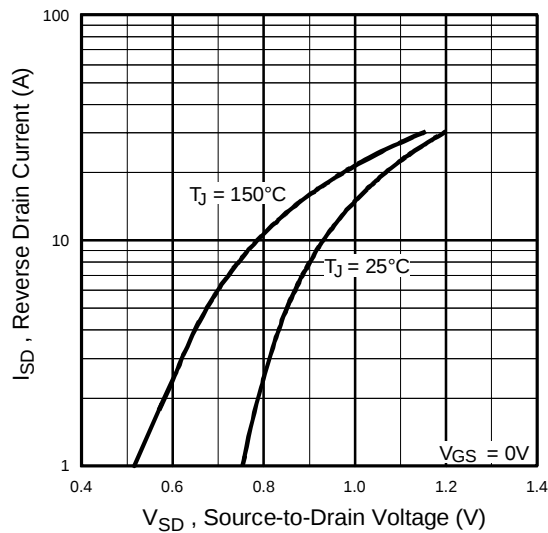
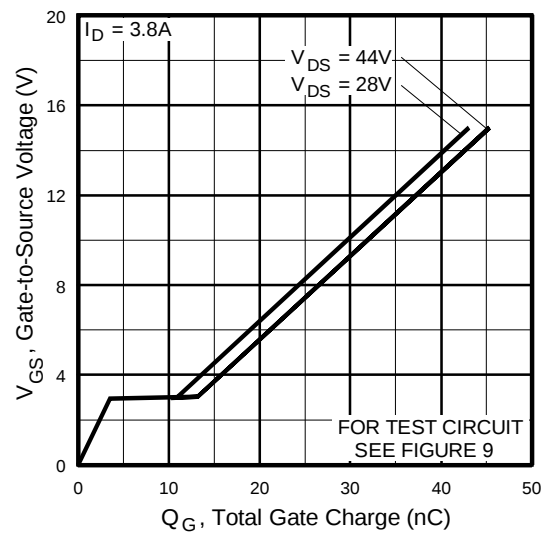
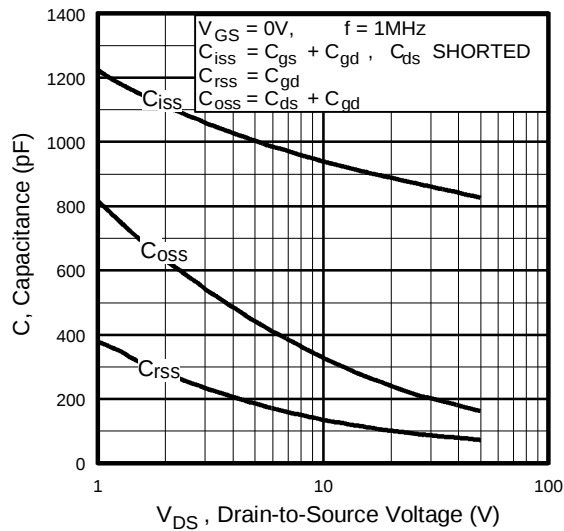
① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② $V_{DD} = 25V$, starting $T_J = 25^\circ\text{C}$, $L = 15\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 3.8A$. (See Figure 12)

③ $I_{SD} \leq 3.8A$, $di/dt \leq 220A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.





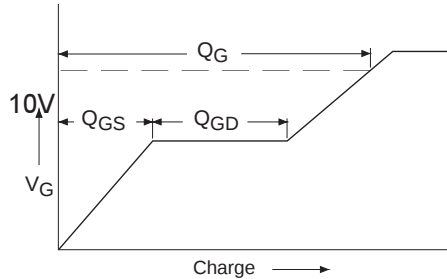


Fig 9a. Basic Gate Charge Waveform

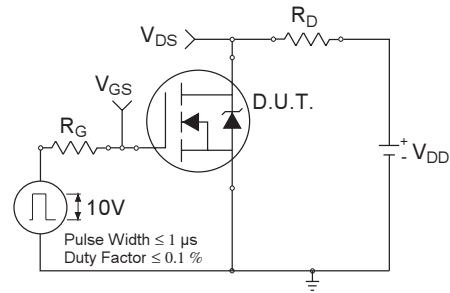


Fig 10a. Switching Time Test Circuit

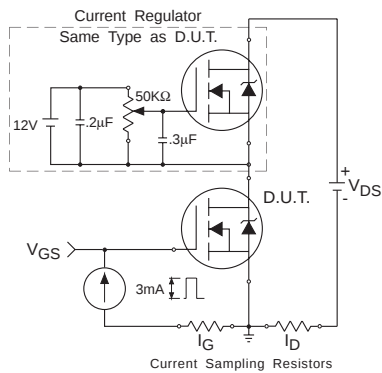


Fig 9b. Gate Charge Test Circuit

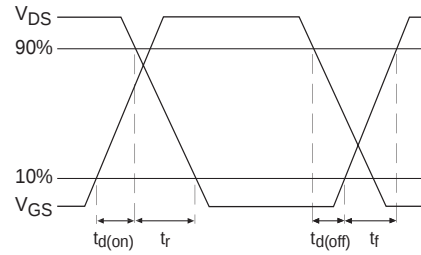


Fig 10b. Switching Time Waveforms

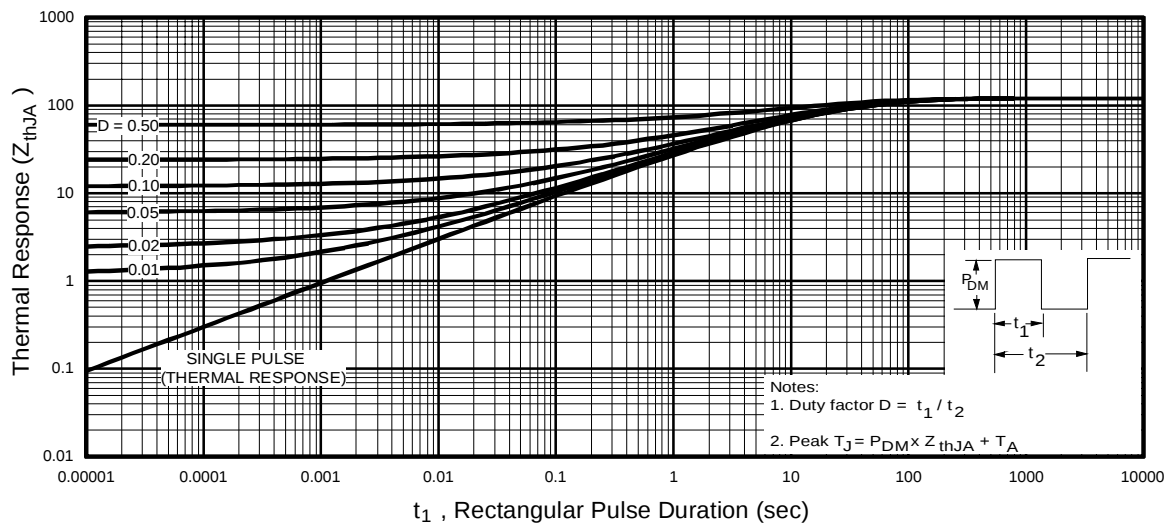


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

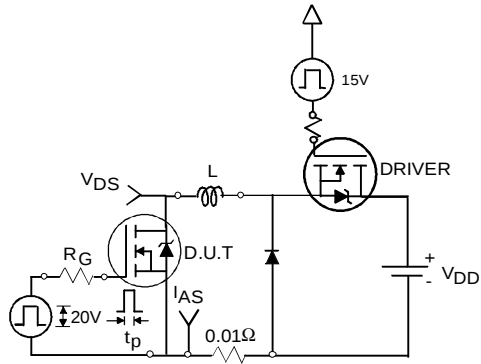


Fig 12a. Unclamped Inductive Test Circuit

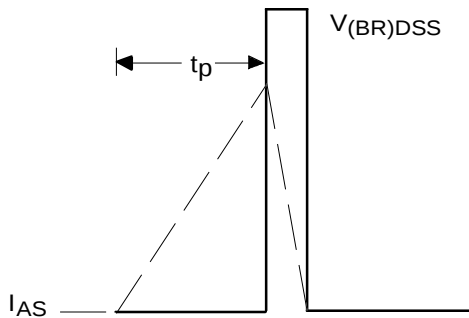


Fig 12b. Unclamped Inductive Waveforms

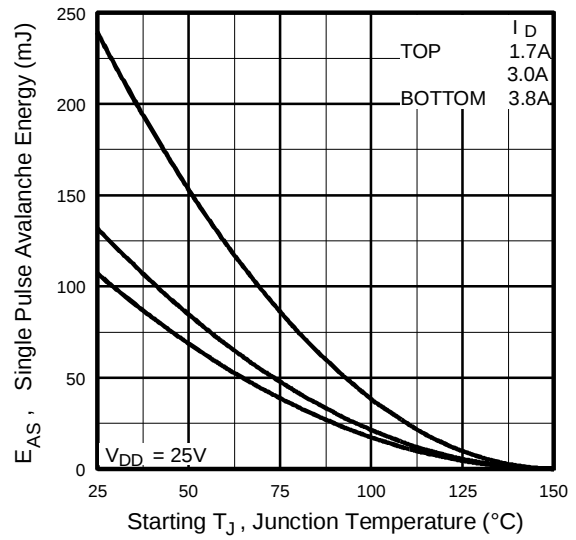


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

Peak Diode Recovery dv/dt Test Circuit

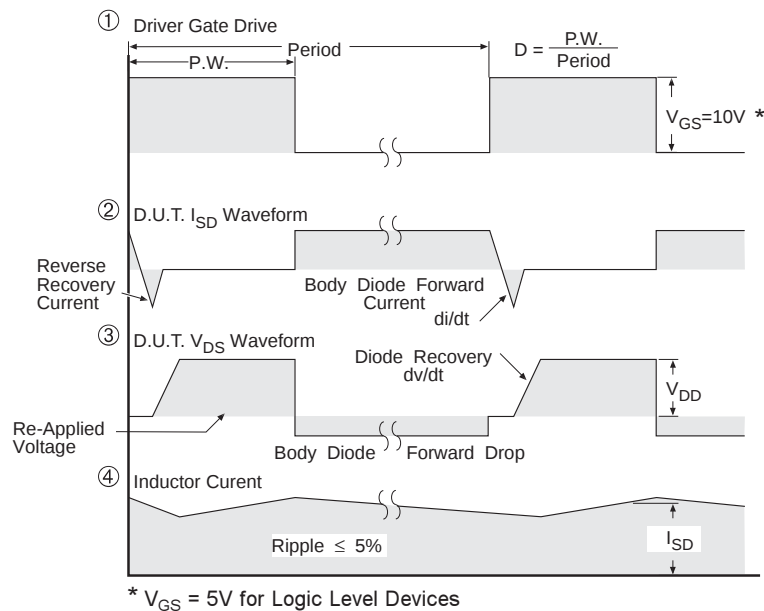
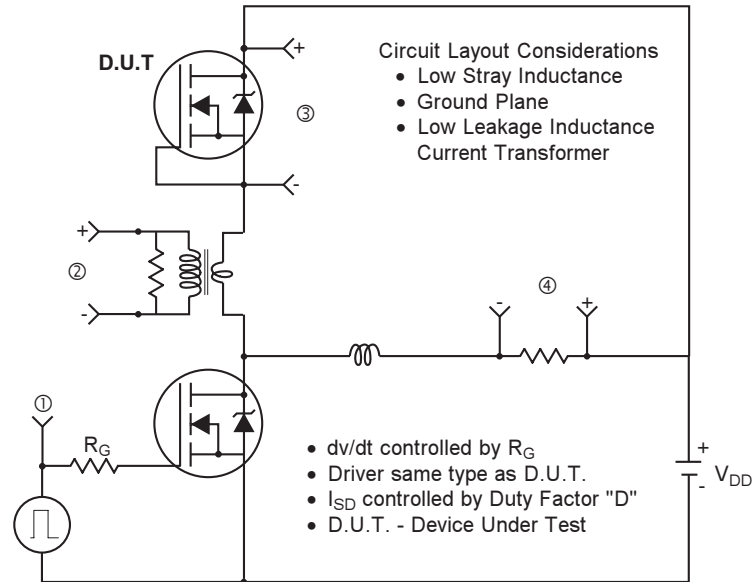


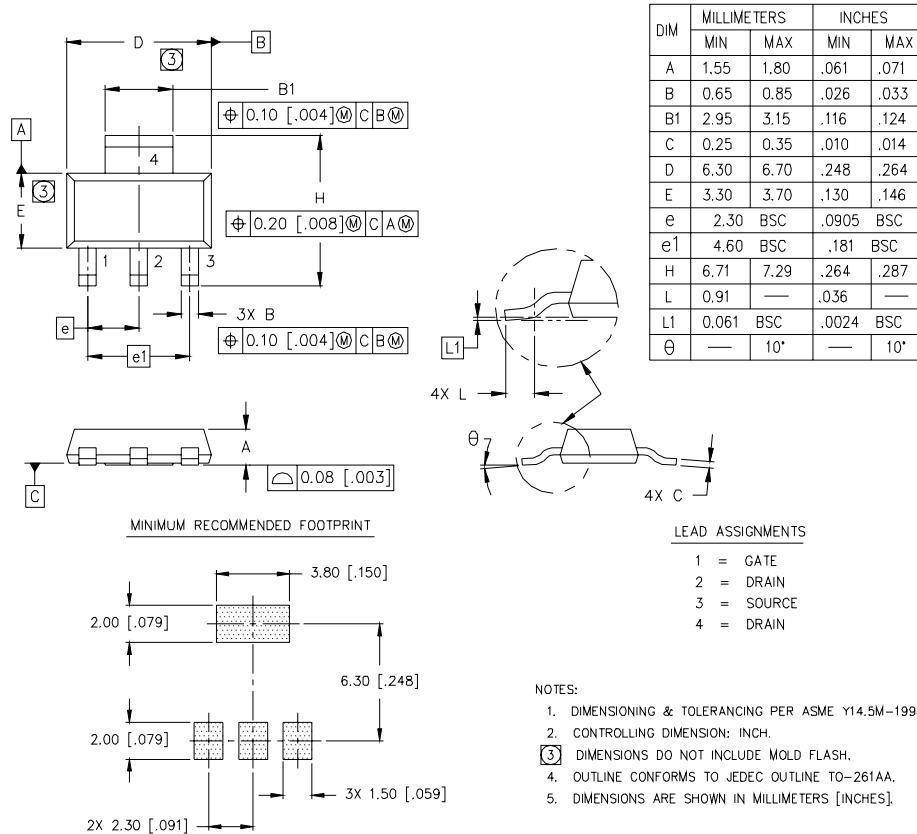
Fig 13. For N-Channel HEXFETS

IRLL2705PbF

International
IR Rectifier

SOT-223 (TO-261AA) Package Outline

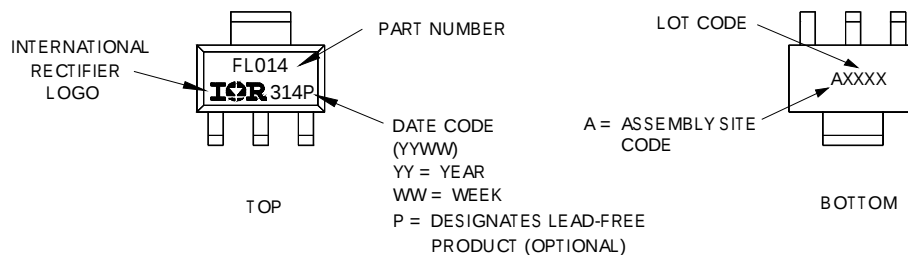
Dimensions are shown in millimeters (inches)



SOT-223 (TO-261AA) Part Marking Information

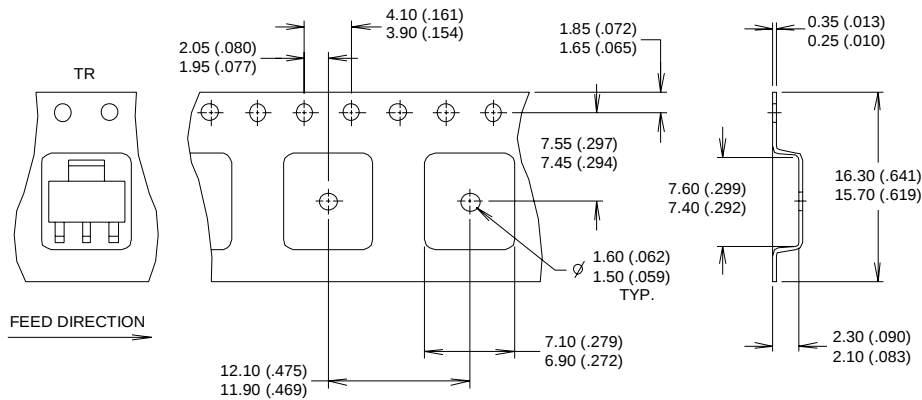
HEXFET PRODUCT MARKING

EXAMPLE: THIS IS AN IRFL014



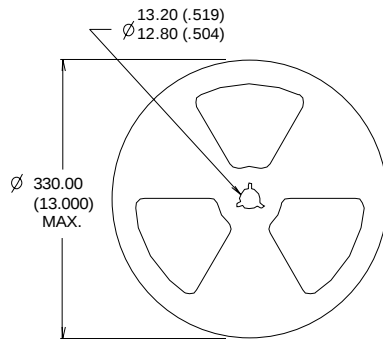
SOT-223 (TO-261AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



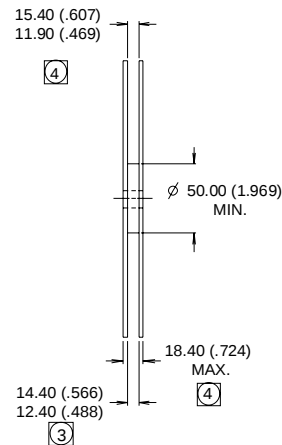
NOTES :

1. CONTROLLING DIMENSION: MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.
3. EACH ϕ 330.00 (13.00) REEL CONTAINS 2,500 DEVICES.



NOTES :

1. OUTLINE COMFORMS TO EIA-418-1.
2. CONTROLLING DIMENSION: MILLIMETER..
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.



Data and specifications subject to change without notice.