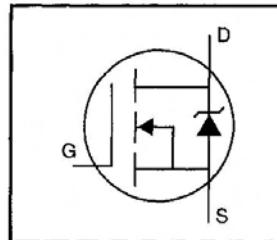


IRLD120PbF

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- Logic-Level Gate Drive
- R_{DS(on)} Specified at V_{GS}=4V & 5V
- 175°C Operating Temperature
- Lead-Free

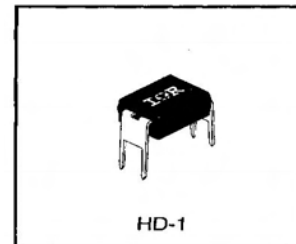


V_{DSS} = 100V
 R_{DS(on)} = 0.27Ω
 I_D = 1.3A

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4-pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1 inch pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 watt.



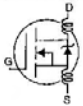
Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 5.0 V	1.3	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 5.0 V	0.94	
I _{DM}	Pulsed Drain Current ①	10	
P _D @ T _C = 25°C	Power Dissipation	1.3	W
	Linear Derating Factor	0.0083	W/°C
V _{GS}	Gate-to-Source Voltage	±10	V
E _{AS}	Single Pulse Avalanche Energy ②	690	mJ
I _{AR}	Avalanche Current ①	1.3	A
E _{AR}	Repetitive Avalanche Energy ①	0.13	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

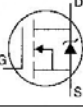
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
R _{θJA}	Junction-to-Ambient	—	—	120	°C/W

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} =0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.27	Ω	V _{GS} =5.0V, I _D =0.78A ④
		—	—	0.38		V _{GS} =4.0V, I _D =0.65A ④
V _{GS(th)}	Gate Threshold Voltage	1.0	—	2.0	V	V _{DS} =V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	1.9	—	—	S	V _{DS} =50V, I _D =0.78A ④
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} =100V, V _{GS} =0V
		—	—	250		V _{DS} =80V, V _{GS} =0V, T _J =150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} =10V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} =-10V
Q _g	Total Gate Charge	—	—	12	nC	I _D =9.2A
Q _{gs}	Gate-to-Source Charge	—	—	3.0		V _{DS} =80V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	7.1		V _{GS} =5.0V See Fig. 6 and 13 ④
t _{d(on)}	Turn-On Delay Time	—	9.8	—	ns	V _{DD} =50V
t _r	Rise Time	—	64	—		I _D =9.2A
t _{d(off)}	Turn-Off Delay Time	—	21	—		R _G =9.0Ω
t _f	Fall Time	—	27	—		R _D =5.2Ω See Figure 10 ④
L _D	Internal Drain Inductance	—	4.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	6.0	—		
C _{iss}	Input Capacitance	—	490	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	150	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	30	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	1.3	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	10		
V _{SD}	Diode Forward Voltage	—	—	2.5	V	T _J =25°C, I _S =1.3A, V _{GS} =0V ④
t _{rr}	Reverse Recovery Time	—	130	140	ns	T _J =25°C, I _F =9.2A
Q _{rr}	Reverse Recovery Charge	—	0.83	1.0	μC	di/dt=100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V_{DD}=25V, starting T_J=25°C, L=153mH R_G=25Ω, I_{AS}=2.6A (See Figure 12)
- ③ I_{SD}≤9.2A, di/dt≤110A/μs, V_{DD}≤V_{(BR)DSS}, T_J≤175°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.

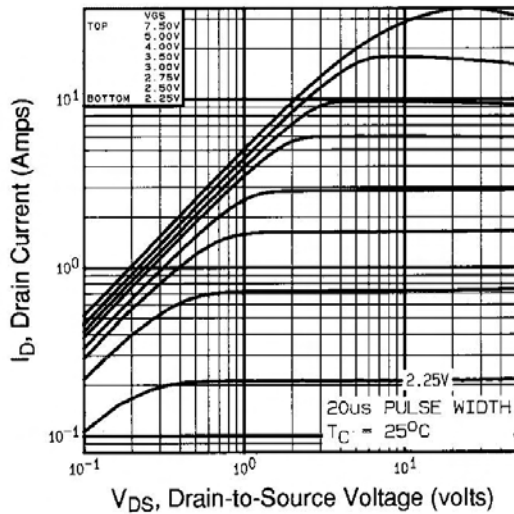


Fig 1. Typical Output Characteristics,
 $T_C=25^\circ\text{C}$

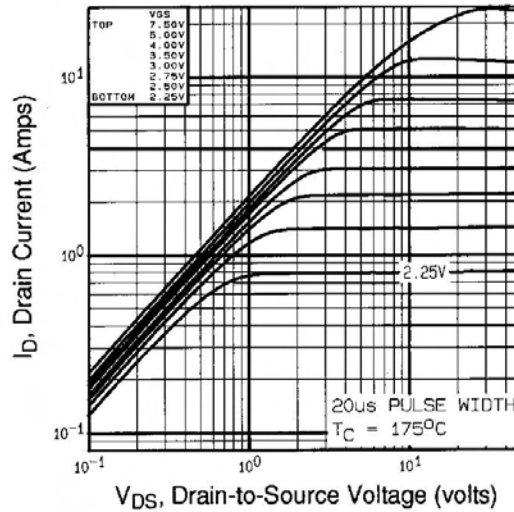


Fig 2. Typical Output Characteristics,
 $T_C=175^\circ\text{C}$

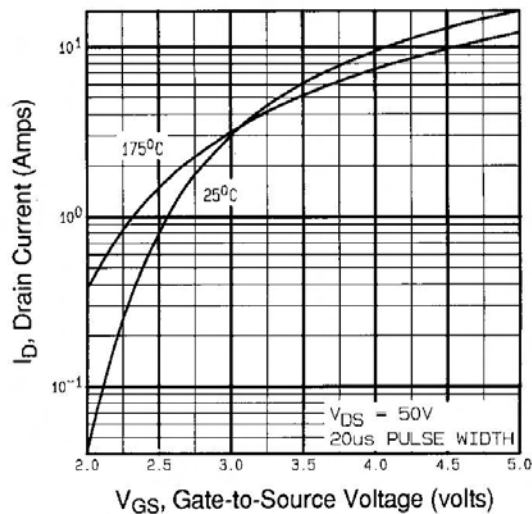


Fig 3. Typical Transfer Characteristics

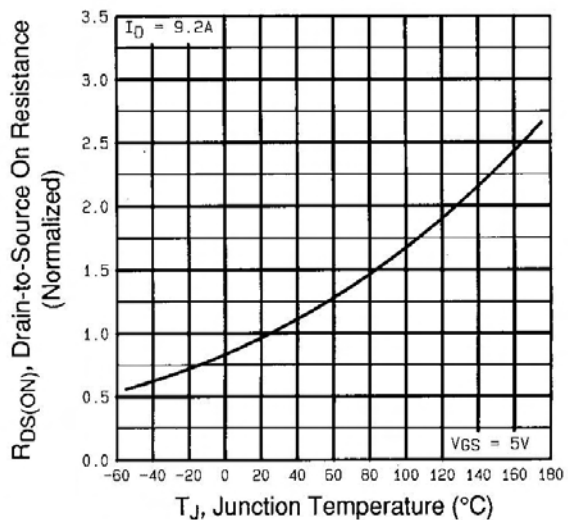


Fig 4. Normalized On-Resistance
Vs. Temperature

IRLD120PbF

International
IR Rectifier

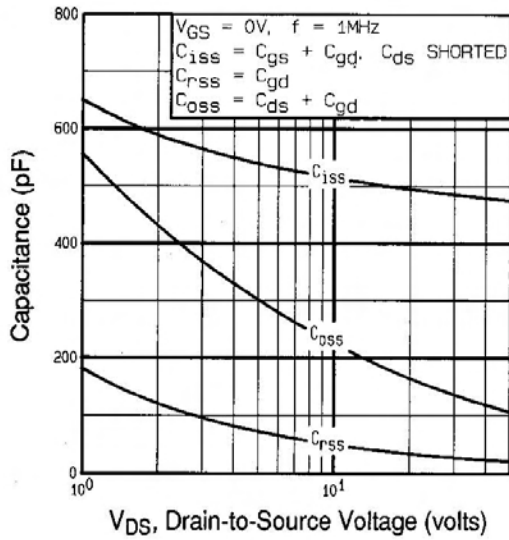


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

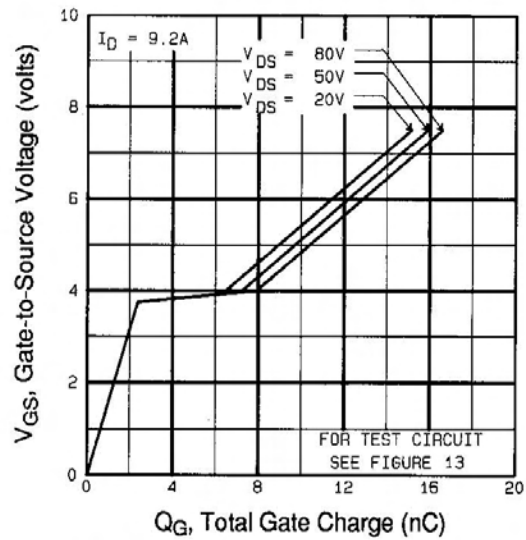


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

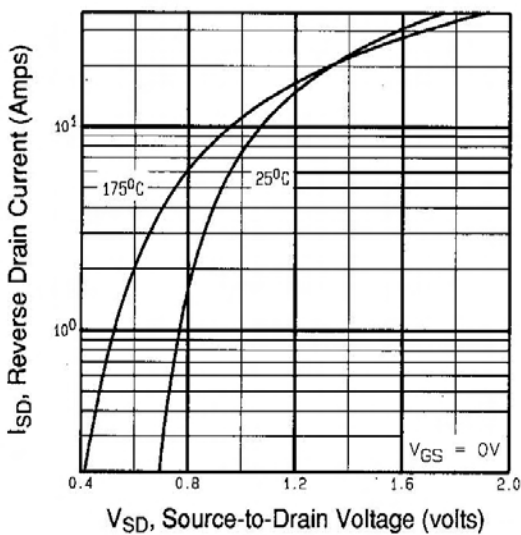


Fig 7. Typical Source-Drain Diode Forward Voltage

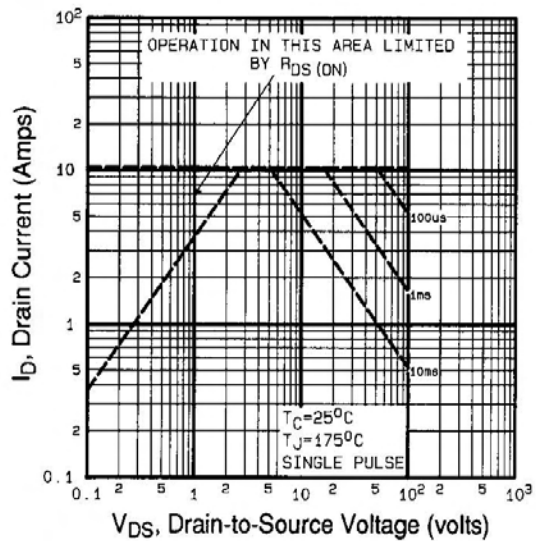


Fig 8. Maximum Safe Operating Area

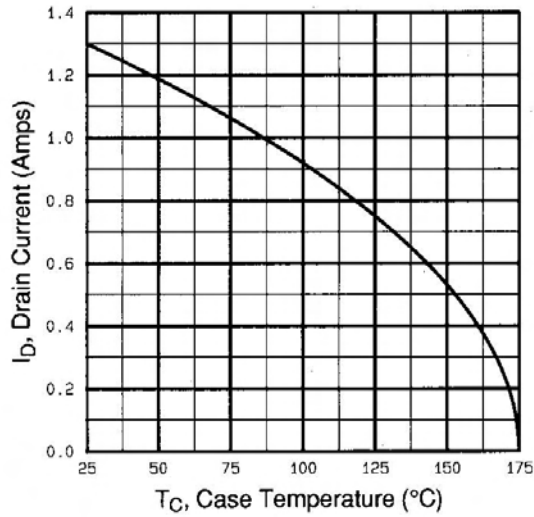


Fig 9. Maximum Drain Current Vs. Case Temperature

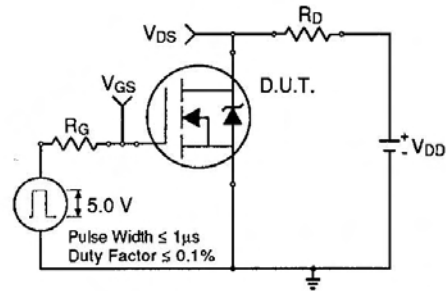


Fig 10a. Switching Time Test Circuit

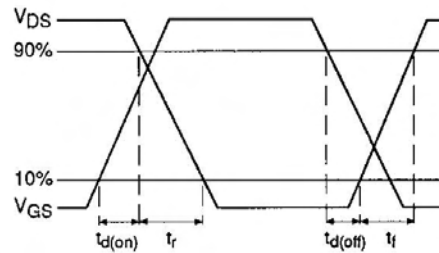


Fig 10b. Switching Time Waveforms

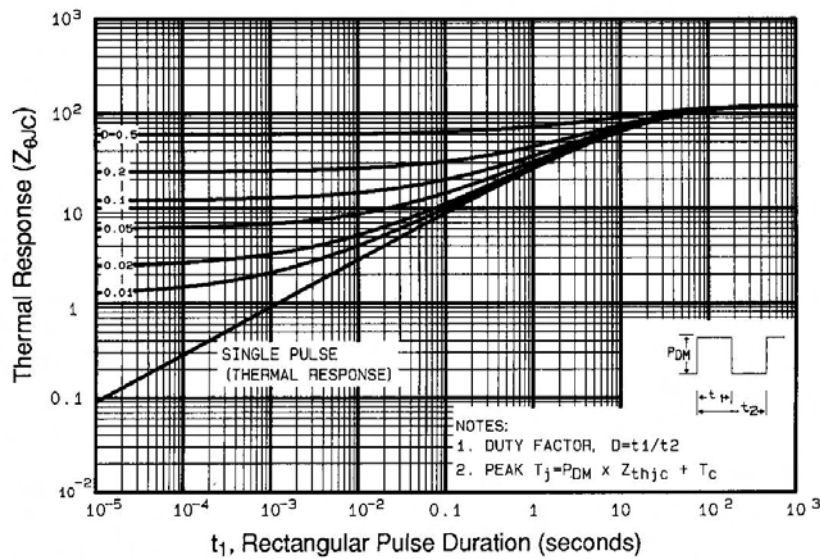


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

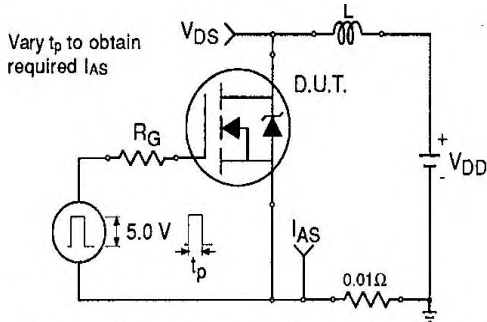


Fig 12a. Unclamped Inductive Test Circuit

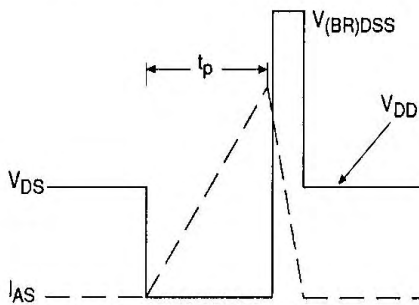


Fig 12b. Unclamped Inductive Waveforms

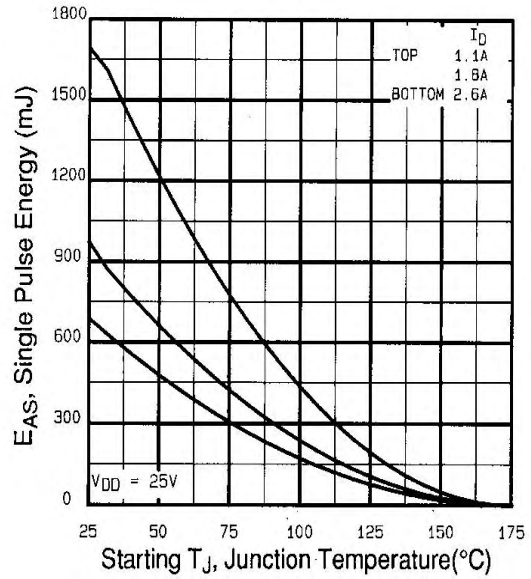


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

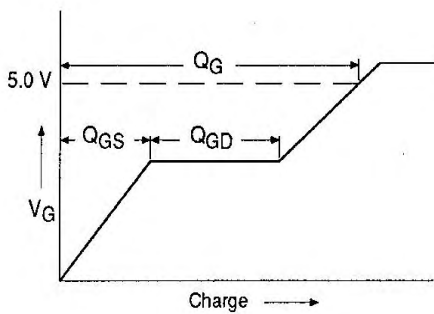


Fig 13a. Basic Gate Charge Waveform

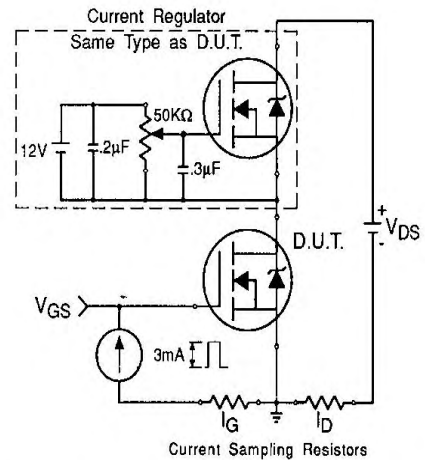
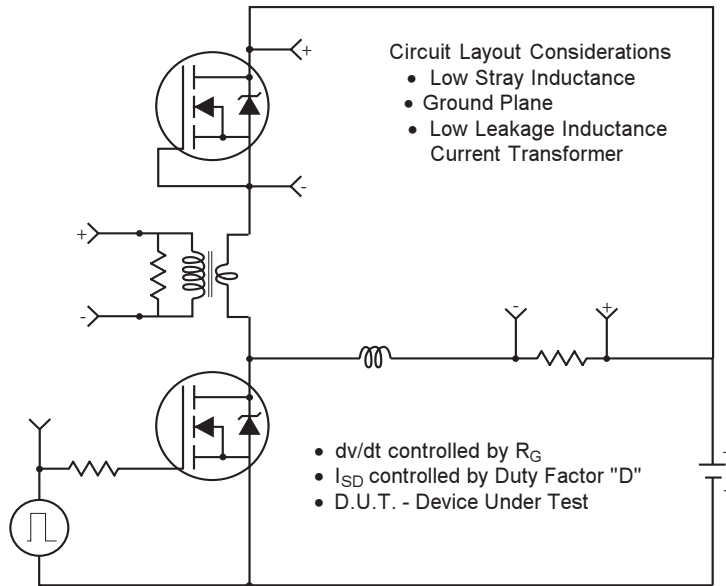
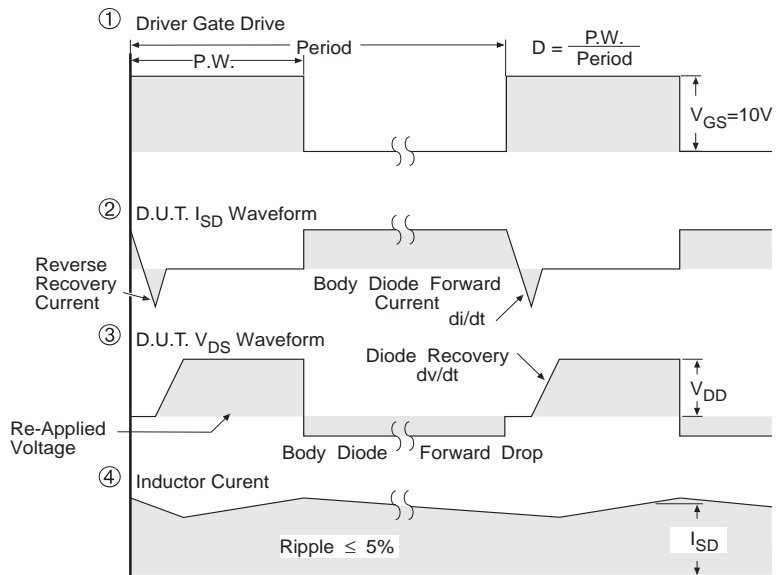


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel
** Use P-Channel Driver for P-Channel Measurements



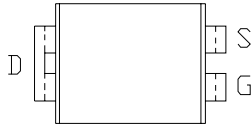
*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14 For N Channel HEXFETS

IRLD120PbF

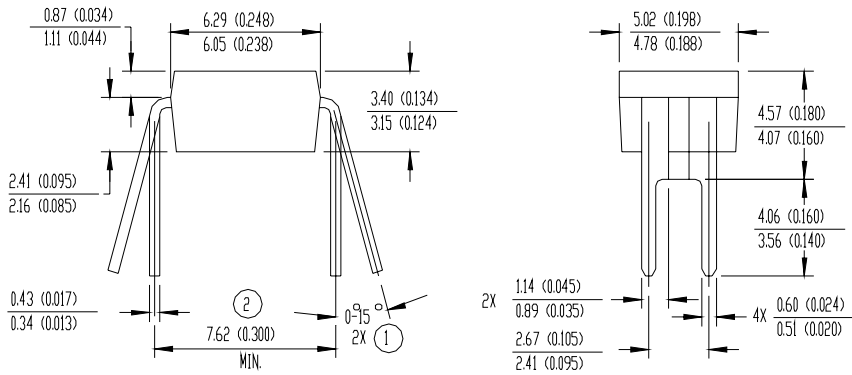
Hexdip Package Outline

International
IR Rectifier



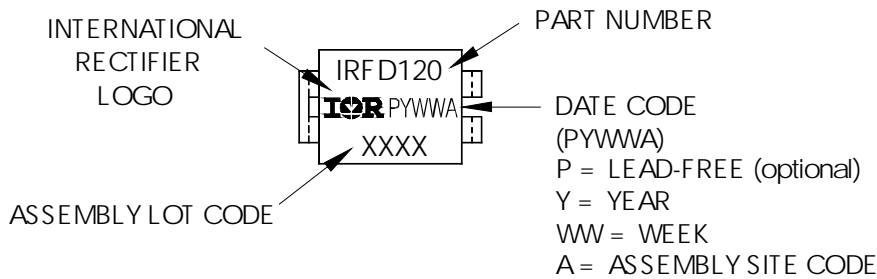
NOTES:

- ① APPLIES TO SPREAD OF LEADS PRIOR TO INSTALLATION
- ② APPLIES TO INSTALLED LEAD CENTERS
- 3 CONTROLLING DIMENSION: INCH
- 4 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES)
- 5 CASE STYLE HD-1 (SIMILAR TO JEDEC OUTLINE MO-001AN)
- 6 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP
SOLDER DIP MAX. + 0.16 (0.006)



Hexdip Part Marking Information

EXAMPLE: THIS IS AN IRFD120



Data and specifications subject to change without notice.

International
IR Rectifier

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TAC Fax: (310) 252-7903

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